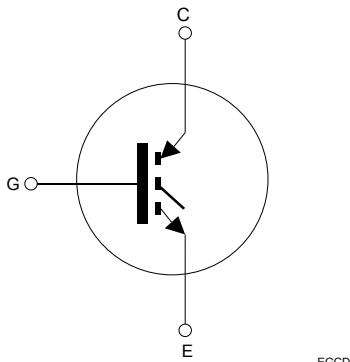


Trench gate field-stop 650 V, 75 A high-speed HB2 series IGBT die in D7 packing



Features

- Maximum junction temperature: $T_J = 175\text{ °C}$
- Low $V_{CE(sat)} = 1.55\text{ V (typ.) @ } I_C = 75\text{ A}$
- Minimized tail current
- Tight parameter distribution
- Positive $V_{CE(sat)}$ temperature coefficient

Applications

- Welding
- PFC converters
- Solar inverters
- Uninterruptable power supplies (UPS)
- EV charging

Description

The newest IGBT 650 V HB2 series represents an evolution of the advanced proprietary trench gate field-stop structure. The performance of the HB2 series is optimized in terms of conduction, thanks to a better $V_{CE(sat)}$ behavior at low current values, as well as in terms of reduced switching energy. The result is a product specifically designed to maximize efficiency for a wide range of fast applications.



Product status link

[STG75H65FB2D7](#)

Product summary

Order code	STG75H65FB2D7
V_{CE}	650 V
I_{CN}	75 A
Die size	5.30 x 4.30 mm
Packing	D7

1 Mechanical parameters

Table 1. Mechanical parameters

Symbol	Value	Unit
Die size including scribe line	5.30 x 4.30	mm
Wafer size	200	mm
Maximum possible dice per wafer	1207	dice
Die thickness	70	µm
Front side passivation	Silicon nitride	
Emitter pad size including gate pad	4.62 x 1.68	mm
Gate pad size	0.46 x 0.46	mm
Front side metallization	composition	AlCu
	thickness	4.5
Back side metallization	composition	Al/Ti/NiV/Ag
	thickness	0.65
Die bond	Electrically conductive glue or soft solder	
Recommended wire bonding	≤500	µm

2 Electrical ratings

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0\text{ V}$)	650	V
V_{GE}	Gate-emitter voltage	± 20	V
$I_{CN}^{(1)}$	Continuous collector current at $T = 100\text{ °C}$	71	A
$I_{CP}^{(1)(2)}$	Pulsed collector current	225	A
T_J	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$

1. Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.
2. Pulse width is limited by maximum junction temperature. Specified by design, not tested in production.

3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$I_C = 1\text{ mA}$, $V_{GE} = 0\text{ V}$	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 15\text{ A}$			1.75	V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 1\text{ mA}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{GE} = 0\text{ V}$, $V_{CE} = 650\text{ V}$			25	μA
I_{GES}	Gate-emitter leakage current	$V_{CE} = 0\text{ V}$, $V_{GE} = \pm 20\text{ V}$			± 250	nA

Table 4. Electrical characteristics (evaluated by design/characterization, not tested in production)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 75\text{ A}$	-	1.55	2.00	V
		$V_{GE} = 15\text{ V}$, $I_C = 75\text{ A}$, $T_J = 175\text{ °C}$	-	1.90		
C_{ies}	Input capacitance	$V_{CE} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GE} = 0\text{ V}$	-	4357		pF
C_{oes}	Output capacitance		-	264		pF
C_{res}	Reverse transfer capacitance		-	117		pF
Q_g	Total gate charge	$V_{CC} = 520\text{ V}$, $I_C = 75\text{ A}$, $V_{GE} = 0\text{ to }15\text{ V}$	-	207		nC

Table 5. Switching characteristics on inductive load

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$, $I_C = 75\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 2.2\ \Omega$	-	28	-	ns
t_r	Current rise time		-	16	-	ns
$t_{d(off)}$	Turn-off-delay time		-	100	-	ns
t_f	Current fall time		-	36	-	ns
$E_{off}^{(1)}$	Turn-off switching energy		-	1050	-	μJ
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$, $I_C = 75\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 2.2\ \Omega$, $T_J = 175\text{ °C}$	-	27	-	ns
t_r	Current rise time		-	17	-	ns
$t_{d(off)}$	Turn-off-delay time		-	123	-	ns
t_f	Current fall time		-	87	-	ns
$E_{off}^{(1)}$	Turn-off switching energy		-	1770	-	μJ

1. Including the tail of the collector current.

Note: The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology. Refer to STGWA75H65DFB2 datasheet for further information.

4 Die layout

Figure 1. Die drawing (dimensions are in mm)

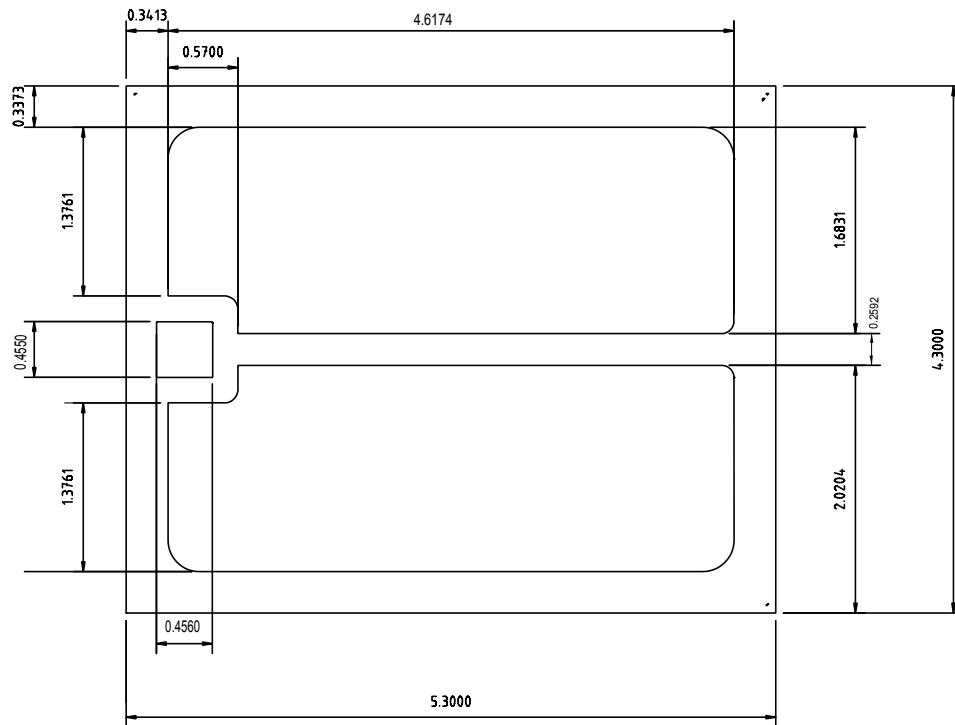
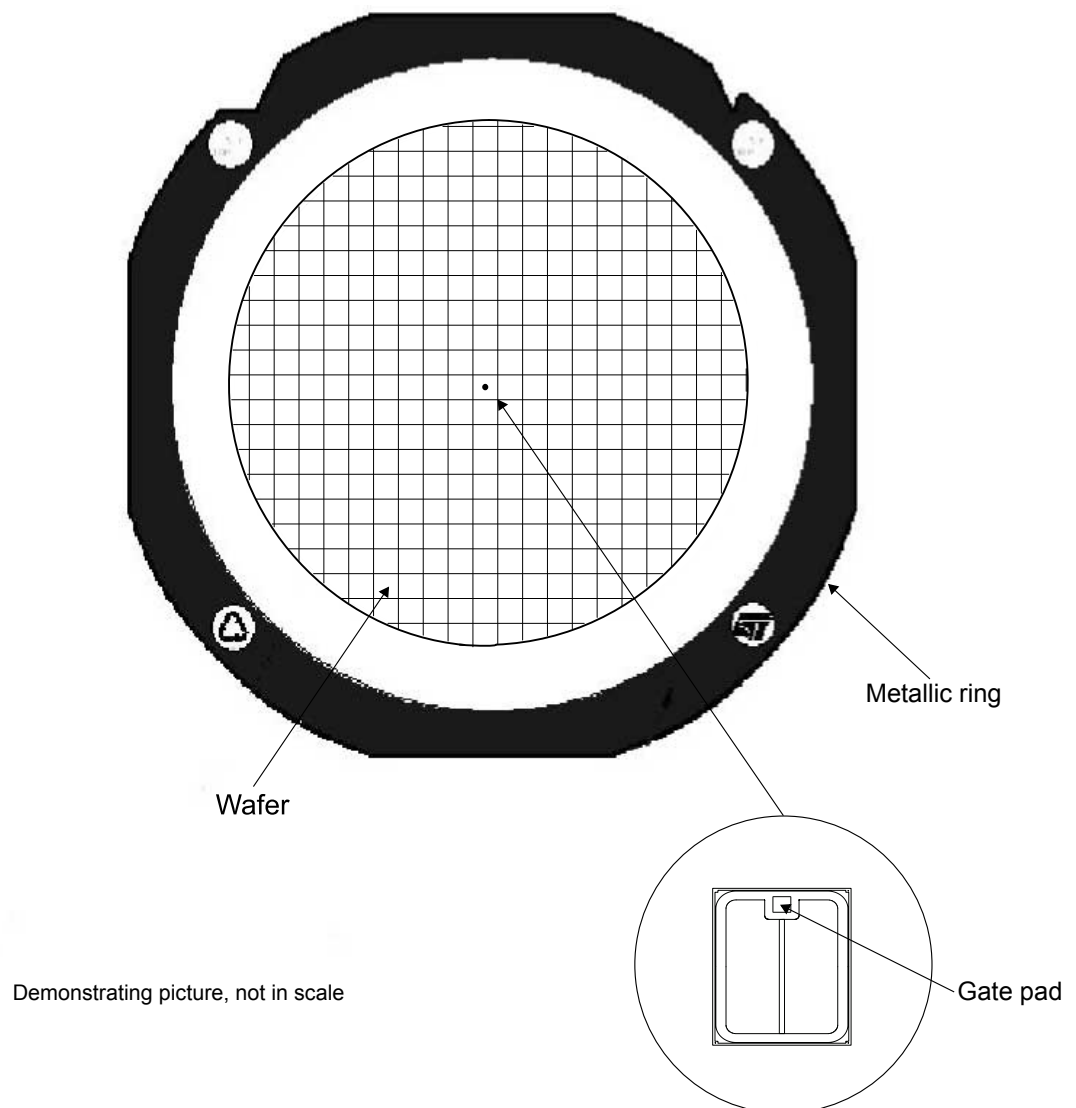


Table 6. Die delivery

Packing	Description	Details
D7	Wafer tested, inked or inkless, cut on sticky foil on 10.8" (276 mm) ring (see Figure 2. D7 drawing and die orientation).	Wafer is held by ring and placed in a proper box, containing a maximum of 25 wafers, sealed under vacuum inside a plastic envelope. The latter is protected by two foam shells and then sealed in a carton box.

Figure 2. D7 drawing and die orientation



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5 Additional information

5.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (that is for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

5.2 Shipping

Several shipping options are offered. Consult the local ST sales office for availability:

- Die on film-sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

5.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die is not to be handled with tweezers. A vacuum wand with a nonmetallic ESD protected tip should be used.

5.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is $18\text{ °C} \pm 2\text{ °C}$ with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by the customer.

After the customer opens the package, the customer is responsible for the products.

Revision history

Table 7. Document revision history

Date	Revision	Changes
07-Apr-2020	1	Initial release.
16-Aug-2022	2	Moved "2.1 <i>Absolute maximum ratings</i> " content as Section 2 Electrical ratings . Moved "2.2 <i>Electrical characteristics</i> " content as Section 3 Electrical characteristics . Updated Table 6. Die delivery . Minor text changes.

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