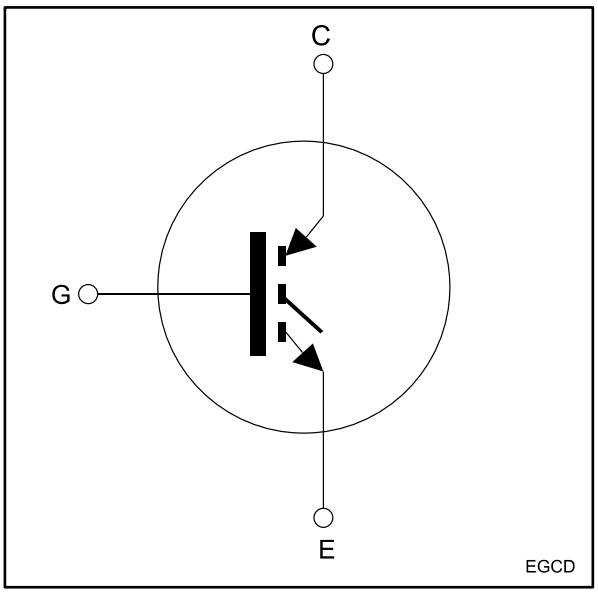
# STG80H65FBD7

## 650 V, 80 A trench gate field-stop HB series high-speed IGBT die in D7 packing

Datasheet - production data




## Features

- Maximum junction temperature: $T_J$ = 175 °C
- High-speed switching series
- Minimized tail current
- $V_{CE(sat)}$ = 1.6 V (typ.) @ $I_C$ = 80 A
- Tight parameter distribution
- Safer paralleling

## Applications

- Solar
- UPS
- Welding
- High-frequency converters
- PFC

## Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the new HB series of IGBTs, which represents an optimum compromise between conduction and switching loss to maximize the efficiency of any frequency converter. Furthermore, the slightly positive $V_{CE(sat)}$ temperature coefficient and very tight parameter distribution result in safer paralleling operation.

**Table 1: Device summary**

| Order code | $V_{CE}$ | $I_{CN}$ | Die size | Packing |
|---|---|---|---|---|
| STG80H65FBD7 | 650 V | 80 A | 6.50 x 6.30 mm² | D7 |

# Contents

# 1 Mechanical parameters

**Table 2: Mechanical parameters**

| Symbol | | Value | Unit |
|---|---|---|---|
| Die size | | 6.50 x 6.30 | mm² |
| Wafer size | | 200 | mm |
| Die thickness | | 70 | µm |
| Maximum possible dice per wafer | | 654 | dice |
| Front side passivation | | Silicone nitride | |
| Emitter pad size E1 (x1) | | 5.45 x 1.85 | mm² |
| Emitter pad size E2 (x2) | | 5.84 x 1.65 | mm² |
| Gate pad size | | 0.37 x 0.50 | mm² |
| Front side metallization | Composition | AlCu | |
| | Thickness | 4.5 | µm |
| Back side metallization | Composition | Al/Ti/NiV/Ag | |
| | Thickness | 0.65 | µm |
| Die bond | | Electrically conductive glue or soft solder | |
| Recommended wire bonding | | ≤500 | µm |

# 2 Electrical ratings

## 2.1 Absolute maximum ratings

**Table 3: Absolute maximum ratings ($T_J$ = 25 °C unless otherwise specified)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage ($V_{GE}$ = 0 V) | 650 | V |
| $V_{GE}$ | Gate-emitter voltage | ±20 | V |
| $I_C$ (1) | Continuous collector current at T = 100 °C | 80 | A |
| $I_{CP}$ (1)(2) | Pulsed collector current | 240 | A |
| $T_J$ | Operating junction temperature range | -55 to 175 | °C |

**Notes:**

(1)Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.

(2)Pulse width is limited by maximum junction temperature.

## 2.2 Electrical characteristics

**Table 4: Static characteristics (tested on wafer unless otherwise specified)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)CES}$ | Collector-emitter breakdown voltage | $I_C$ = 2 mA, $V_{GE}$ = 0 V | 650 | | | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_{GE}$ = 15 V, $I_C$ = 15 A | | | 2.1 | V |
| $V_{GE(th)}$ | Gate threshold voltage | $V_{CE}$ = $V_{GE}$, $I_C$ = 1 mA | 5 | 6 | 7 | V |
| $I_{CES}$ | Collector cut-off current | $V_{GE}$ = 0 V, $V_{CE}$ = 650 V | | | 100 | µA |
| $I_{GES}$ | Gate-emitter leakage current | $V_{GE}$ = ±20 V, $V_{CE}$ = 0 V | | | ±250 | µA |

**Table 5: Electrical characteristics (not tested at chip level, verified by design/characterization)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_{GE}$ = 15 V, $I_C$ = 80 A | - | 1.6 | 2 | V |
| | | $V_{GE}$ = 15 V, $I_C$ = 80 A, $T_J$ = 175 °C | - | 1.9 | | V |
| $C_{ies}$ | Input capacitance | $V_{CE}$ = 25 V, f = 1 MHz, $V_{GE}$ = 0 V | - | 10524 | | pF |
| $C_{oes}$ | Output capacitance | | - | 385 | | pF |
| $C_{res}$ | Reverse transfer capacitance | | - | 215 | | pF |
| $Q_g$ | Total gate charge | $V_{CC}$ = 520 V, $I_C$ = 80 A, $V_{GE}$ = 0 to 15 V | - | 414 | | nC |

**Table 6: Switching characteristics on inductive load**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{CC}$ = 400 V, $I_C$ = 80 A, $V_{GE}$ = 15 V, $R_G$ = 10 Ω | - | 84 | - | ns |
| $t_r$ | Current rise time | | - | 52 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 280 | - | ns |
| $t_f$ | Current fall time | | - | 31 | - | ns |
| $E_{off}$(1) | Turn-off switching energy | | - | 1.5 | - | mJ |
| $t_{d(on)}$ | Turn-on delay time | $V_{CC}$ = 400 V, $I_C$ = 80 A, $V_{GE}$ = 15 V, $R_G$ = 10 Ω, $T_J$ = 175 °C | - | 77 | - | ns |
| $t_r$ | Current rise time | | - | 51 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 328 | - | ns |
| $t_f$ | Current fall time | | - | 30 | - | ns |
| $E_{off}$(1) | Turn-off switching energy | | - | 2.1 | - | mJ |

**Notes:**

(1)Including the tail of the collector current.

The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology. Refer to the STGWA80H65FB datasheet for further information.

# 3 Die layout

**Figure 1: Die drawing (dimensions are in mm)**

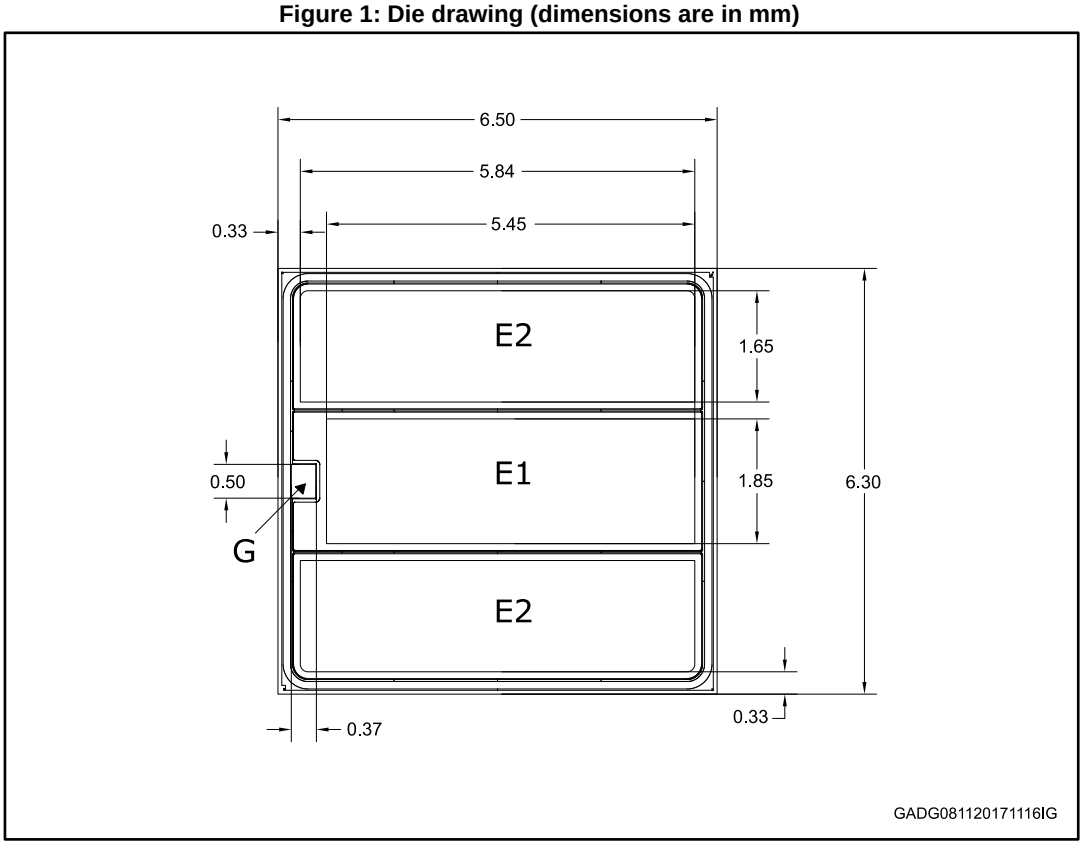
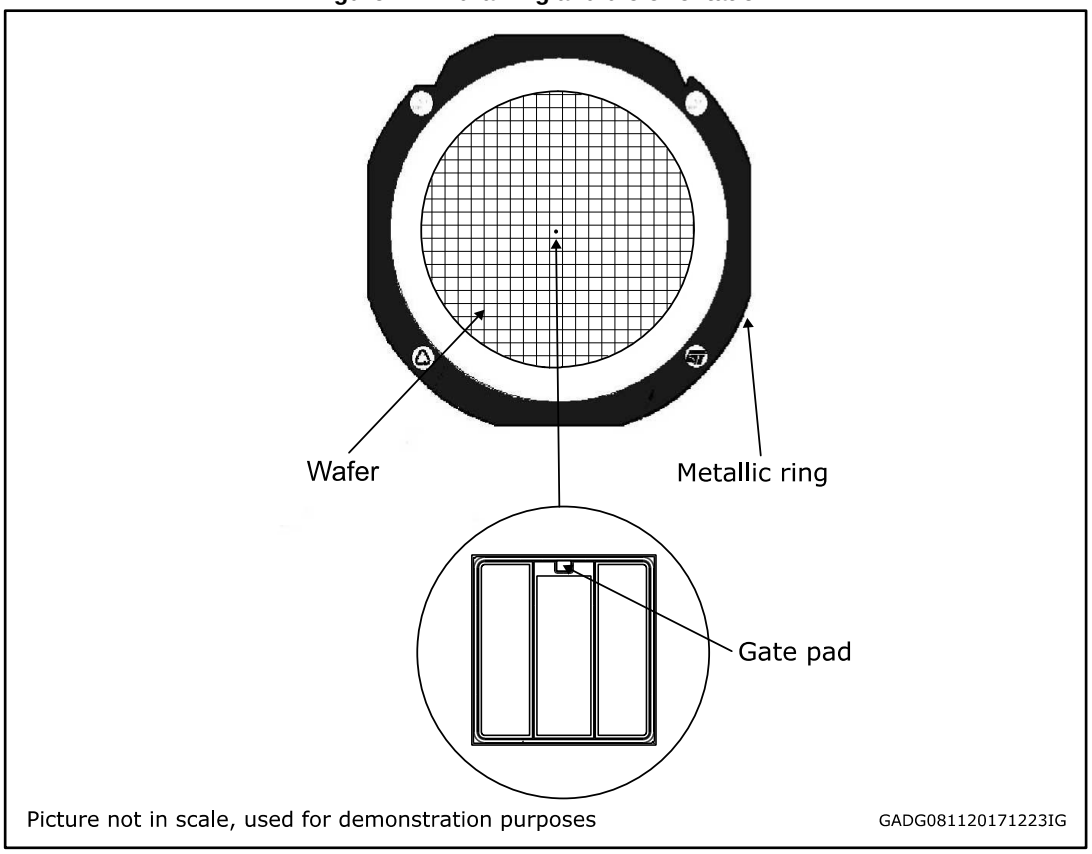



**Table 7: Die delivery**

| Package option | Description | Details |
|---|---|---|
| D7 | Wafer (8 inches) tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see *Figure 2: "D7 drawing and die orientation"*) | The wafer (8 inches) is held by a ring protected by two carton shells inside a plastic vacuum-sealed envelope. The maximum number of wafers for each package is 5, weight is about 3.7 kg. |

**Figure 2: D7 drawing and die orientation**



# 4 Additional information

## 4.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (i.e. for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

## 4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

## 4.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

## 4.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is 18 °C ±2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by customer.

After the customer opens the package, the customer is responsible for the products.

# 5 Revision history

Table 8: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 08-Nov-2017 | 1 | Initial release |

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