STGAP2HSA

Automotive grade galvanically isolated 4 A single gate driver
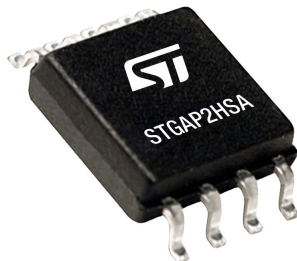
SO-8W

Product status link
STGAP2HSA

Product label
SUSTAINABLE TECHNOLOGY

Features

- AEC-Q100 qualified
- Driver current capability: 4 A sink/source @25°C
- 100 V/ns Common Mode Transient Immunity (CMTI)
- Overall input-output propagation delay: 60 ns
- Rail-to-rail outputs
- 4 A Miller CLAMP dedicated pin
- UVLO function
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shut-down protection
- Standby function
- Wide body SO-8W package
- Galvanic isolation
  - High voltage rail up to 1200 V
  - 5000 V_{PK} isolation, IEC 60747-17 certified
  - 6000 V_{PK} surge
  - 3500 V_{RMS} isolation rating for 1 minute, UL 1577 recognized

Applications

- DC-DC converters
- On-board charger (OBC)
- DC charging stations
- Automotive HVAC compressors
- Fans and pumps
- Heaters
- 600/1200 V inverters
- Motor drivers for EV

Description

The STGAP2HSA is a single gate driver which provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for mid and high power applications such as power conversion and motor driver inverters in industrial applications. The device has a single output pin and Miller CLAMP function that prevents gate spikes during fast commutations in half-bridge topologies. This configuration provides high flexibility and bill of material reduction for external components.

DS15065 - Rev 1 - September 2025
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The device integrates protection functions: UVLO with optimized value for Si MOSFETs and thermal shut down are included to facilitate the design of highly reliable systems. Dual input pins allow the selection of signal polarity control and implementation of HW interlocking protection to avoid cross-conduction in case of controller malfunction. The input to output propagation delay is less than 60 ns, which delivers high PWM control accuracy. A standby mode is available to reduce idle power consumption.

1   Block diagram

Figure 1. Block diagram
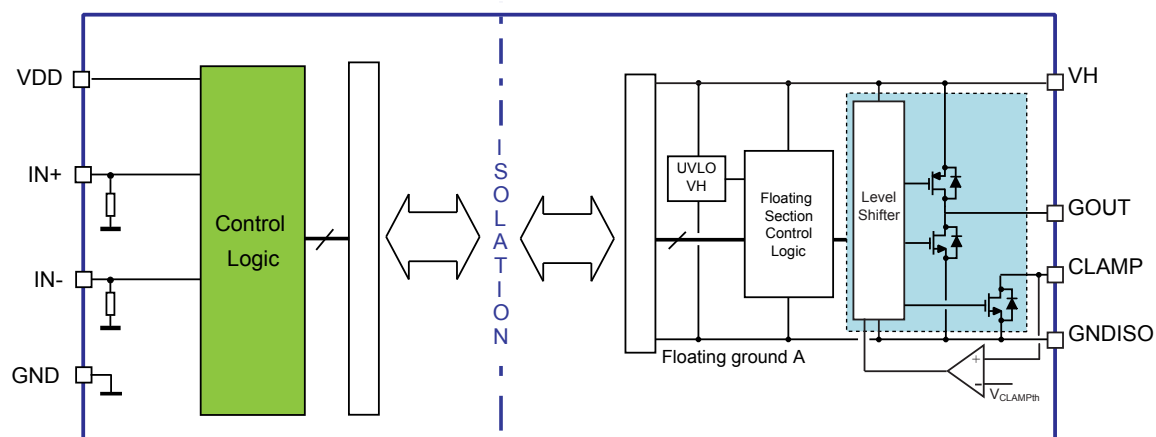
2 Pin description and connection diagram
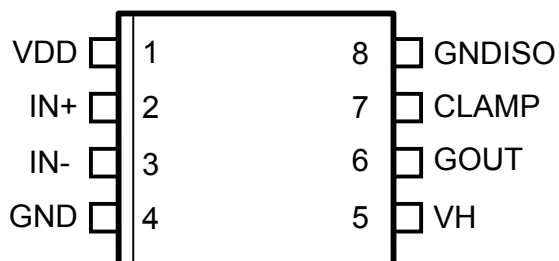
Figure 2. Pin connection (top view)

Table 1. Pin Description

Pin #	Pin Name	Type	Function
1	VDD	Power Supply	Driver logic supply voltage.
2	IN+	Logic Input	Driver logic input, active high.
3	IN-	Logic Input	Driver logic input, active low.
4	GND	Power Supply	Driver logic ground.
5	VH	Power Supply	Gate driving positive voltage supply.
6	GOUT	Analog Output	Sink/Source output.
7	CLAMP	Analog Output	Active Miller Clamp.
8	GNDISO	Power Supply	Gate driving Isolated ground.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. **Absolute maximum ratings**

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	-0.3	6	V
V_{LOGIC}	Logic pins voltage vs. GND	-	-0.3	6	V
VH	Positive supply voltage (VH vs. GNDISO)	-	-0.3	28	V
V_{OUT}	Voltage on gate driver outputs (GON, GOFF, CLAMP VS. GNDISO)	-	-0.3	VH+0.3	V
T_J	Junction temperature	-	-40	150	°C
T_{stg}	Storage temperature	-	-50	150	°C
ESD	HBM (human body model)	-		2	kV

3.2 Recommended operating conditions

Table 3. **Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	3.1	4.0	V
V_{LOGIC}	Logic pins voltage vs. GND	-	0	5.5	V
VH	Positive supply voltage (VH vs. GNDISO)	-	Max(VH$_{ON}$)	26	V
F_{SW}	Maximum switching frequency[1]	-	-	1	MHz
t_{OUT}	Output pulse width (GOUT, GON-GOFF)	-	100	-	ns
T_J	Operating Junction temperature	-	-40	125	°C
T_{amb}	Ambient temperature	-	-40	125	°C

1. *Actual limit depends on power dissipation and T_J.*

3.3 Thermal data

Table 4. **Thermal data**

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-8W	120	°C/W

4 Electrical characteristics

Test Conditions: -40 °C ≤ T_J ≤ 125 °C, VH = 15 V, VDD = 3.3 V unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test conditions		Min	Typ	Max	Unit
Dynamic characteristics								
t_{Don}	IN+, IN-	Input to output propagation delay ON	T_J = 25 °C			60		ns
			-40 °C ≤ T_J ≤ +125 °C		40	-	90	
t_{Doff}	IN+, IN-	Input to output propagation delay OFF	T_J = 25 °C			60		ns
			-40 °C ≤ T_J ≤ +125 °C		40	-	90	
PWD		Pulse Width Distortion $\lvert t_{Don} - t_{Doff}\rvert$					8	ns
t_r		Rise time	T_J = 25 °C, C_L= 4.7 nF		-	30	-	ns
t_f		Fall time	See Figure 11		-	30	-	ns
CMTI [1]		Common-mode transient immunity $\lvert dV_{ISO}/dt\rvert$	V_{CM} = 1500 V See Figure 12		100			V/ns
Supply voltage								
VH_{on}	VH	VH UVLO turn on threshold			8.6	9.1	9.6	V
VH_{off}	VH	VH UVLO turn off threshold			7.9	8.4	8.9	V
VH_{hyst}	VH	VH UVLO hysteresis			0.55	0.71	0.8	V
I_{QHU}	VH	VH under-voltage quiescent supply current	VH = 7 V			1.3	1.9	mA
I_{QH}	VH	VH quiescent supply current				1.3	1.9	mA
I_{QHSBY}	VH	Stand-by VH quiescent supply current	Standby mode			400	550	µA
SafeClp	GOUT / GOFF	GOFF active clamp	I_{GOFF} = 0.2 A VH floating	T_J = 25° C		1.9	2.2	V
				-40°C ≤ T_J ≤ +125°C			3.0	
I_{QDD}	VDD	VDD quiescent supply current				1	1.3	mA
I_{QDDSBY}	VDD	Stand-by VDD quiescent supply current	Standby mode			40	100	µA
Logic Inputs								
V_{il}	IN+, IN-	Low level logic threshold voltage			0.29·VDD	1/3·VDD	0.39·VDD	V
V_{ih}	IN+, IN-	High level logic threshold voltage			0.58·VDD	2/3·VDD	0.7·VDD	V
I_{INh}	IN+, IN-	INx logic "1" input bias current	INx = 5 V		30	50	60	µA
I_{INl}	IN+, IN-	INx logic "0" input bias current	INx = GND				1	µA
R_{pd}	IN+, IN-	Inputs pull-down resistors	INx = 5 V		85	100	155	kΩ

Symbol	Pin	Parameter	Test conditions	Min	Typ	Max	Unit
Driver buffer section							
I_{GON}	GOUT / GON	Source short circuit current	$T_J = 25$ °C [1]		4.4		A
			-40 °C ≤ T_J ≤ 125 °C	3		5.5	
V_{GONH}	GOUT / GON	Source output high level voltage	$I_{GON} = 100$ mA	VH-0.21	VH-0.11		V
R_{GON}	GOUT / GON	Source R_{DS_ON}	$I_{GON} = 100$ mA		1.12	2.11	Ω
I_{GOFF}	GOUT / GOFF	Sink short circuit current	$T_J = 25$ °C [1]		4		A
			-40 °C ≤ T_J ≤ 125 °C	2.4		5.5	
V_{GOFFL}	GOUT / GOFF	Sink output low level voltage	$I_{GOFF} = 100$ mA		89.7	160	mV
R_{GOFF}	GOUT / GOFF	Sink R_{DS_ON}	$I_{GOFF} = 100$ mA		0.897	1.60	Ω
Clamp Miller function							
$V_{CLAMPth}$	CLAMP	CLAMP voltage threshold	V_{CLAMP} vs. GNDISO	1.3	2	2.6	V
I_{CLAMP}	CLAMP	CLAMP short circuit current	$V_{CLAMP} = 15$ V $T_J = 25$ °C [1]		4		A
			-40 °C ≤ T_J ≤ 125 °C	2.4		5.0	
V_{CLAMP_L}	CLAMP	CLAMP low level output voltage	$I_{CLAMP} = 100$ mA		96	160	mV
R_{CLAMP}	CLAMP	CLAMP R_{DS_ON}	$I_{CLAMP} = 100$ mA		0.96	1.60	Ω
Over-temperature protection							
T_{SD}		Shut down temperature [1]		170			°C
T_{hys}		Temperature hysteresis [1]			20		°C
Stand-by							
t_{STBY}		Stand-by time	See Section 6.7	200	280	500	µs
t_{WUP}		Wake-up time	See Section 6.7	10	20	35	µs
t_{awake}		Wake-up delay	See Section 6.7	90	130	200	µs
$t_{stbyfilt}$		Stand-by filter	See Section 6.7	200	280	800	ns

1. *Characterization data, not tested in production*

5 Isolation

Table 6. Isolation and safety specifications

Symbol	Parameter	Test Conditions	Value	Unit
General				
CLR	Clearance (Minimum external air Gap)	Measured from input terminals to output terminals, shortest distance trough air	8	mm
CPG	Creepage (Minimum External Tracking)	Measured from input terminals to output terminals, shortest distance path along body	8	mm
CTI	Comparative Tracking Index (Tracking Resistance)	IEC 60112	≥ 400	V
-	Material Group	According to IEC 60664-1	II	-
-	Overvoltage Category per IEC 60664-1	Rated mains voltages ≤ 150 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 300 V_{RMS}	I - III	-
		Rated mains voltages ≤ 600 V_{RMS}	I - II	-
		Rated mains voltages ≤ 1000 V_{RMS}	I	-
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage	1200	V_{PEAK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage (sinewave)	850	V_{RMS}
		DC voltage	1200	V_{PEAK}
V_{PR}	Partial Discharge test voltage	Method a, Type and sample test $V_{PR} = V_{IORM} \times 1.6$, t_m= 10 s Partial discharge < 5 pC	1920	V_{PEAK}
		Method b1, 100% Production test $V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s Partial discharge < 5 pC	2250	V_{PEAK}
V_{IOTM}	Maximum Transient Isolation Voltage	Method a, Type and sample test t_{ini} = 60 s	5000	V_{PEAK}
$V_{IOTM,test}$	Transient Isolation Voltage test	Method b1, 100% Production test $V_{IOTM,test} = V_{IOTM} \times 1.2$, t_{ini} = 1 s	6000	V_{PEAK}
V_{IMP}	Maximum Impulse Voltage	Type test; Tested in air 1.2/50 µs waveform per IEC 62368-1	4600	V_{PEAK}
V_{IOSM}	Maximum Surge isolation Voltage	Type test; Tested in oil 1.2/50 µs waveform per IEC 62368-1 $V_{IOSM} \geq V_{IMP} \times 1.3$	6000	V_{PEAK}
R_{IO}	isolation Resistance	Type and Sample test; V_{IO} = 500 V T_{amb} = 25 °C	> 10^{12}	Ω
		Type and Sample test; V_{IO} = 500 V $T_{amb,max}$ = 125 °C	> 10^{11}	
		Type and Sample test; V_{IO} = 500 V $T_{amb} = T_S$ = 150 °C	> 10^{9}	
IEC 60747-17 certification pending				

Symbol	Parameter	Test Conditions	Value	Unit
UL-1577				
V_{ISO}	Isolation Withstand voltage	60 s; Type test	3540 / 5000	V_{RMS} / V_{PEAK}
$V_{ISO,test}$	Isolation Voltage test	1 s; 100% production	4240 / 6000	V_{RMS} / V_{PEAK}

Table 7. Safety limits

Symbol	Parameter	Test condition	Value	Unit
T_S	Safety temperature		150	°C
P_{SI}	Maximum input power dissipation	$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150 °C VDD = 4.0 V	11	mW
P_{SO}	Maximum output power dissipation	$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150 °C	1.03	W
I_{SO}	Maximum output current	$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150 °C VH-GNDISO = 26 V	39	mA
		$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150 °C VH-GNDISO = 15 V	68	

Safety limitings are aimed at minimizing potential damage to the isolation barrier upon failure of input or output circuitry. Without current limiting, excessive power dissipation might damage the die and the isolation barrier consequently. The maximum limits of P_S and I_S should not be exceeded. These limits vary with the ambient temperature T_{amb}, according to the related derating curves.

Figure 3. Thermal derating curve for power safety limiting
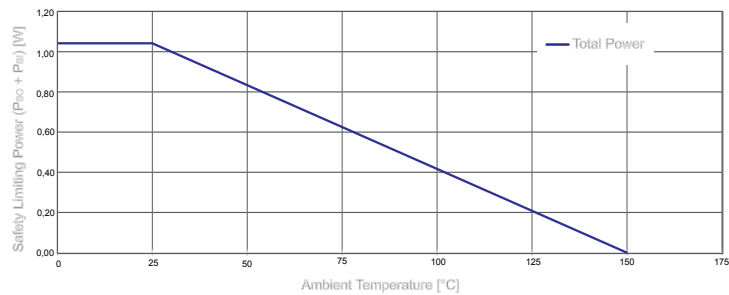
Figure 4. Thermal derating curves for current safety limiting
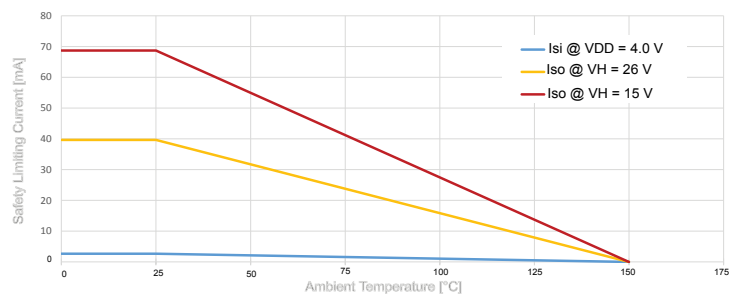
6 Functional description

6.1 Gate driving power supply and UVLO

The STGAP2HSA is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows implementation of either unipolar or bipolar gate driving.

Figure 5. Power supply configuration for unipolar and bipolar gate driving
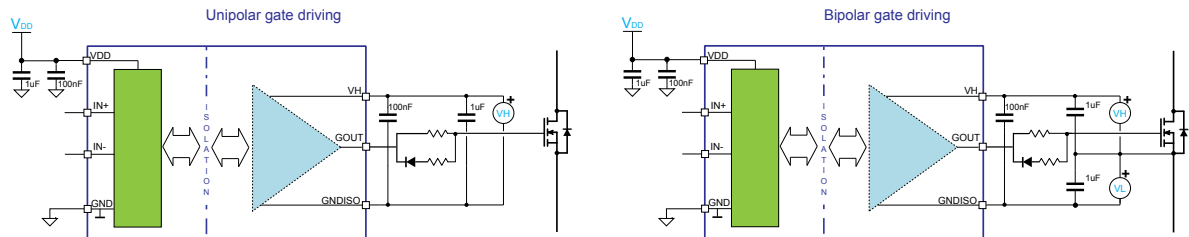
Undervoltage protection is available on VH supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH voltage falls below the VH_{off} threshold, the output buffer enters a "safe state". When VH voltage reaches the VH_{on} threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1 µF and 10 µF should be placed close to it.

6.2 Power-up, power-down and "safe state"

The following conditions define the "safe state":

• GOUT = OFF state;
• CLAMP = ON state;

Such conditions are maintained at power-up of the isolated side (VH < VH_{on}) and during whole device power down phase (VH < VH_{off}), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage sides, the device output state depends on the status of the input pins.

6.3 Control inputs

The device is controlled through the IN+ and IN- logic inputs, in accordance with the truth table below.

Table 8. Inputs truth table (applicable when device is not in UVLO or "safe state")

Input pins		Output pin
IN+	IN-	GOUT
L	L	LOW
H	L	**HIGH**
L	H	LOW
H	H	LOW

A deglitch filter allows input signals with duration shorter than tdeglitch to be ignored, thereby preventing noise spikes potentially present in the application from generating unwanted commutations.

6.4 Miller Clamp function

The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the C_{GD} capacitance.

During the turn-off period the gate of the external switch is monitored through the CLAMP pin. The CLAMP switch is activated when gate voltage goes below the voltage threshold, $V_{CLAMPth}$, thus creating a low impedance path between the switch gate and the GNDISO pin.

6.5 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced in "safe state" until communication link is properly established again.

6.6 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the T_{SD} temperature threshold, the device is forced in "safe state". The device operation is restored as soon as the junction temperature is lower than '$T_{SD} - T_{hys}$'.

6.7 Standby function

In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH supply pins is reduced to I_{QDDSBY} and I_{QHSBY} respectively, and the output remains in "safe state" (the output is actively forced low).

The way to enter standby is to keep both IN+ and IN- high ("standby" value) for a time longer than t_{STBY}. During stand-by the inputs can change from the "standby" value.

To exit stand-by, IN+ and IN- must be put in any combination different from the "standby" value for a time longer than $t_{stbyfilt}$, and then in the "standby" value for a time t such that $t_{WUP} < t < t_{STBY}$.

When the input configuration is changed from the "standby" value the output is enabled and set according to inputs state after a time t_{awake}.

Figure 6. Standby state sequences
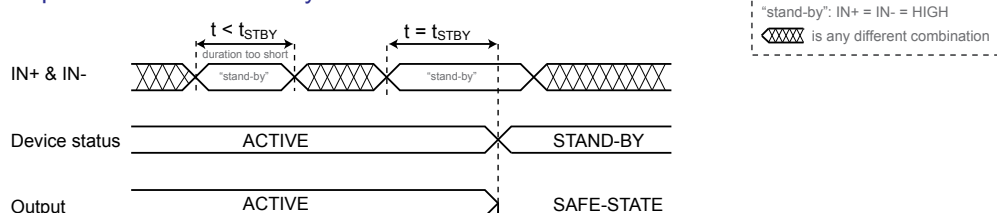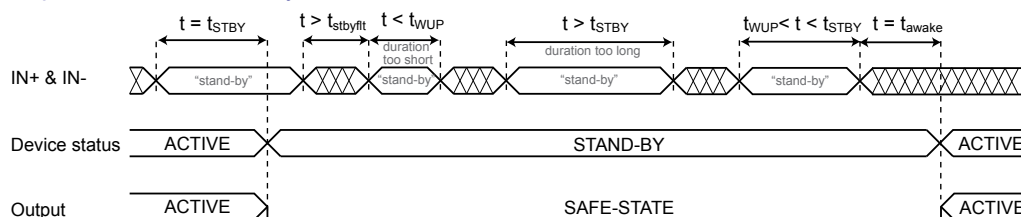
7 Typical application diagram

Figure 7. Typical application diagram - Miller Clamp
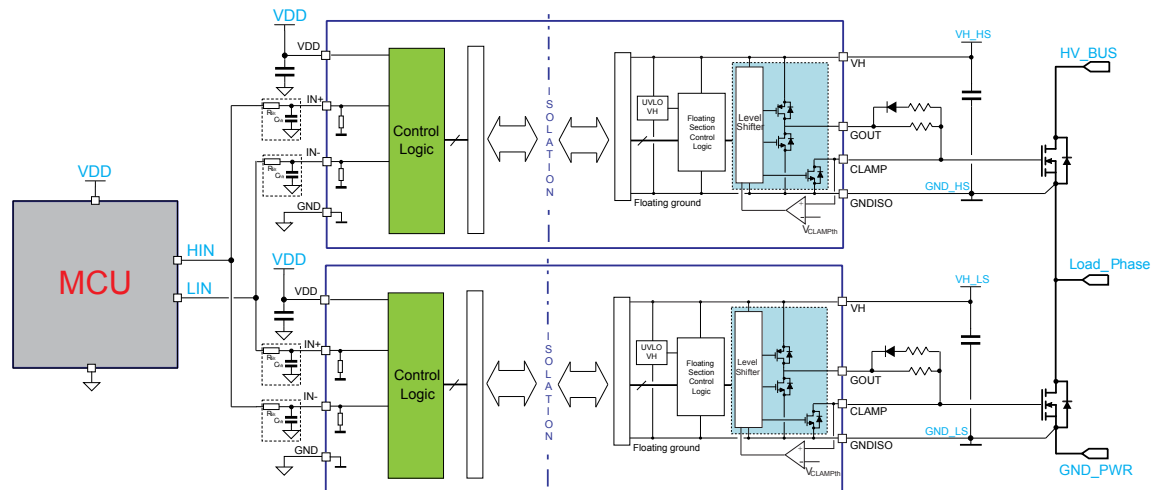
Figure 8. Typical application diagram - Miller Clamp and negative gate driving
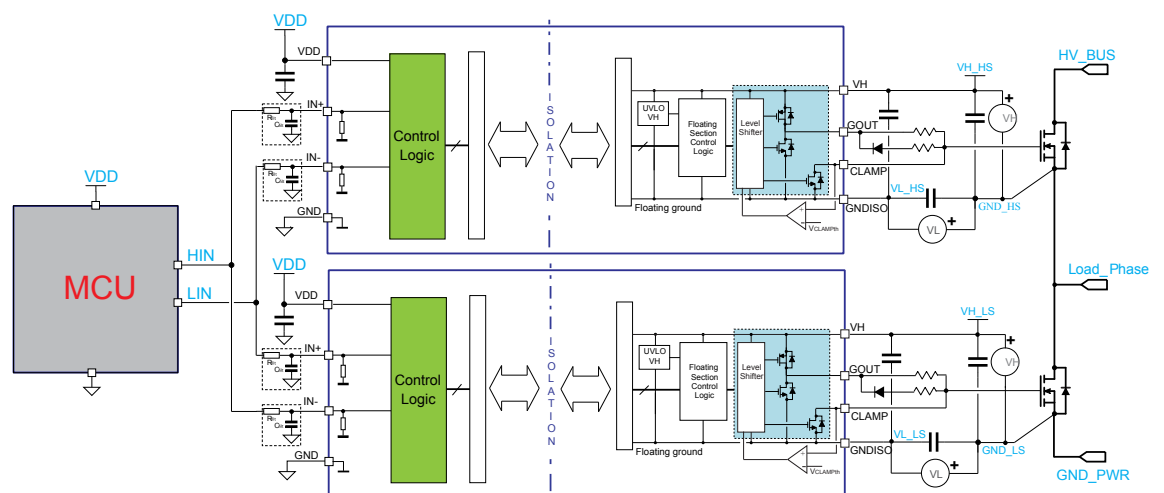
8 Layout

8.1 Layout guidelines and considerations

In order to optimize the PCB layout, the following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pins. A 100 nF capacitor must be placed between VDD and GND and between VH and GNDISO, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current, a second capacitor with a value between 1 µF and 10 µF should also be placed close to the supply pins.

- It is good practice to add filtering capacitors close to logic inputs of the device (IN+, IN-), particularly for fast switching or noisy applications.

- The power transistors must be placed as close as possible to the gate driver to minimize the gate loop area and inductance that might carry noise or cause ringing.

- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.

- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

An example of STGAP2HSA suggested PCB layout with main signals highlighted by different colors is shown in Figure 9 (see Figure 10 for reference schematic). It is recommended to follow this example for correct positioning and connection of filtering capacitors.

Figure 9. STGAP2HSA suggested PCB layout: top and bottom

TOP　　　　　　　　　　BOTTOM
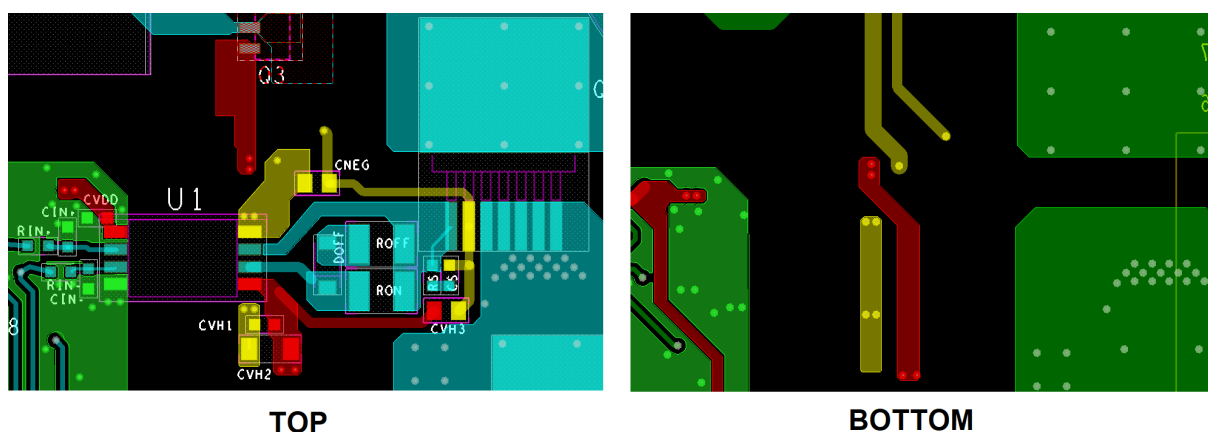
Figure 10. STGAP2HSA reference schematic for suggested PCB layout
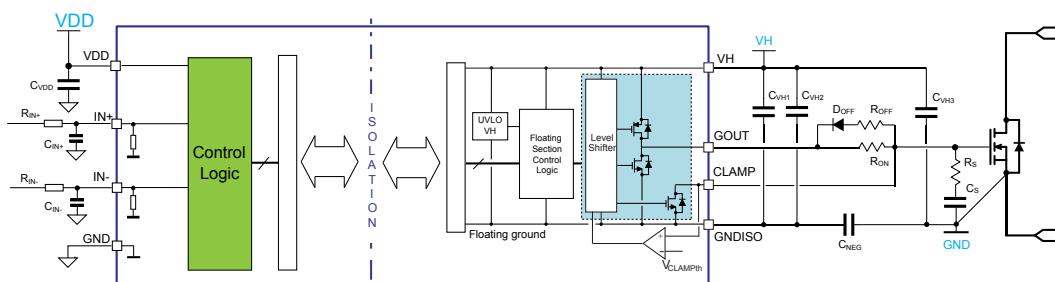
9 Testing and characterization information

Figure 11. Timings definition
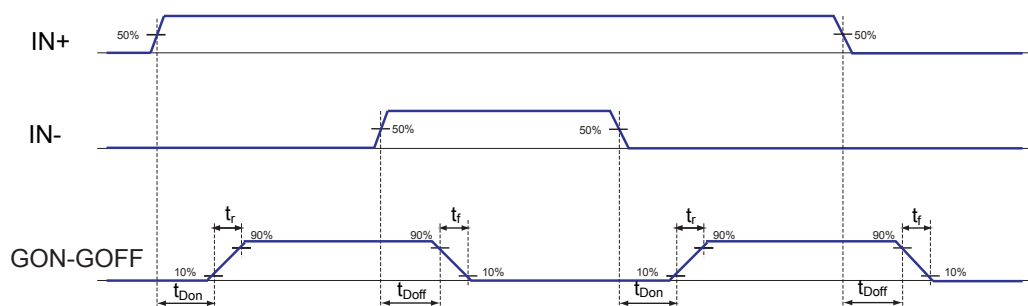
Figure 12. CMTI test circuit
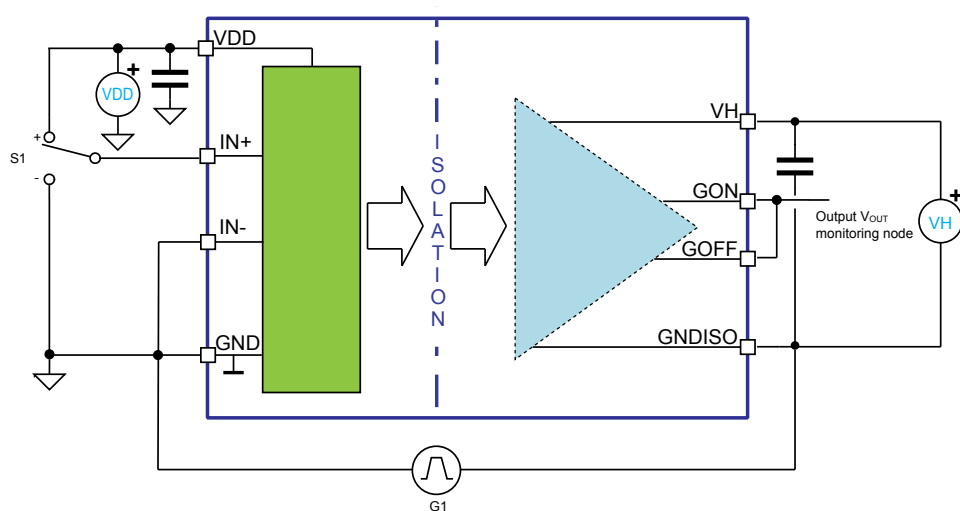
10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO-8W package information

Table 9. SO-8W package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max
A	2.34		2.64
A1	0.1		0.3
b	0.3		0.51
c	0.2		0.33
D[1]	5.64		6.05
e	1.27 BSC		
E1	7.39		7.59
E	10.11		10.52
L	0.61		0.91
h	0.25		0.76
Θ	0°		8°
aaa	0.25		
bbb	0.25		
ccc	0.1		

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

Figure 13. SO-8W mechanical data
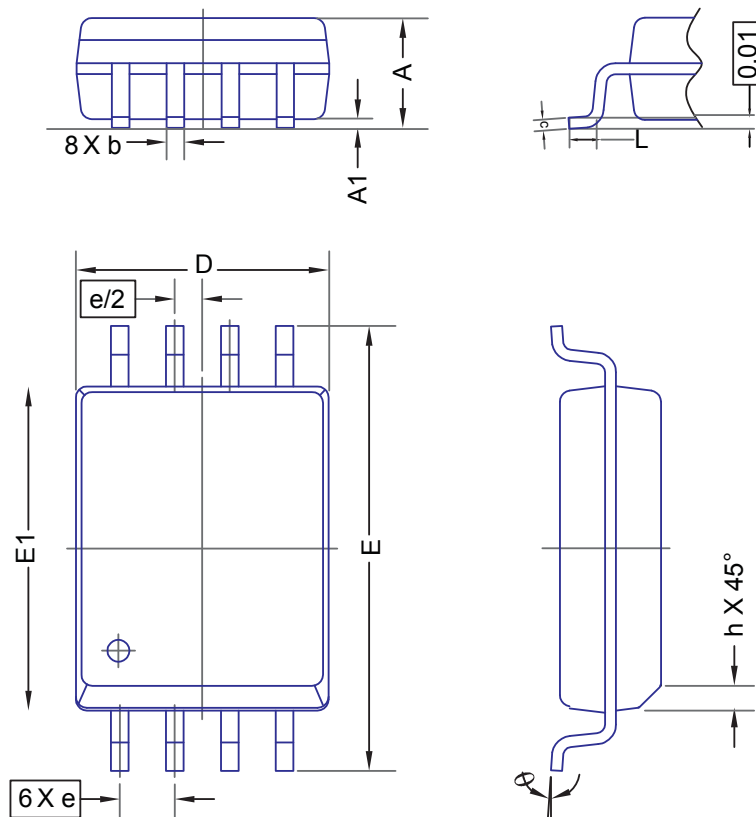
10.2 SO-8W suggested land pattern

Figure 14. SO-8W suggested land pattern
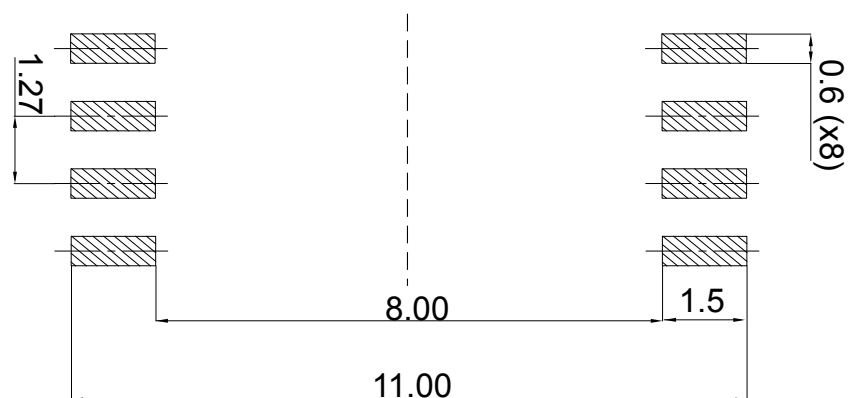
11 Ordering information

Table 10. Device summary

Order code	Output configuration	Package	Package marking	Packaging
STGAP2HSAC	GOUT-CLAMP	SO-8W	GP2HSAC	Tube
STGAP2HSACTR	GOUT-CLAMP	SO-8W	GP2HSAC	Tape and Reel

Revision history

Table 11. Document revision history

Date	Version	Changes
09-Sep-2025	1	Initial release.

Contents

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List of figures

IMPORTANT NOTICE – READ CAREFULLY