STGAP2S

Datasheet

Galvanically isolated 4 A single gate driver

SO-8

Product status link
STGAP2S

Product label
SUSTAINABLE TECHNOLOGY

Features

- High voltage rail up to 1700 V
- Driver current capability: 4 A sink/source @25°C
- 100 V/ns Common Mode Transient Immunity (CMTI)
- Overall input-output propagation delay: 75 ns
- Separate sink and source option for easy gate driving configuration
- 4 A Miller CLAMP dedicated pin option
- UVLO function
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shut-down protection
- Standby function
- Narrow body SO-8 package
- UL 1577 recognized

Application

- Motor driver for home appliances, factory automation, industrial drives and fans.
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

Description

The STGAP2S is a single gate driver which provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for mid and high power applications such as power conversion and motor driver inverters in industrial applications. The device is available in two different configurations. The configuration with separated output pins allows to independently optimize turn-on and turn-off by using dedicated gate resistors. The configuration featuring single output pin and Miller CLAMP function prevents gate spikes during fast commutations in half-bridge topologies. Both configurations provide high flexibility and bill of material reduction for external components.

The device integrates UVLO and thermal shutdown protection functions to facilitate the design of highly reliable systems. Dual input pins allow the selection of signal polarity control and implementation of HW interlocking protection to avoid cross-conduction in case of controller malfunction. The input to output propagation delay is less than 75 ns, which delivers high PWM control accuracy. A standby mode is available to reduce idle power consumption.

1 Block diagram

Figure 1. **Block diagram - separated outputs option**

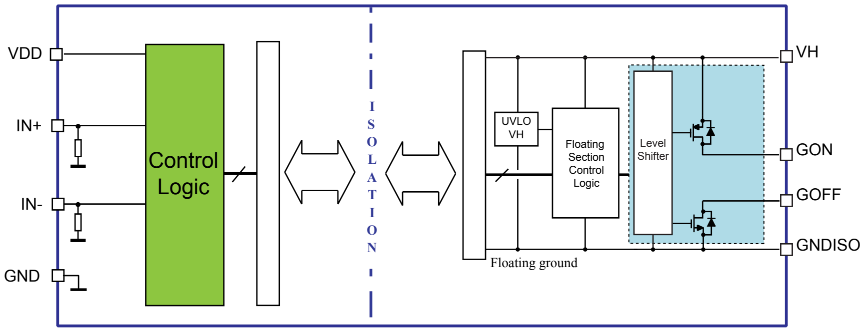
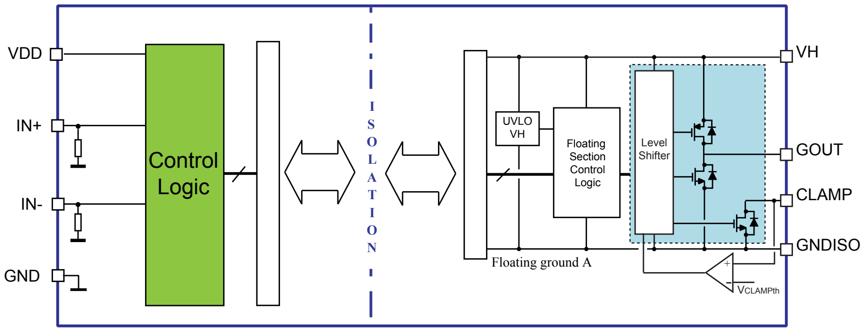


Figure 2. **Block diagram - single output and Miller clamp option**



2 Pin description and connection diagram

Figure 3. Pin connection (top view), separated outputs option

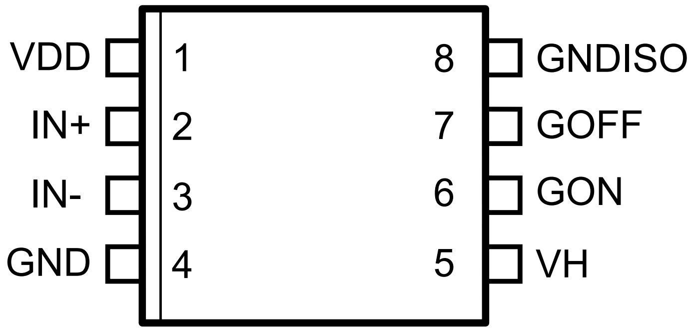


Figure 4. Pin connection (top view), single output and Miller clamp option

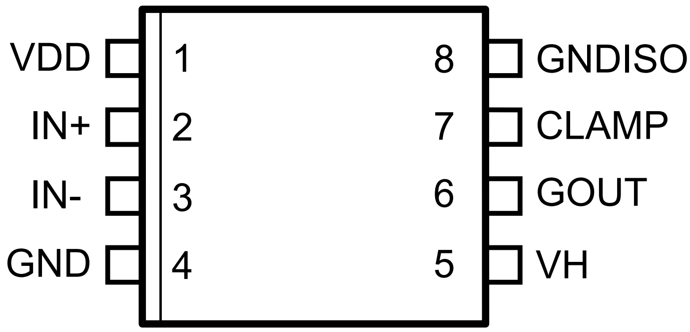


Table 1. Pin description

Pin no.		Pin name	Type	Function
Figure 3	Figure 4			
1	1	VDD	Power supply	Driver logic supply voltage
2	2	IN+	Logic input	Driver logic input, active high
3	3	$\overline{\text{IN-}}$	Logic input	Driver logic input, active low
4	4	GND	Power supply	Driver logic ground
5	5	VH	Power supply	Gate driving positive voltage supply
-	6	GOUT	Analog output	Sink/source output
-	7	CLAMP	Analog output	Active Miller clamp
6	-	GON	Analog output	Source output
7	-	GOFF	Analog output	Sink output
8	8	GNDISO	Power supply	Gate driving Isolated ground

3 Electrical data

3.1 Absolute maximum ratings

Table 2. **Absolute maximum ratings**

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	-0.3	6.5	V
V_{LOGIC}	Logic pins voltage vs. GND	-	-0.3	6.5	V
VH	Positive supply voltage (VH vs. GNDISO)	-	-0.3	28	V
V_{OUT}	Voltage ongate driver outputs (GON, GOFF, CLAMP vs. GNDISO)	-	- 0.3	VH +0.3	V
V_{ISO-OP}	Input to output isolation voltage (GND vs. GNDISO)	DC or peak	-1700	+1700	V
T_J	Junction temperature	-	-40	150	°C
T_{stg}	Storage temperature	-	-50	150	°C
P_{Din}	Power dissipation input chip	T_{amb} = 25 °C	-	21	mW
P_{Dout}	Power dissipation output chip	T_{amb} = 25 °C	-	850	mW
ESD	HBM (human body model)	-	2		kV

3.2 Thermal data

Table 3. **Thermal data**

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-8	123	°C/W

3.3 Recommended operating conditions

Table 4. **Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	3.1	5.5	V
V_{LOGIC}	Logic pins voltage vs. GND	-	0	5.5	V
VH	Positive supply voltage (VH vs. GNDISO)	-	9.6	26	V
F_{SW}	Maximum switching frequency (1)	-	-	1	MHz
t_{OUT}	Output pulse width (GOUT, GON-GOFF)	-	100	-	ns
T_J	Operating junction temperature	-	-40	125	°C
T_{amb}	Operating junction temperature	-	-40	125	°C

1. *Actual limit depends on power dissipation and T_J.*

4 Electrical characteristics

Table 5. Electrical characteristics

(T_J = 25 °C, VH = 15 V, VDD = 5 V, unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	IN+, IN-	Input to output propagation delay ON	-	50	75	90	ns
t_{Doff}	IN+, IN-	Input to output propagation delay OFF	-	50	75	90	ns
t_r	-	Rise time	C_L =4.7 nF, 10% ÷ 90%	-	30	-	ns
t_f	-	Fall time	C_L =4.7 nF, 90% ÷ 10%	-	30	-	ns
PWD	-	Pulse width distortion |tDon -tDoff|	-	-	-	20	ns
$t_{deglitch}$	IN+, IN-	Inputs deglitch filter	-	-	20	40	ns
CMTI [(1)]	-	Common-mode transient immunity, |dV_{ISO}/dt|	V_{CM} = 1500 V, see Figure 13	100	-	-	V/ns
Supply voltage							
VH_{on}	-	VH UVLO turn-on threshold	-	8.6	9.1	9.6	V
VH_{off}	-	VH UVLO turn-off threshold	-	7.9	8.4	8.9	V
VH_{hyst}	-	VH UVLO hysteresis	-	0.60	0.75	0.95	V
I_{QHU}	-	VH undervoltage quiescent supply current	VH = 7 V	-	1.3	1.8	mA
I_{QH}	-	VH quiescent supply current	-	-	1.3	1.8	mA
I_{QHSBY}	-	Standby VH quiescent supply current	Standby mode	-	400	550	µA
SafeClp	-	GOFF active clamp	I_{GOFF} =0.2 A; VH floating	-	2	2.3	V
I_{QDD}	-	VDD quiescent supply current	-	-	1	1.3	mA
I_{QDDSBY}	-	Standby VDD quiescent supply current	Standby mode	-	40	65	µA
Logic inputs							
V_{il}	IN+, IN-	Low level logic threshold voltage	-	0.29 ·VDD	1/3 · VDD	0.37 · VDD	V
V_{ih}	IN+, IN-	High level logic threshold voltage	-	0.62 ·VDD	2/3 · VDD	0.70 · VDD	V
I_{INh}	IN+, IN-	INx logic “1” input bias current	INx = 5 V	33	50	77	µA
I_{INl}	IN+, IN-	INx logic “0” input bias current	INx = GND	-	-	1	µA
R_{pd}	IN+, IN-	Inputs pull-down resistors	INx = 5 V	65	100	150	kΩ
Driver buffer section							
I_{GON}	-	Source short-circuit current	T_J = 25 °C	-	4	-	A
			T_J = -40 ÷ +125 °C[(1)]	3	-	5	
V_{GONH}	-	Source output high level voltage	I_{GON} = 100 mA	VH -0.15	VH -0.125	-	V
R_{GON}	-	Source R_{DS_ON}	I_{GON} = 100 mA	-	1.125	1.5	Ω

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{GOFF}	-	Sink short-circuit current	T_J = 25 °C	-	4	-	A
			T_J = -40 ÷ +125 °C(1)	3	-	5	
V_{GOFFL}	-	Sink output low level voltage	I_{GOFF} = 100 mA	-	96	120	mV
R_{GOFF}	-	Sink R_{DS_ON}	I_{GOFF} = 100 mA	-	0.96	1.2	Ω
Miller Clampfunction (STGAP2SC only)							
$V_{CLAMPth}$	-	CLAMP voltage threshold	V_{CLAMP} vs. GNDISO	1.3	2	2.6	V
I_{CLAMP}	-	CLAMP short-circuit current	V_{CLAMP} = 15 V		-		A
			T_J = 25 °C	-	4	-	
			T_J = -40 ÷ +125 °C(1)	2	-	5	
V_{CLAMP_L}	-	CLAMP low level output voltage	I_{CLAMP} = 100 mA	-	96	115	mV
R_{CLAMP}	-	CLAMP R_{DS_ON}	I_{CLAMP} = 100 mA	-	0.96	1.15	Ω
Overtemperature protection							
T_{SD}	-	Shutdown temperature	-	170	-	-	°C
T_{hys}	-	Temperature hysteresis	-	-	20	-	°C
Standby							
t_{STBY}	-	Standby time	See Section 6.3	200	280	500	µs
t_{WUP}	-	Wake-up time	See Section 6.3	10	20	35	µs
t_{awake}	-	Wake-up delay	See Section 6.3	90	140	200	µs
$t_{stbyfilt}$	-	Standby filter	See Section 6.3	200	280	800	ns

1. *Characterization data, not tested in production.*

5 Isolation

Table 6. Isolation specification

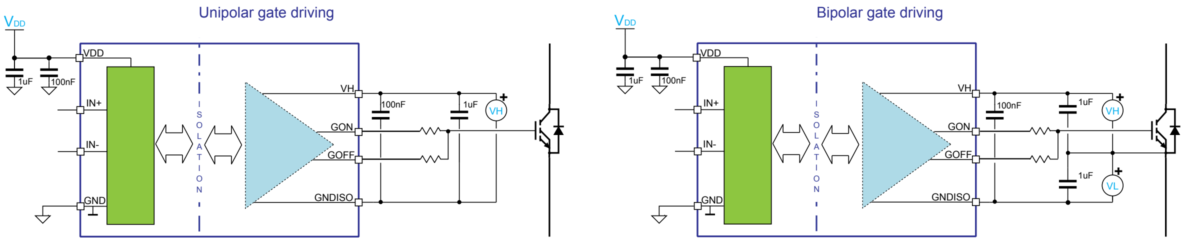
Symbol	Parameter	Test conditions	Value	Unit
General				
CLR	Clearance (Minimum External Air Gap)	Measured from input terminals to output terminals, shortest distance trough air	4	mm
CPG	Creepage (Minimum External Tracking)	Measured from input terminals to output terminals, shortest distance path along body	4	mm
CTI	Comparative Tracking Index (Tracking Resistance)	DIN IEC 112/VDE 0303 Part 1	≥ 400	V
-	Material Group	DIN VDE 0110, 1/89, Table 1	II	-
Isolation characteristics				
V_{PR}	Partial discharge test voltage In accordance with VDE 0884-17	Method a, Type test V_{PR} = 2720, t_m = 10 s Partial discharge < 5 pC	2720	V_{PEAK}
		Method b1, 100 % Production test V_{PR} = 3200, t_m = 1 s Partial discharge < 5 pC	3200	V_{PEAK}
V_{IOTM}	Maximum Transient Isolation Voltage	t_{ini} = 60 s, Type test	4800	V_{PEAK}
V_{IOSM}	Maximum Surge Isolation Voltage	Type test	4800	V_{PEAK}
R_{IO}	Isolation Resistance	V_{IO} = 500 V, Type test	> 10^9	Ω
UL-1577				
V_{ISO}	Isolation Withstand voltage	60 s; Type test	2828/4000	V_{RMS} / V_{PEAK}
$V_{ISO,test}$	Isolation Voltage test	1 s; 100% production	3394/4800	V_{RMS} / V_{PEAK}
Recognized under the UL 1577 Component Recognition Program - file number E362869				

6 Functional description

6.1 Gate driving power supply and UVLO

The STGAP2S is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows implementation of either unipolar or bipolar gate driving.

Figure 5. Power supply configuration for unipolar and bipolar gate driving



Undervoltage protection is available on VH supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH voltage goes below the VH_{off} threshold, the output buffer goes in “safe state”. When VH voltage reaches the VH_{on} threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors, which are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1 µF and 10 µF should be placed close to it.

6.2 Power up, power down and 'safe state'

The following conditions define the “safe state”:

- GOFF = ON state
- GON = high impedance
- CLAMP = ON state (for STGAP2SC)

Such conditions are maintained at power up of the isolated side ($VH < VH_{on}$) and during whole device power down phase ($VH < VH_{off}$), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in *safestate*, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage side the device output state depends on the input pins' status.

6.3 Control inputs

The device is controlled through the IN+ and IN- logic inputs, in accordance to the truth table described in Table 7.

Table 7. Inputs truth table (applicable when device is not in UVLO or “safe state”)

Input pins		Output pins	
IN+	IN-	GON	GOFF
L	L	OFF	ON
H	L	ON	OFF
L	H	OFF	ON
H	H	OFF	ON

Adeglitch filter allow the input pins to ignore signals with duration shorter than $t_{deglitch}$, so preventing noise spikes possibly present in the application from generating unwanted commutations.

6.4 Miller clamp function

The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the C_{GD} capacitance.

During the turn-off period the gate of the external switch is monitored through the CLAMP pin. The CLAMP switch is activated when gate voltage goes below the voltage threshold. $V_{CLAMPth}$, thus creating a low impedance path between the switch gate and the GNDISO pin.

6.5 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced in “safe state” until communication link is properly established again.

6.6 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the TSD temperature threshold, the device is forced in “safe state”. The device operation is restored as soon as the junction temperature is lower than T_{SD} - T_{hys}.

6.7 Standby function

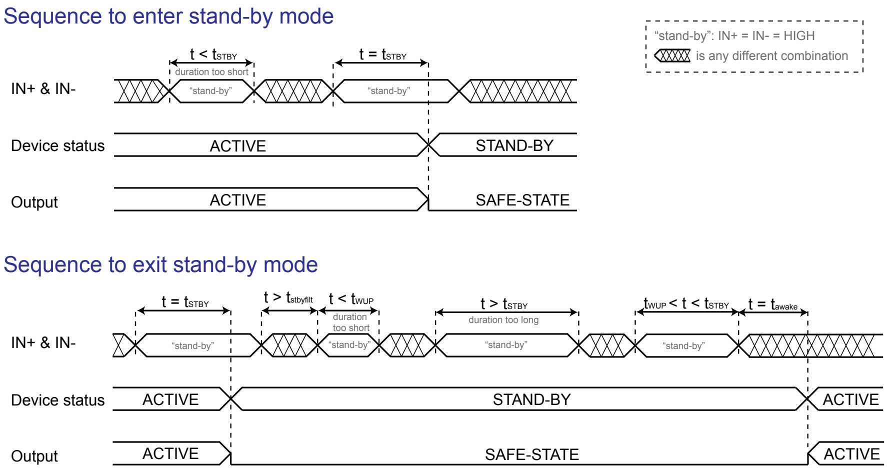
Inorder to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH supply pins is reduced to I_{QDDSBY} and I_{QHSBY} respectively, and the output remains in 'safe state' (the output is actively forced low).

The way to enter standby is to keep both IN+ and IN- high (“standby” value) for a time longer than t_{STBY}. During standby the inputs can change from the “stand-by” value.

To exit stand-by, IN+ and IN- must be put in any combination different from the “standby” value for a time longer than tstbyfilt , and then in the “standby” value for a time t such that t_{WUP}<t < t_{STBY}.

When the input configuration is changed from the “standby” value the output is enabled and set according to inputs state after a time t_{awake}.

Figure 6. Standby state sequences



7 Typical application diagram

Figure 7. Typical application diagram - separated outputs

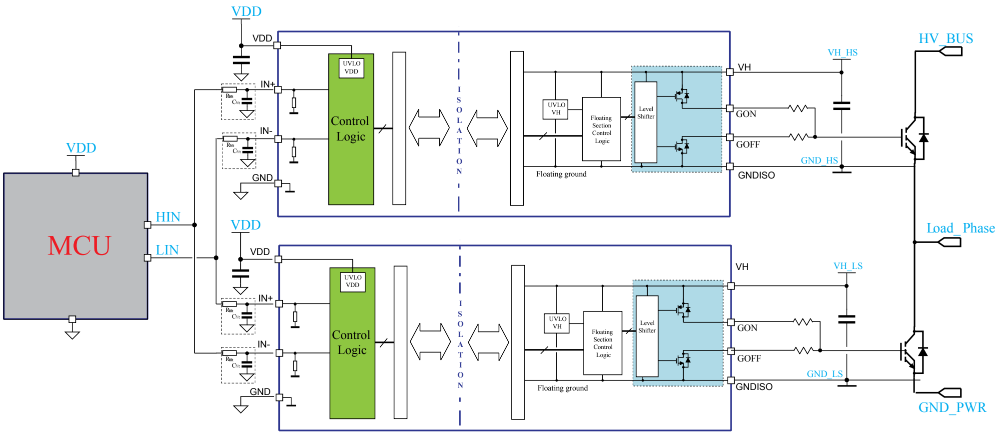


Figure 8. Typical application diagram - separated outputs and negative gate driving

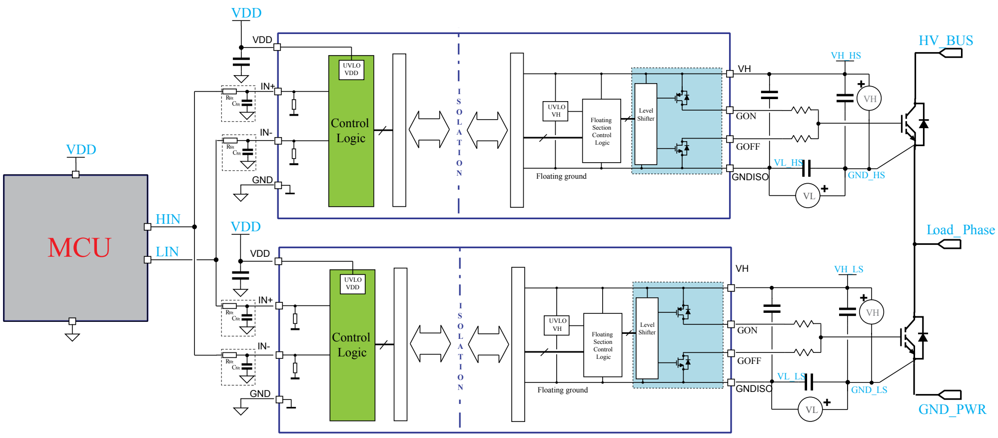


Figure 9. Typical application diagram - Miller clamp

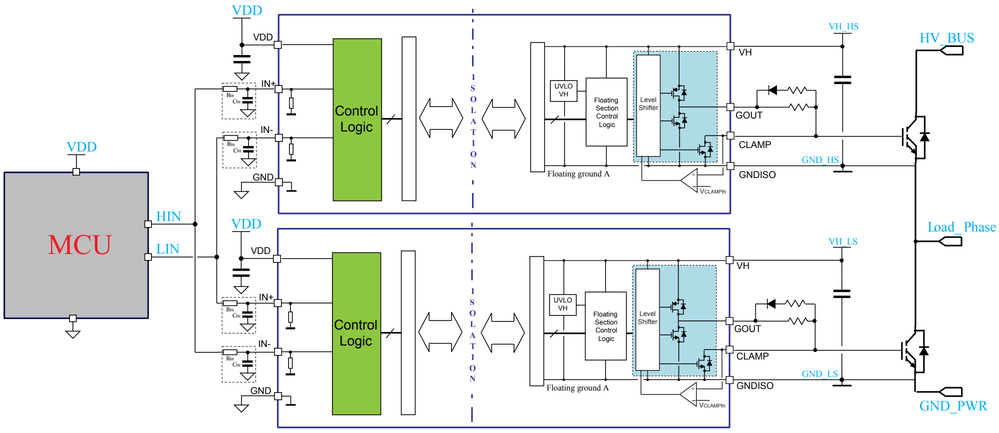
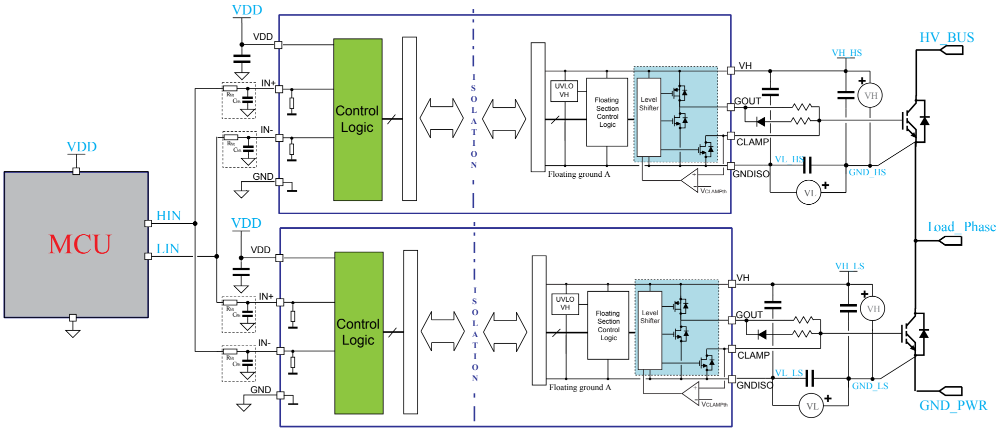


Figure 10. Typical application diagram - Miller clamp and negative gate driving



8 Layout

8.1 Layout guidelines and considerations

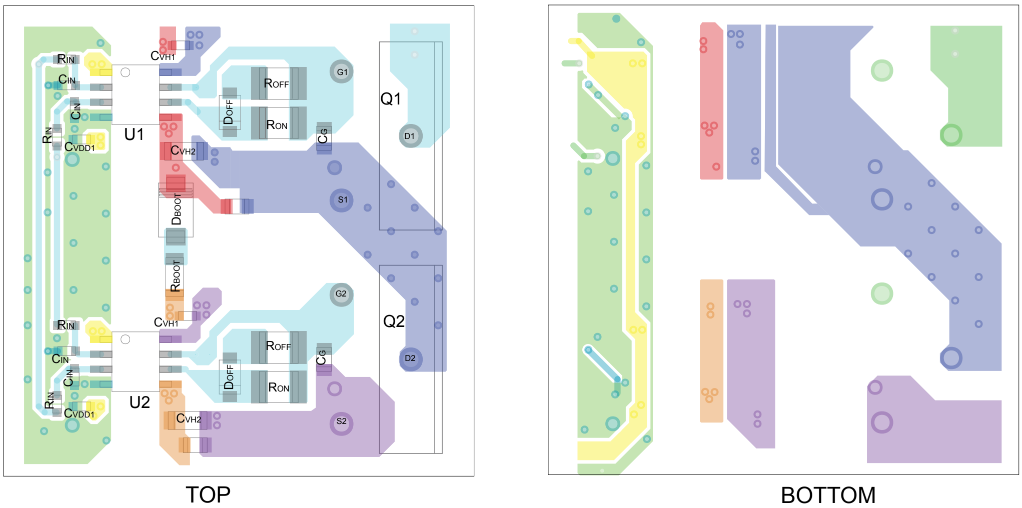
Inorder to optimize the PCB layout, following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pins. A 100 nF capacitor must be placed between VDD and GND and between VH and GNDISO, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current a second capacitor with value in the range between 1 µF and 10 µF should also be placed close to the supply pins.
- As a good practice it is suggested to add filtering capacitors close to logic inputs of the device (IN+, IN-), in particular for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver, so to minimize the gate loop area and inductance that might bring to noise or ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

Anexample of STGAP2SC Half-Bridge PCB layout with main signals highlighted by different colors is shown in Figure 11 . It is recommended to follow this example for proper positioning and connection of filtering capacitors.

Figure 11. Layer traces and copper



9 Testing and characterization information

Figure 12. Timings definition

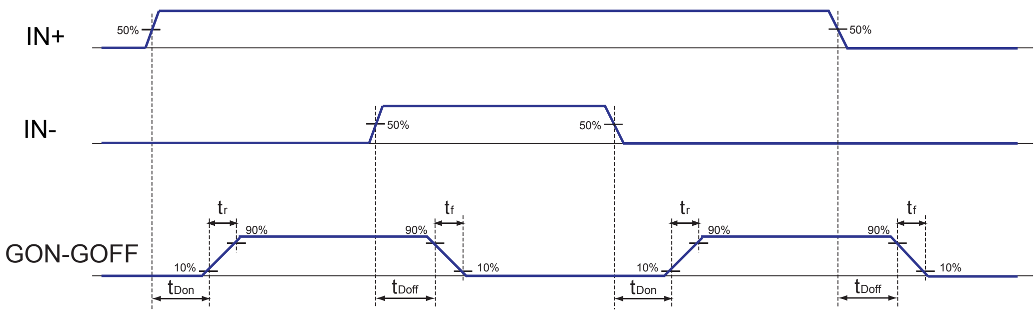
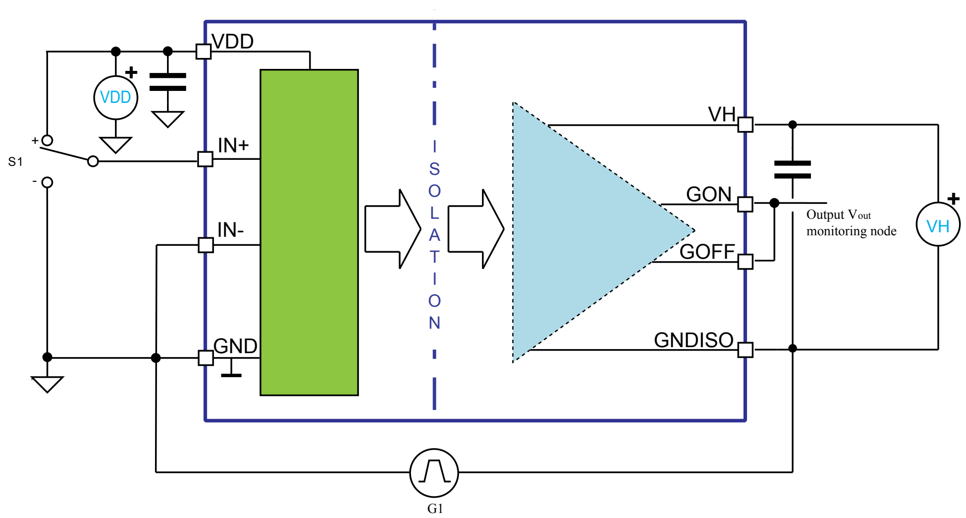


Figure 13. CMTI test circuit



10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO-8 package information

Figure 14. SO-8 package outline

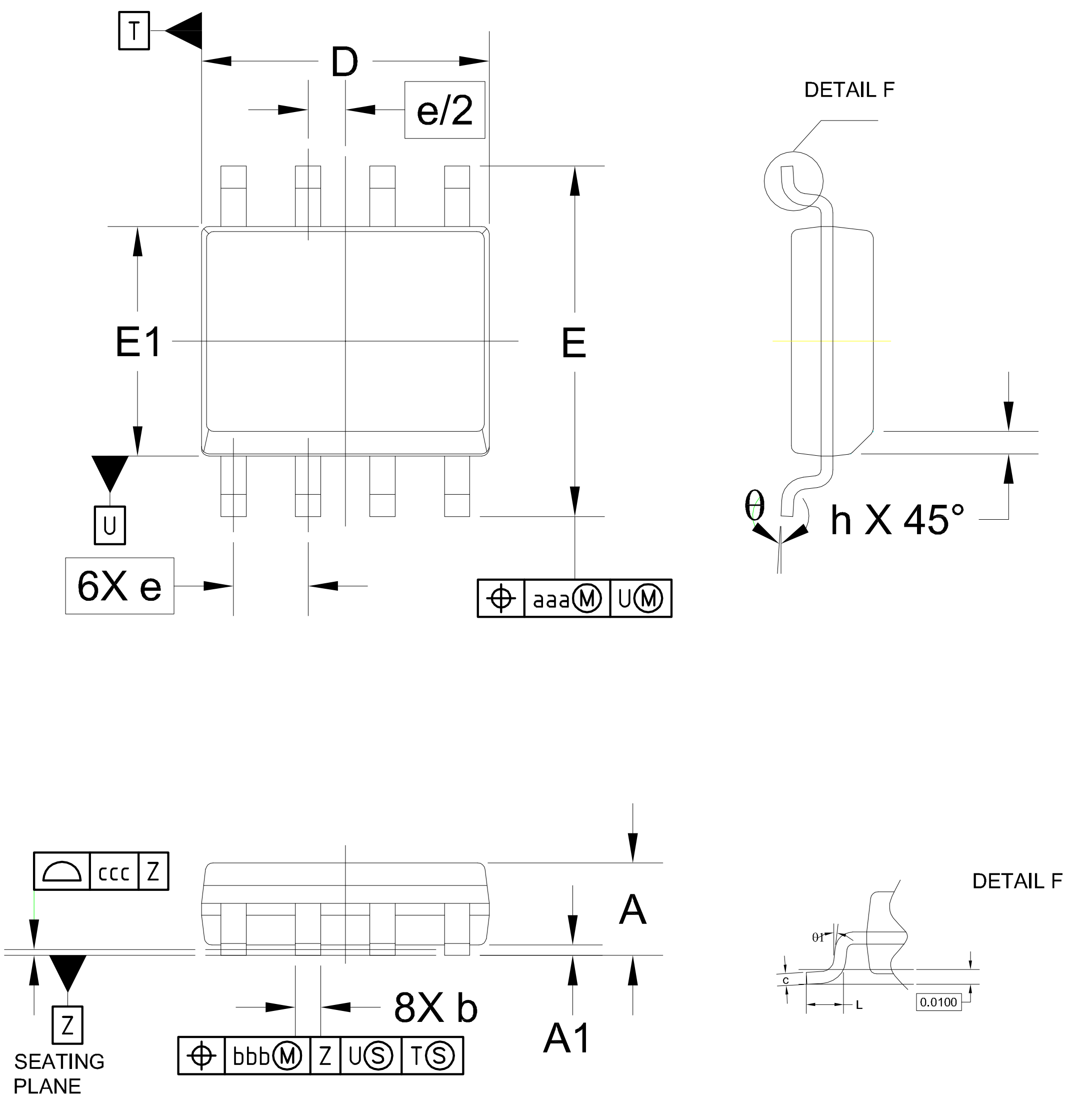


Table 8. SO-8 package mechanical data

Dim.	mm			Notes
	Min.	Typ.	Max.	
A	1.35		1.75	
A1	0.1		0.25	
b	0.35		0.49	
c	0.19		0.25	
D	4.8		5	
E1	3.8	3.9	4	
E	5.8	6	6.2	
e	1.27 BSC			
L	0.4		1.25	
h	0.25		0.5	
ϴ	0		7	
ϴ1	2		12	
aaa		0.25		
bbb		0.25		
ccc		0.1		

11 Suggested land pattern

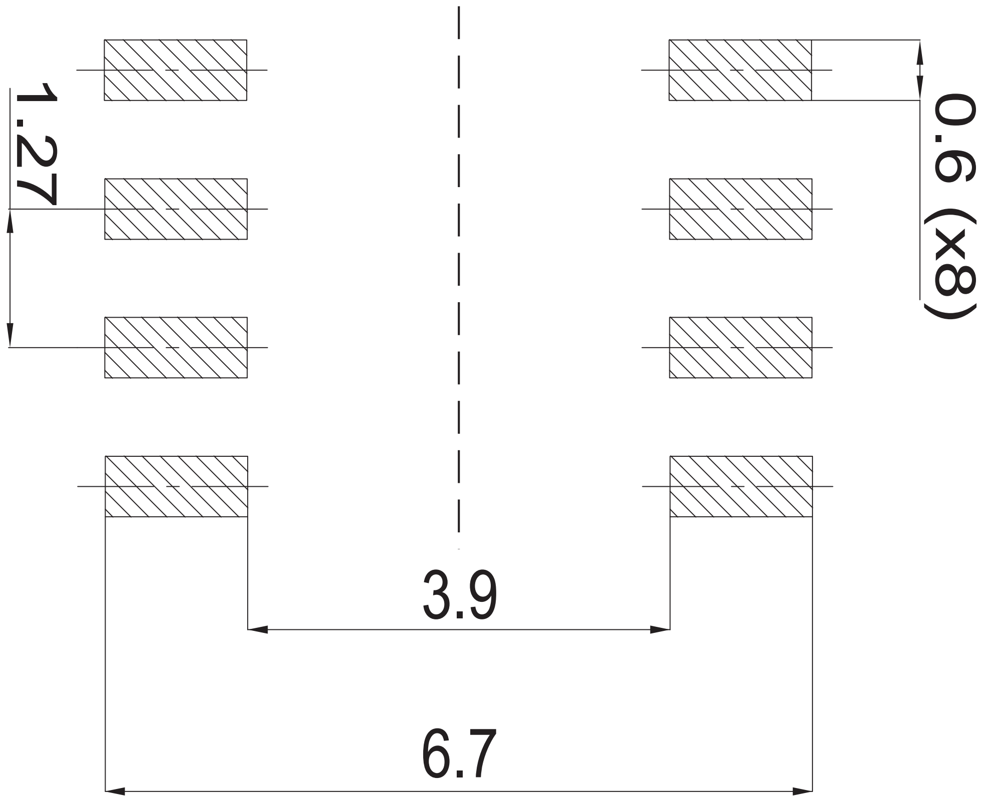


Figure 15. SO-8 suggested land pattern

12 Ordering information

Table 9. Device summary

Order code	Output configuration	Package marking	Package	Packaging
STGAP2SM	GON-GOFF	GAP2S2	SO-8	Tube
STGAP2SMTR	GON-GOFF	GAP2S2	SO-8	Tape and reel
STGAP2SCM	GOUT-CLAMP	GAP2SC2	SO-8	Tube
STGAP2SCMTR	GOUT-CLAMP	GAP2SC2	SO-8	Tape and reel

Revision history

Table 10. **Document revision history**

Date	Version	Changes
06-Jun-2018	1	Initial release.
16-Jul-2021	2	Updated Table 4, Table 5, Table 8 and Section 8. Added *Table 6, Table 7 and Table 8*.
25-Jul-2022	3	Updated Section 3.1, added UL file certification.
17-Mar-2025	4	Updated Section Features, Table 2 (T_{stg} and T_{amb} symbol), Table 4 (added T_{amb}), and Section 5: Isolation (new table format). Added Note in Section 10.1.
27-Mar-2025	5	Removed Note in Section 10.1, and update Figure 14.

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