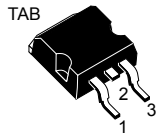
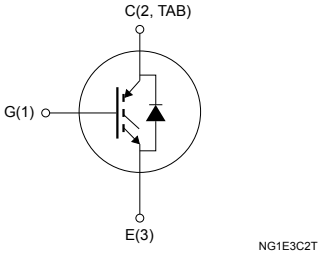
STGB20H65DFB2

Datasheet

Trench gate field-stop, 650 V, 20 A, high-speed HB2 series IGBT in a D²PAK package



D²PAK



Features

- Maximum junction temperature: T_J = 175 °C
- Low $V_{CE(sat)}$ = 1.65 V (typ.) @ I_C = 20 A
- Very fast and soft recovery co-packaged diode
- Minimized tail current
- Tight parameter distribution
- Low thermal resistance
- Positive $V_{CE(sat)}$ temperature coefficient

Applications

- Welding
- PFC converters - single phase input
- Solar inverters (string and central)
- Uninterruptable power supplies (UPS)
- EV charging - DC fast charging stations

Description

The newest IGBT 650 V HB2 series represents an evolution of the advanced proprietary trench gate field-stop structure. The performance of the HB2 series is optimized in terms of conduction, thanks to a better $V_{CE(sat)}$ behavior at low current values, as well as in terms of reduced switching energy. A very fast soft recovery diode is co-packaged in antiparallel with the IGBT. The result is a product specifically designed to maximize efficiency for a wide range of fast applications.

Product status link
STGB20H65DFB2

Product summary	
Order code	STGB20H65DFB2
Marking	G20H65DFB2
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	650	V
I_C	Continuous collector current at T_C = 25 °C	40	A
	Continuous collector current at T_C = 100 °C	25	A
I_{CP}(1)(2)	Pulsed collector current	60	A
V_{GE}	Gate-emitter voltage	±20	V
	Transient gate-emitter voltage ($t_p \leq 10$ µs)	±30	
I_F	Continuous forward current at T_C = 25 °C	40	A
	Continuous forward current at T_C = 100 °C	23	
I_{FP}(1)(2)	Pulsed forward current	60	A
P_{TOT}	Total power dissipation at T_C = 25 °C	147	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	°C

1. *Pulse width is limited by maximum junction temperature.*
2. *Defined by design, not subject to production test.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case IGBT	1.02	°C/W
	Thermal resistance junction-case diode	1.47	
R_{thJA}	Thermal resistance junction-ambient	62.5	

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V, I_C = 1 mA	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 20 A		1.65	2.1	V
		V_{GE} = 15 V, I_C = 20 A, T_J = 125 °C		1.95		
		V_{GE} = 15 V, I_C = 20 A, T_J = 175 °C		2.1		
V_F	Forward on-voltage	I_F = 20 A		1.65	2.55	V
		I_F = 20 A, T_J = 125 °C		1.4		
		I_F = 20 A, T_J = 175 °C		1.3		
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 650 V			25	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±250	nA

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	1010	-	pF
C_{oes}	Output capacitance		-	81	-	
C_{res}	Reverse transfer capacitance		-	26	-	
Q_g	Total gate charge	V_{CC} = 520 V, I_C = 20 A, V_{GE} = 0 to 15 V (see Figure 28. Gate charge test circuit)	-	56	-	nC
Q_{ge}	Gate-emitter charge		-	9.4	-	
Q_{gc}	Gate-collector charge		-	27.8	-	

Table 5. Switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, I_C = 20 A, V_{GE} = 15 V, R_G = 10 Ω (see Figure 27. Test circuit for inductive load switching)	-	16	-	ns
t_r	Current rise time		-	8	-	ns
E_{on} (1)	Turn-on switching energy		-	265	-	µJ
$t_{d(off)}$	Turn-off delay time		-	78.8	-	ns
t_f	Current fall time		-	35	-	ns
E_{off} (2)	Turn-off switching energy		-	214	-	µJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, I_C = 20 A, V_{GE} = 15 V, R_G = 10 Ω, T_J = 175 °C (see Figure 27. Test circuit for inductive load switching)	-	17	-	ns
t_r	Current rise time		-	9	-	ns
E_{on} (1)	Turn-on switching energy		-	556	-	µJ
$t_{d(off)}$	Turn-off delay time		-	98	-	ns
t_f	Current fall time		-	80	-	ns
E_{off} (2)	Turn-off switching energy		-	378	-	µJ

1. *Including the reverse recovery of the diode.*
2. *Including the tail of the collector current.*

Table 6. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_F = 20 A, V_R = 400 V, V_{GE} = 15 V, di/dt = 1000 A/µs (see Figure 30. Diode reverse recovery waveform)	-	215	-	ns
Q_{rr}	Reverse recovery charge		-	970	-	nC
I_{rrm}	Reverse recovery current		-	17	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	303	-	A/µs
E_{rr}	Reverse recovery energy		-	293	-	µJ
t_{rr}	Reverse recovery time	I_F = 20 A, V_R = 400 V, V_{GE} = 15 V, di/dt = 1000 A/µs, T_J = 175 °C (see Figure 30. Diode reverse recovery waveform)	-	330	-	ns
Q_{rr}	Reverse recovery charge		-	2772	-	nC
I_{rrm}	Reverse recovery current		-	30	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	244	-	A/µs
E_{rr}	Reverse recovery energy		-	866	-	µJ

2.1 Electrical characteristics (curves)

Figure 1. Power dissipation vs case temperature

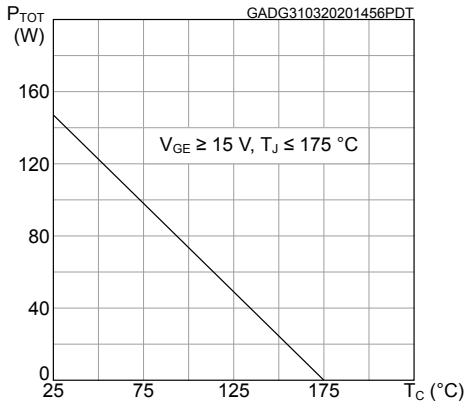


Figure 2. Collector current vs case temperature

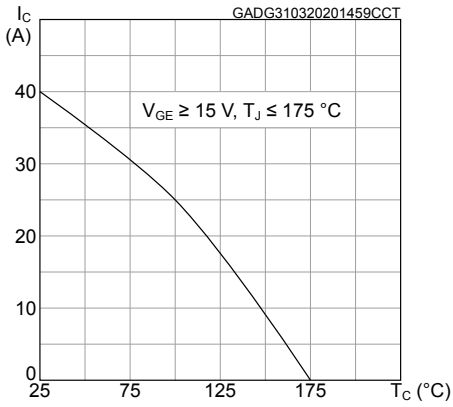


Figure 3. Output characteristics (T_J = 25 °C)

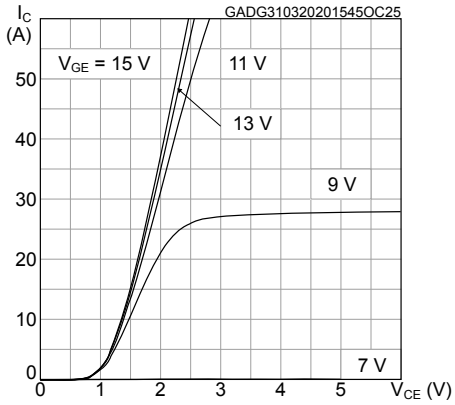


Figure 4. Output characteristics (T_J = 175 °C)

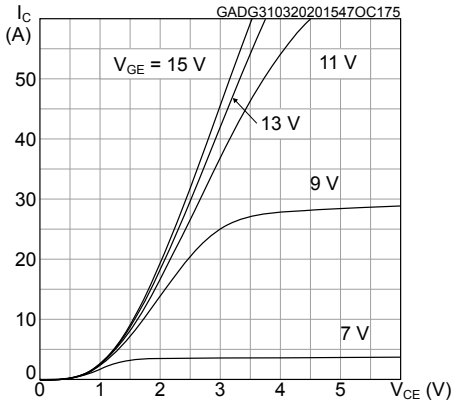


Figure 5. $V_{CE(sat)}$ vs junction temperature

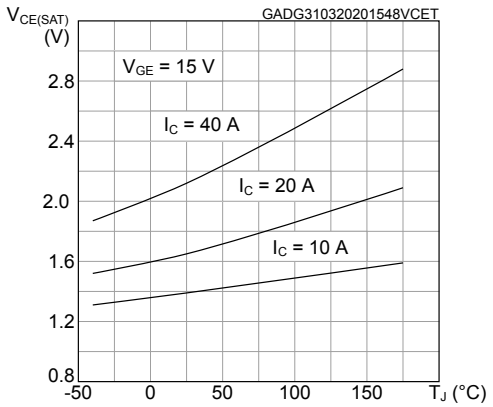


Figure 6. $V_{CE(sat)}$ vs collector current

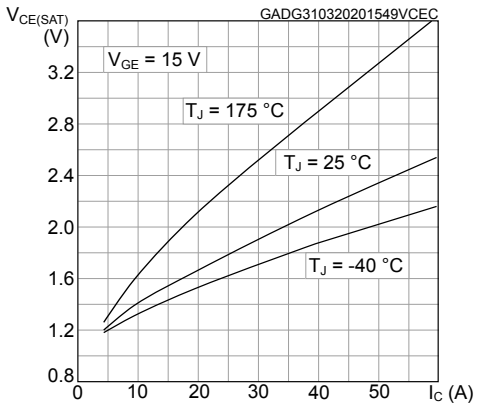


Figure 7. Forward bias safe operating area

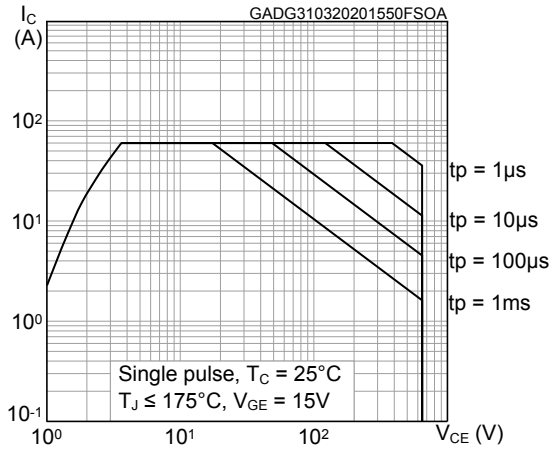


Figure 8. Collector current vs switching frequency

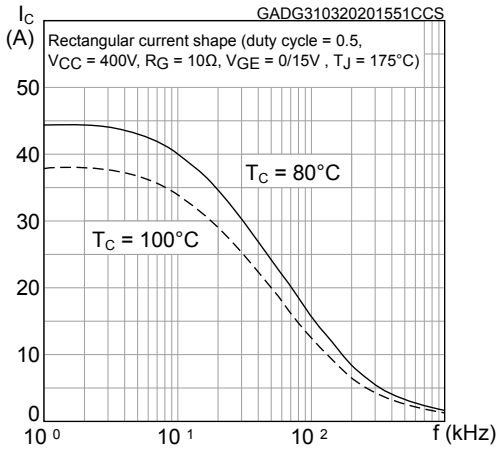


Figure 9. Transfer characteristics

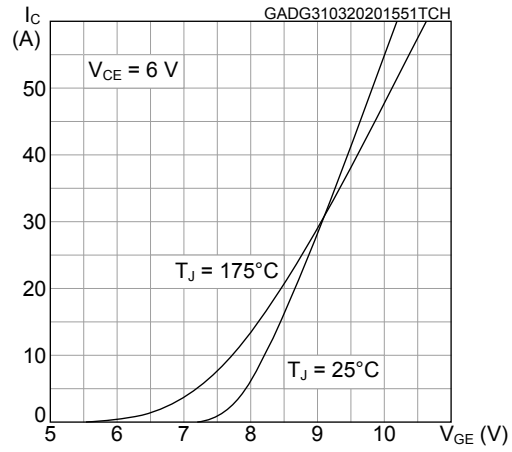


Figure 10. Diode V_F vs forward current

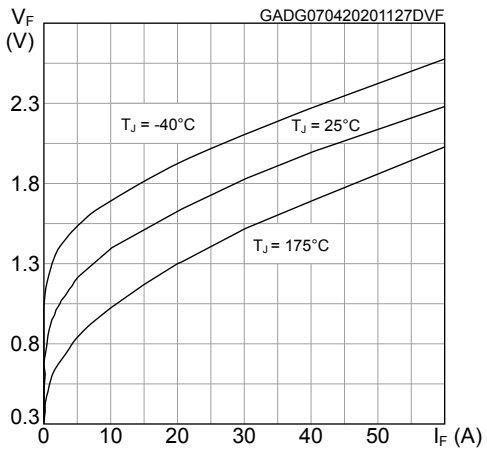


Figure 11. Normalized $V_{GE(th)}$ vs junction temperature

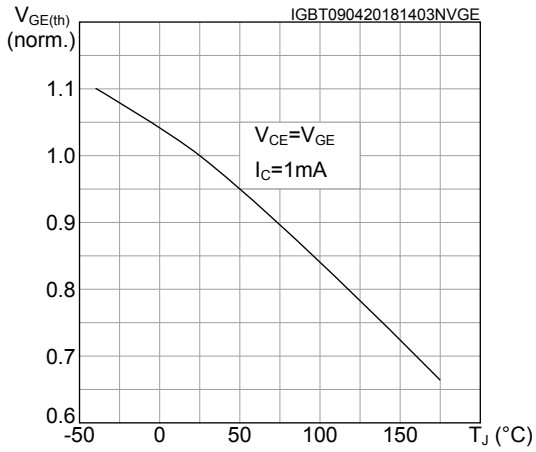


Figure 12. Normalized $V_{(BR)CES}$ vs junction temperature

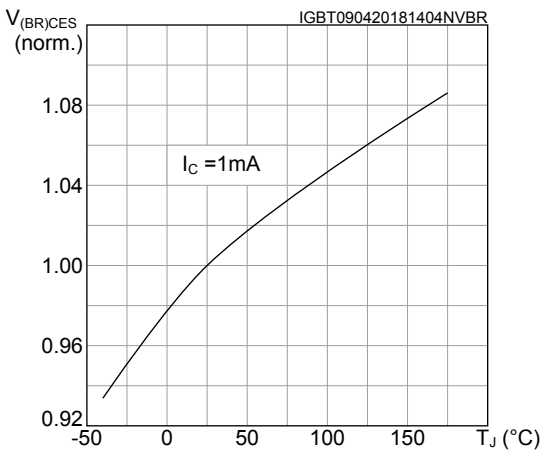


Figure 13. Capacitance variations

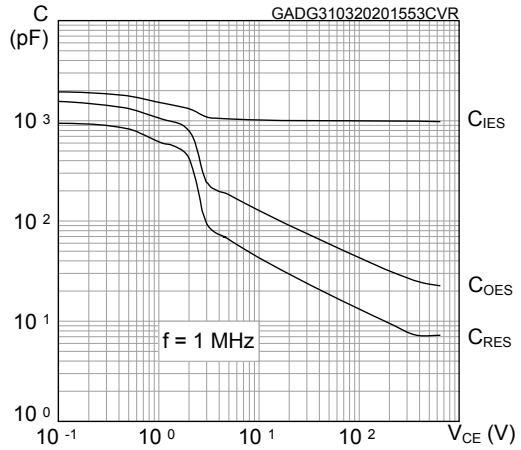


Figure 14. Gate charge vs gate-emitter voltage

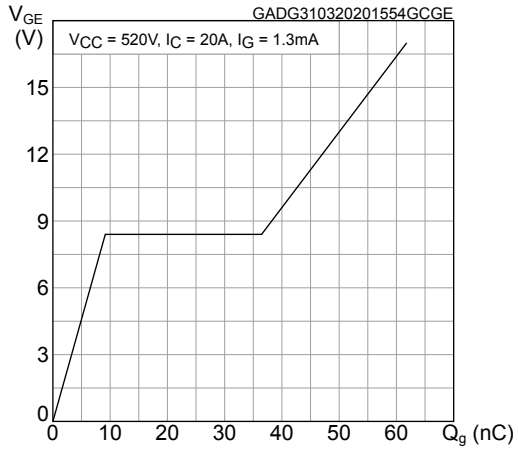


Figure 15. Switching energy vs collector current

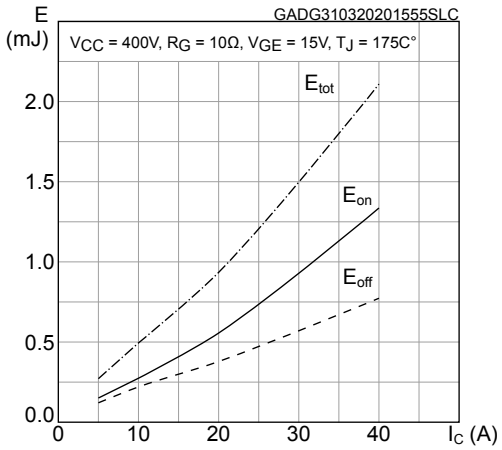


Figure 16. Switching energy vs temperature

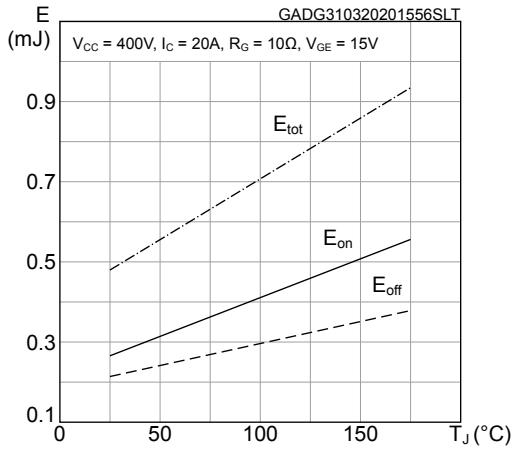


Figure 17. Switching energy vs collector emitter voltage

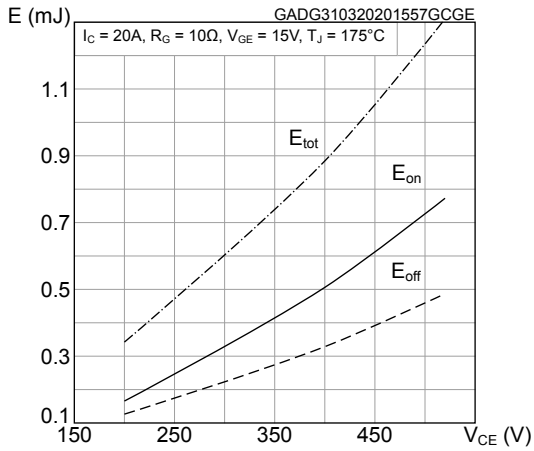


Figure 18. Switching energy vs gate resistance

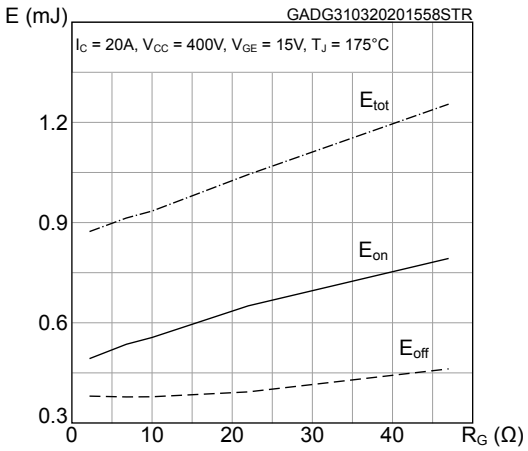


Figure 19. Switching times vs collector current

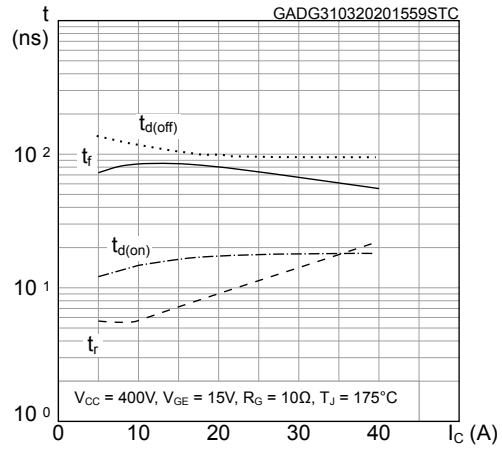


Figure 20. Switching times vs gate resistance

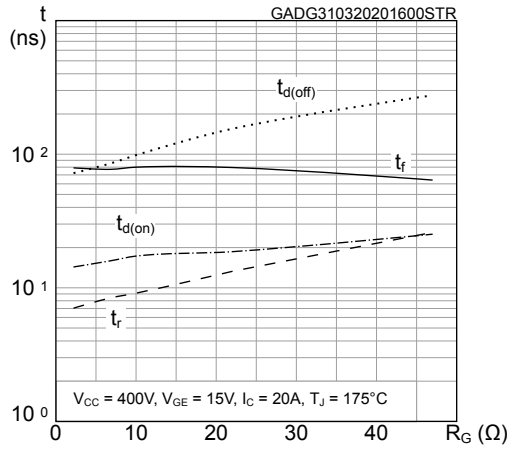


Figure 21. Reverse recovery current vs diode current slope

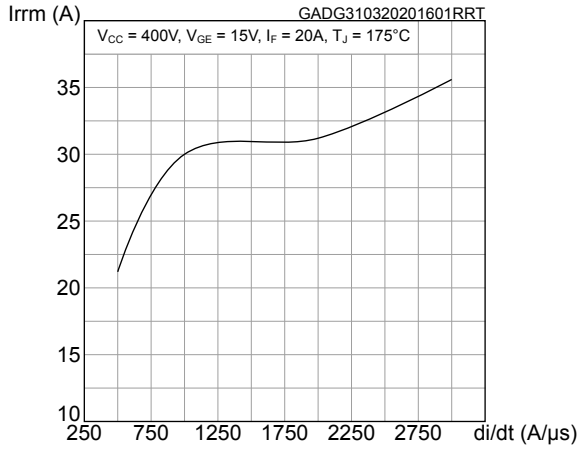


Figure 22. Reverse recovery time vs diode current slope

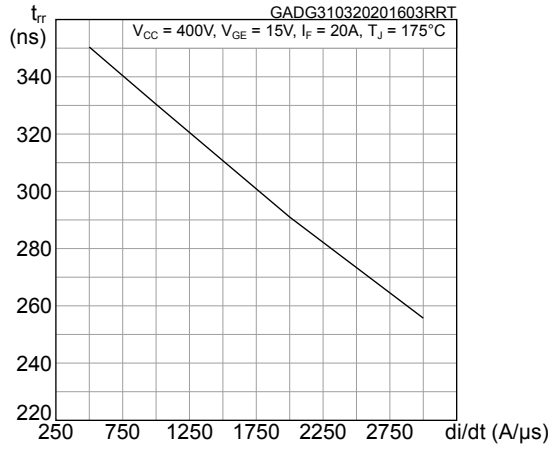


Figure 23. Reverse recovery charge vs diode current slope

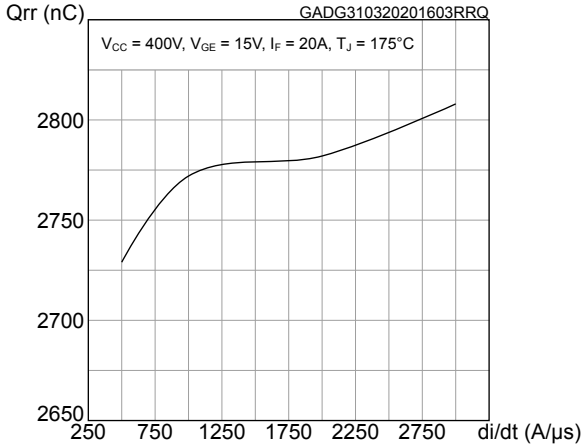


Figure 24. Reverse recovery energy vs diode current slope

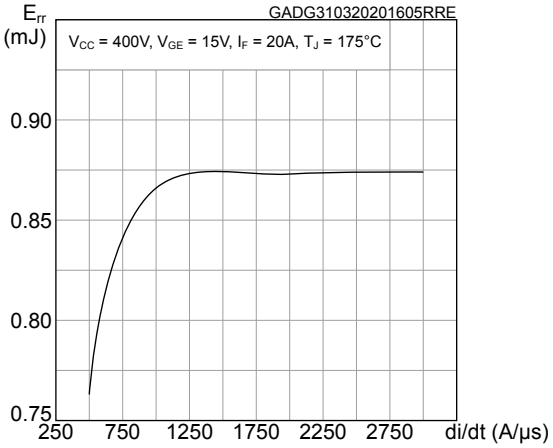


Figure 25. Thermal impedance for IGBT

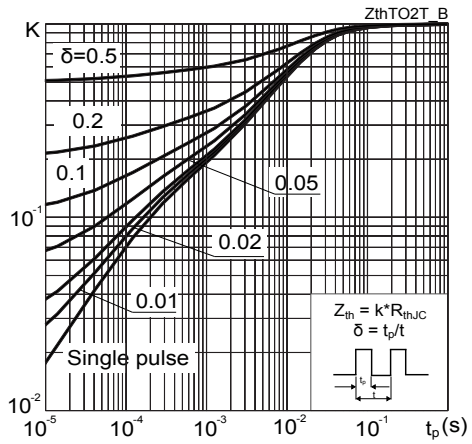
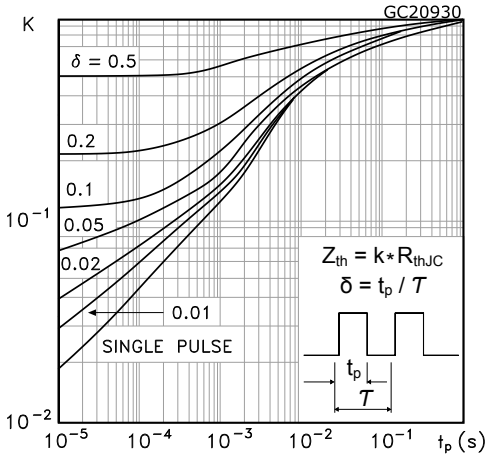


Figure 26. Thermal impedance for diode



3 Test circuits

Figure 27. Test circuit for inductive load switching

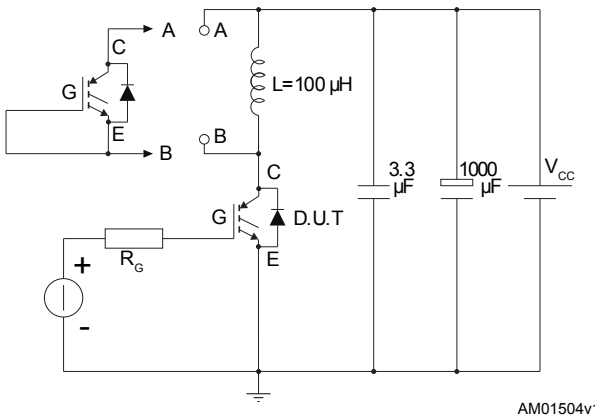


Figure 28. Gate charge test circuit

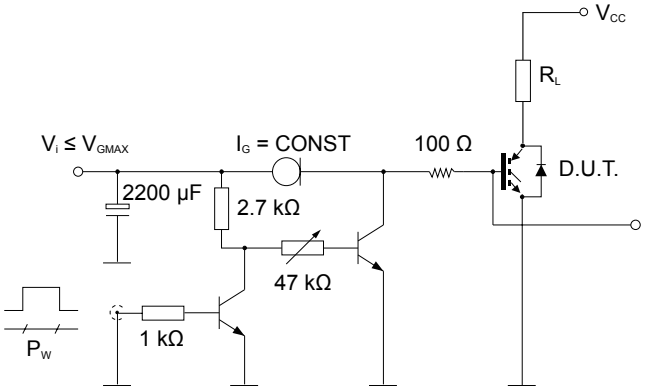


Figure 29. Switching waveform

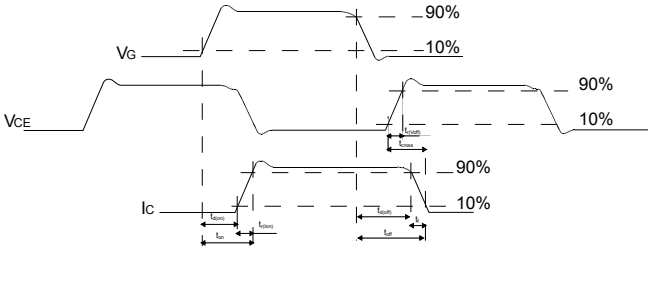
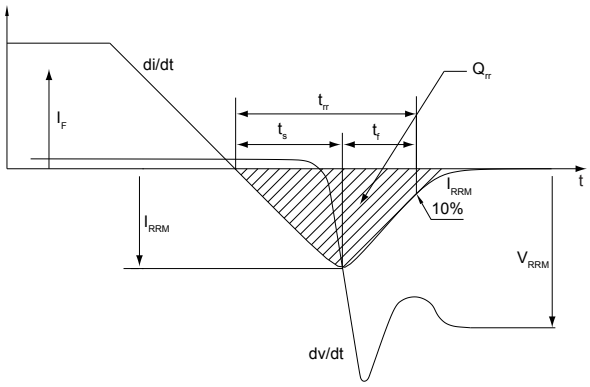


Figure 30. Diode reverse recovery waveform

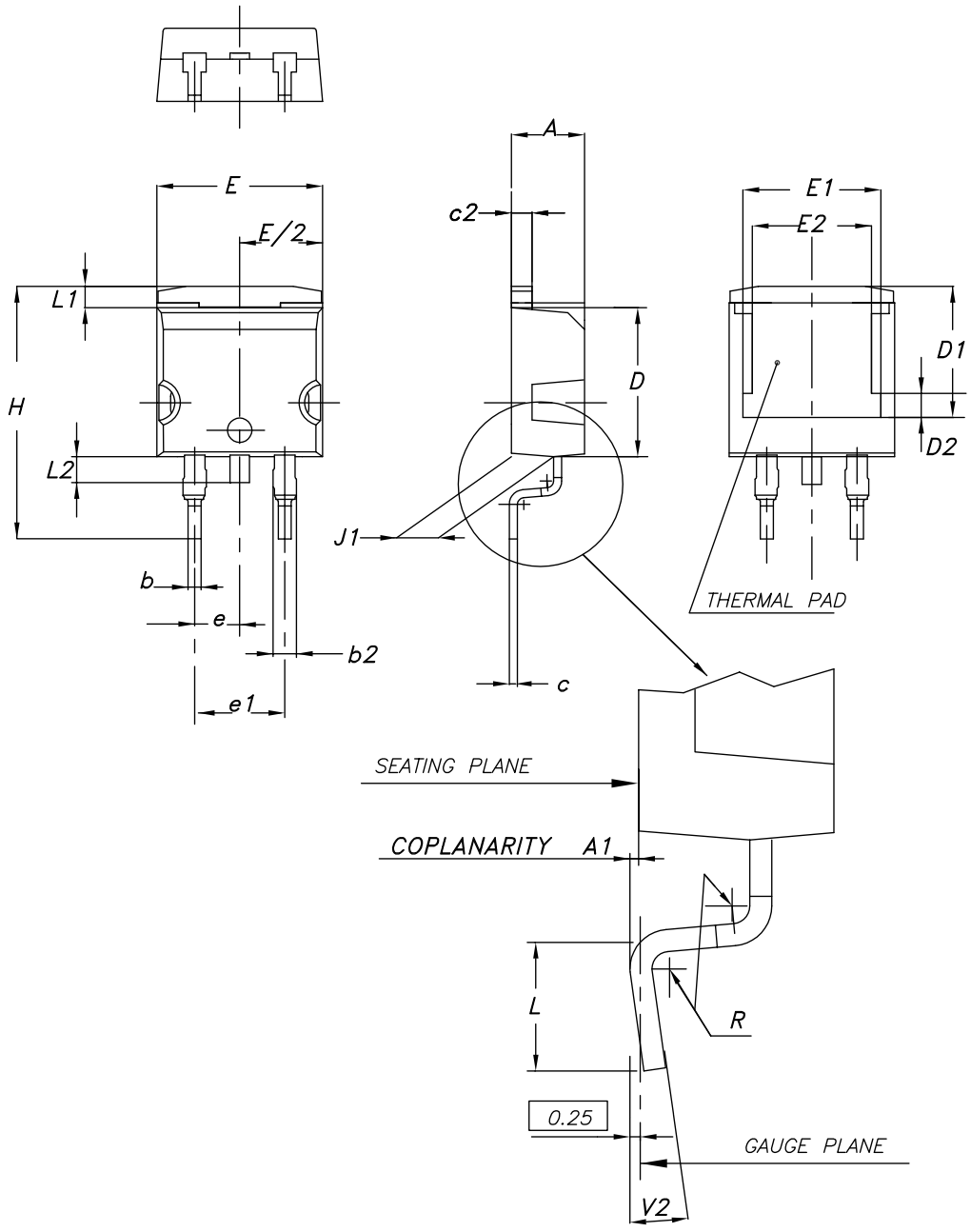


4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 31. **D²PAK (TO-263) type A2 package outline**

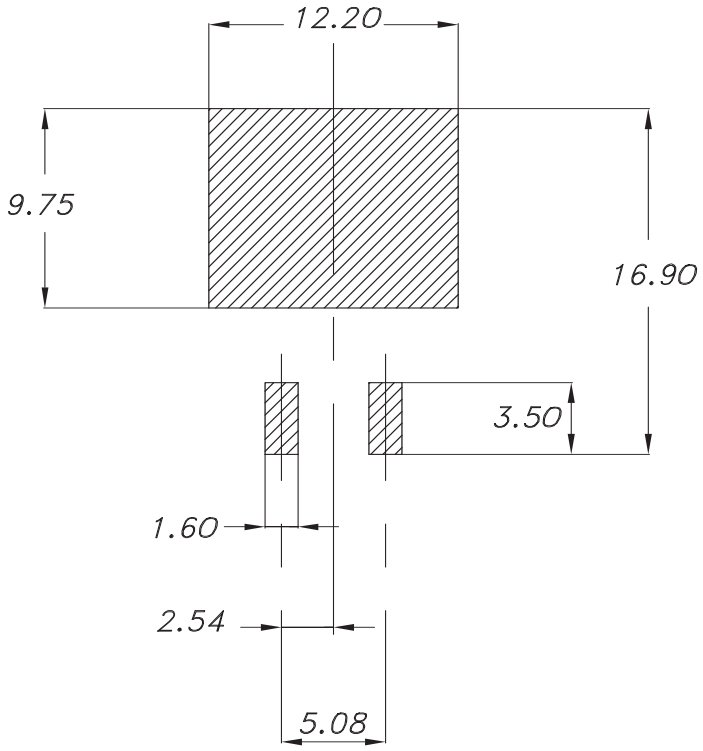


0079457_A2_27

Table 7. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

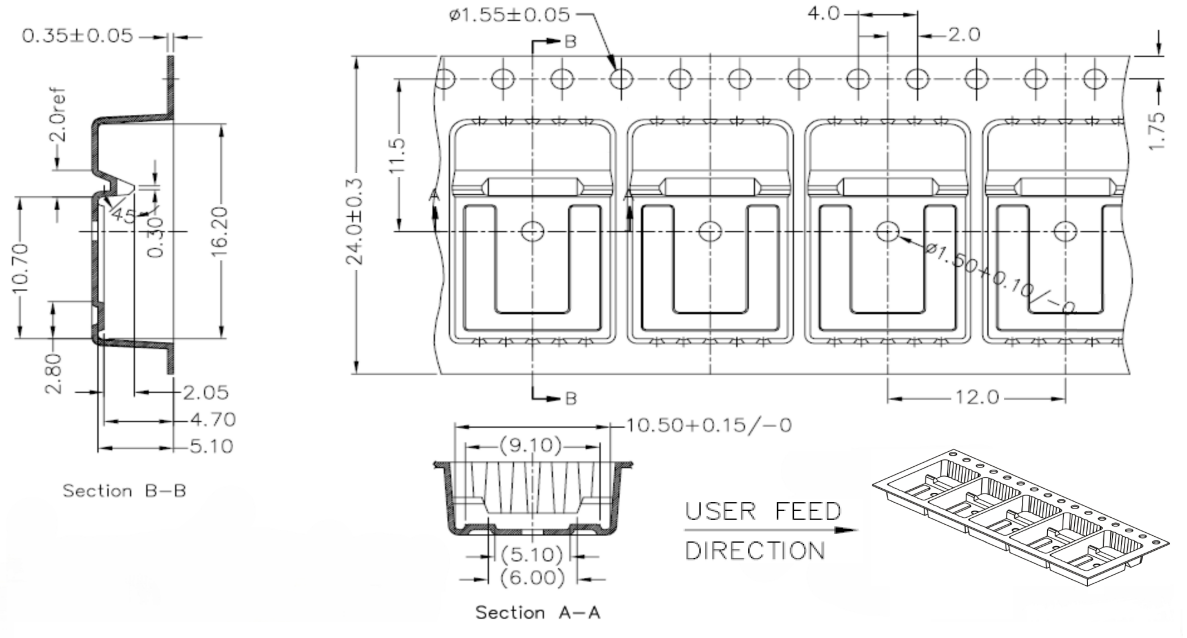
Figure 32. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 33. D²PAK tape drawing



DM01095771_1

Revision history

Table 8. **Document revision history**

Date	Version	Changes
05-May-2020	1	First release.
17-Apr-2025	2	Updated Section 4: Package information.

Contents