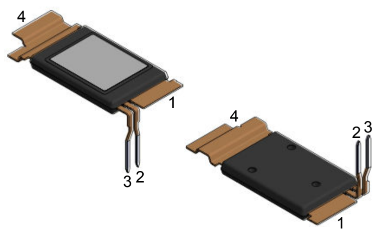
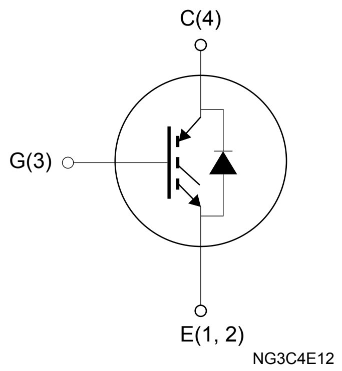
STGST200G65DFAG, STGST200G65DTAG

Datasheet

Automotive-grade trench gate field-stop IGBT 650 V, 200 A in a STPAK package



STPAK



Features

- AEC-Q101 qualified
- $V_{CE(sat)}$ = 1.52 V (typ.) @ I_C = 200 A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Low thermal resistance
- Very fast and soft recovery antiparallel diode

Applications

- Main inverter (electric traction)

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. This device represents an optimum compromise in performance to maximize the efficiency of inverter systems where low-loss are essential. Furthermore, a positive $V_{CE(sat)}$ temperature coefficient and tight parameter distribution result in safer paralleling operation.

Product status link
STGST200G65DFAG
STGST200G65DTAG

Product summary	
Order code	**STGST200G65DFAG**
Marking	G200G65DFAG
Package	STPAK longer pins
Packing	Tray
Order code	**STGST200G65DTAG**
Marking	G200G65DTAG
Package	STPAK longer pins
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	650	V
I_C (1)	Continuous collector current at T_C = 25 °C	365	A
	Continuous collector current at T_C = 100 °C	228	
I_{CP} (1)	Pulsed collector current (t_p ≤ 1 µs)	800	A
V_{GE}	Gate-emitter voltage	±20	V
I_F (1)	Continuous forward current at T_C = 25 °C	238	A
	Continuous forward current at T_C = 100 °C	145	
P_{TOT}	Total power dissipation at T_C = 25 °C	1000	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	°C

1. *Limited by maximum junction temperature.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case, IGBT	0.15	°C/W
	Thermal resistance, junction-to-case, diode	0.29	

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V, I_C = 1 mA	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C= 200 A		1.52	1.80	V
		V_{GE} = 15 V, I_C = 200 A, T_J = 175 °C		1.75		
V_F	Forward on-voltage	I_F = 150 A		1.85	2.32	V
		I_F = 150 A, T_J = 175 °C		1.47		
		I_F = 200 A		2.00	2.57	
		I_F = 200 A, T_J = 175 °C		1.65		
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 2 mA	4.75	5.50	6.25	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 650 V,			10	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V			50	nA
		V_{CE} = 0 V, V_{GE} = -20 V	-50			

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	14.3	-	nF
C_{oes}	Output capacitance		-	0.7	-	nF
C_{res}	Reverse transfer capacitance		-	0.4	-	nF
Q_g	Total gate charge	V_{CC} = 400 V, I_C = 200 A, V_{GE} =18 V (see Figure 28. Gate charge test circuit)	-	900	-	nC

Table 5. IGBT switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, V_{GE} = -5 to +18 V, R_G = 4.7 Ω, I_C = 200 A (see Figure 27. Test circuit for inductive load switching)	-	68.5	-	ns
t_r	Current rise time		-	41		ns
E_{on}(1)	Turn-on switching energy		-	1.41	-	mJ
$t_{d(off)}$	Turn-off delay time		-	362	-	ns
t_f	Current fall time		-	48	-	ns
E_{off}(2)	Turn-off switching energy		-	4.77	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, V_{GE} = -5 to +18 V, R_G = 4.7 Ω, I_C = 200 A, T_J = 175 °C (see Figure 27. Test circuit for inductive load switching)	-	68	-	ns
t_r	Current rise time		-	44	-	ns
E_{on}(1)	Turn-on switching energy		-	2.53	-	mJ
$t_{d(off)}$	Turn-off delay time		-	400	-	ns
t_f	Current fall time		-	96	-	ns
E_{off}(2)	Turn-off switching energy		-	7.46	-	mJ

1. *Including the reverse recovery of the diode.*
2. *Including the tail of the collector current.*

Table 6. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{rm}	Reverse recovery current	V_{CC} = 400 V, V_{GE} = -5 to +18 V, R_G = 4.7 Ω, di/dt = 4318 A/μs, I_C = 200 A (see Figure 27. Test circuit for inductive load switching)	-	101	-	A
t_{rr}	Reverse recovery time		-	164	-	ns
Q_{rr}	Reverse recovery charge		-	6.3	-	μC
E_{rr}	Reverse recovery energy		-	2	-	mJ
I_{rm}	Reverse recovery current	V_{CC} = 400 V, V_{GE} = -5 to +18 V, R_G = 4.7 Ω, di/dt = 4513 A/μs, I_C = 200 A, T_J = 175 °C (see Figure 27. Test circuit for inductive load switching)	-	198	-	A
t_{rr}	Reverse recovery time		-	300	-	ns
Q_{rr}	Reverse recovery charge		-	22	-	μC
E_{rr}	Reverse recovery energy		-	7.1	-	mJ

2.1 Electrical characteristics (curves)

Figure 1. Power dissipation vs case temperature

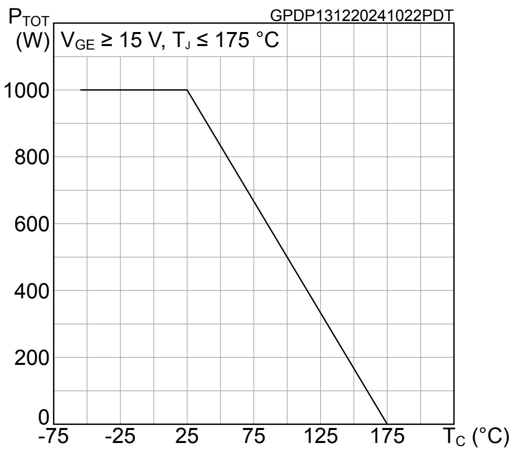


Figure 2. Collector current vs case temperature

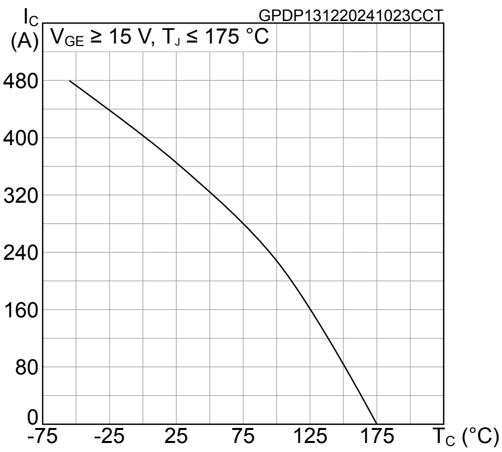


Figure 3. Output characteristics (T_J = 25 °C)

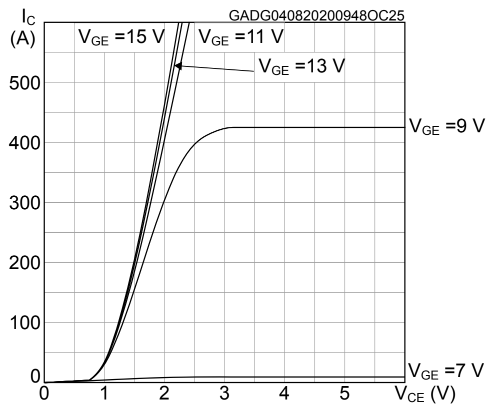


Figure 4. Output characteristics (T_J = 175 °C)

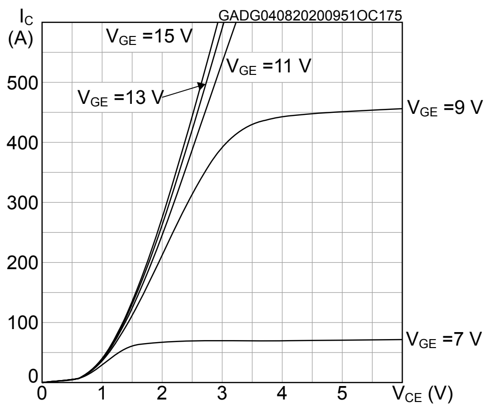


Figure 5. Output characteristics (T_J = -55 °C)

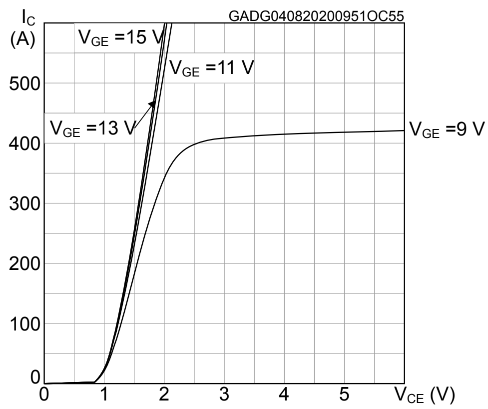


Figure 6. $V_{CE(sat)}$ vs junction temperature

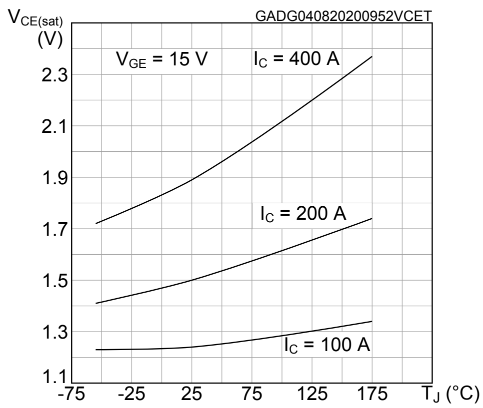


Figure 7. $V_{CE(sat)}$ **vs collector current**

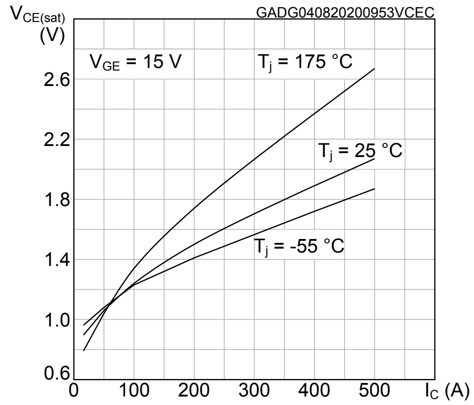


Figure 8. **Forward bias safe operating area**

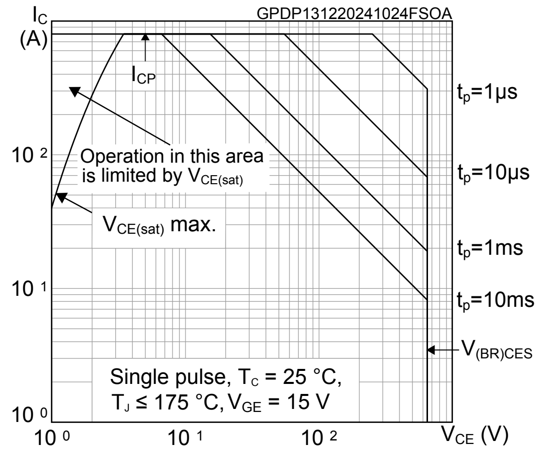


Figure 9. **Transfer characteristics**

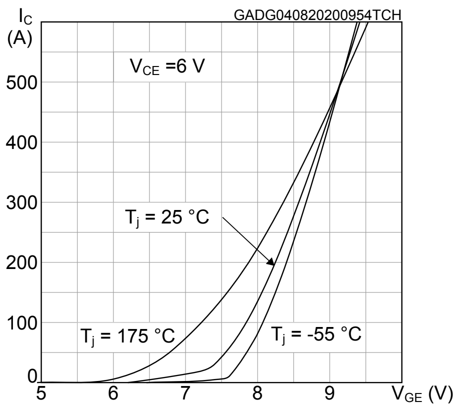


Figure 10. **Diode** V_F **vs forward current**

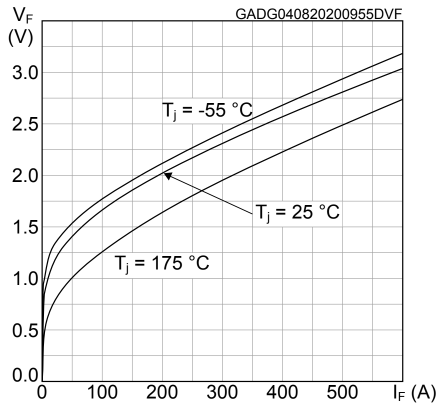


Figure 11. **Normalized** $V_{GE(th)}$ **vs junction temperature**

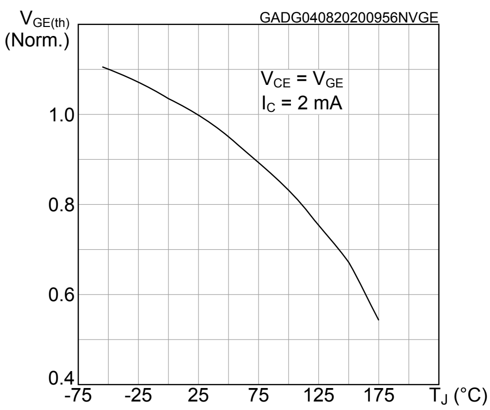


Figure 12. **Normalized** $V_{(BR)CES}$ **vs junction temperature**

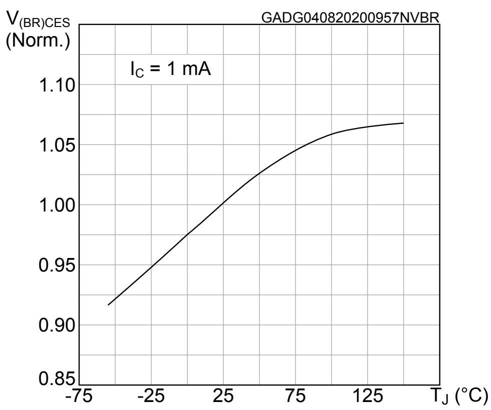


Figure 13. Capacitance variations

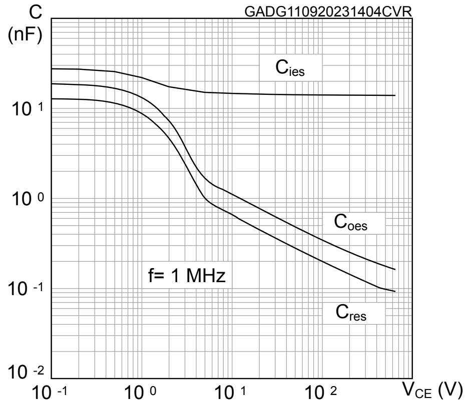


Figure 14. Gate charge vs gate-emitter voltage

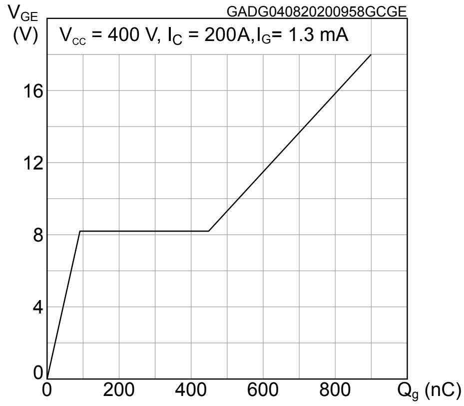


Figure 15. Switching energy vs collector current

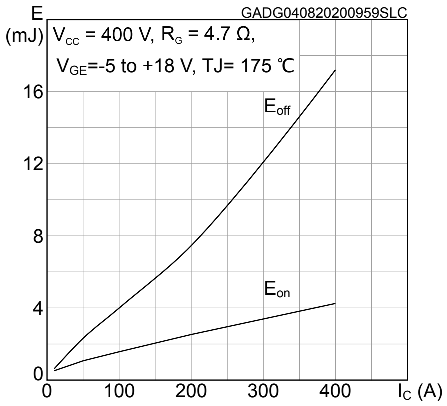


Figure 16. Switching energy vs temperature

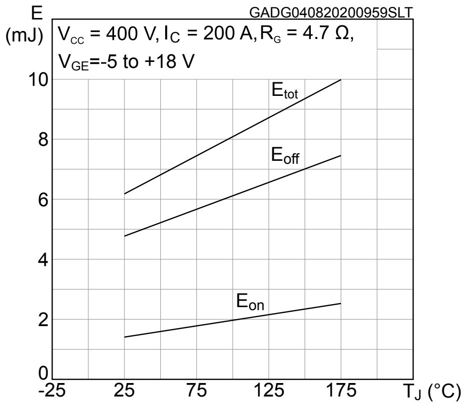


Figure 17. Switching energy vs collector emitter voltage

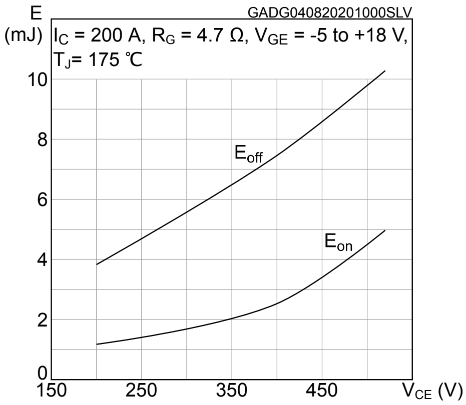


Figure 18. Switching energy vs gate resistance

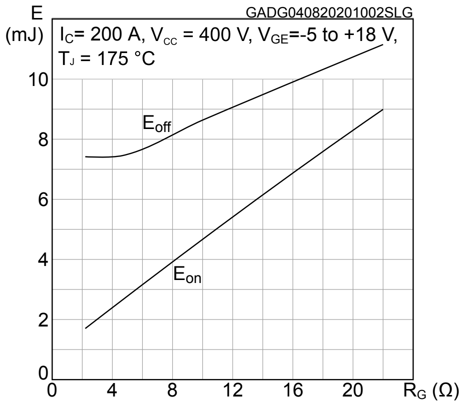


Figure 19. Switching times vs collector current

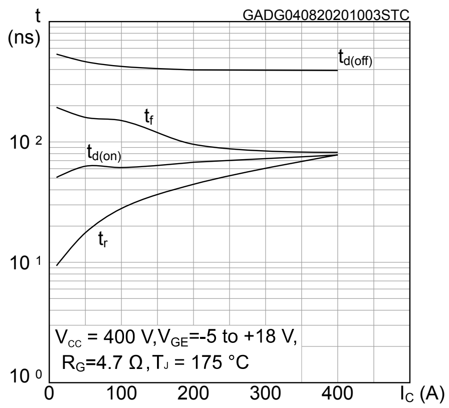


Figure 20. Switching times vs gate resistance

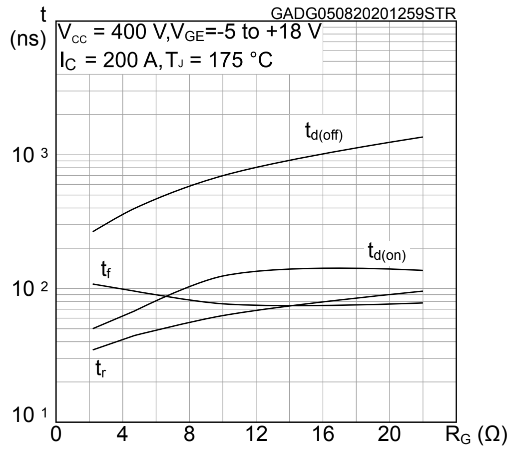


Figure 21. Reverse recovery current vs diode current slope

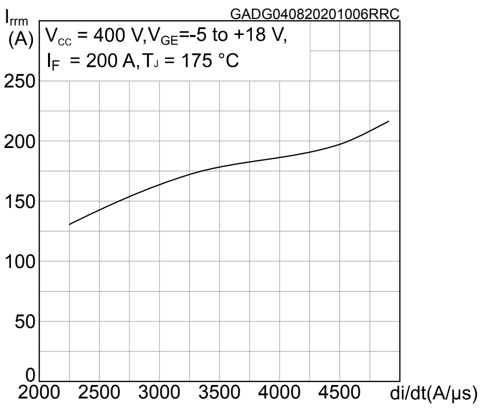


Figure 22. Reverse recovery time vs diode current slope

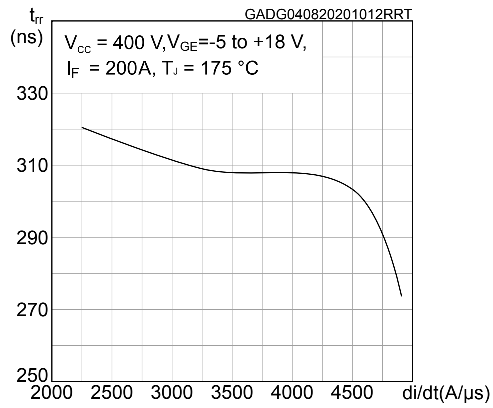


Figure 23. Reverse recovery charge vs diode current slope

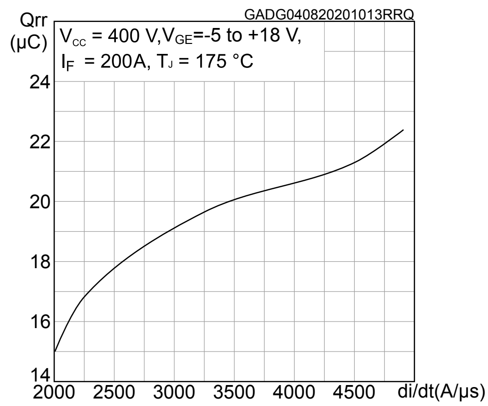


Figure 24. Reverse recovery energy vs diode current slope

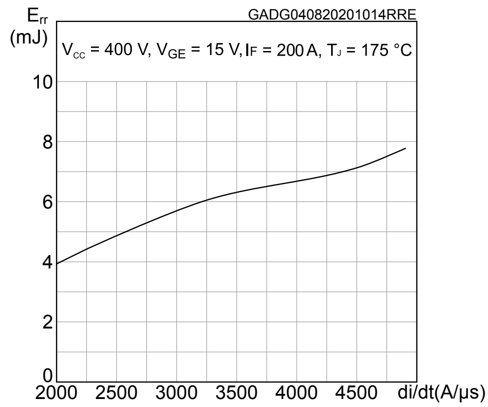


Figure 25. Normalized thermal impedance for IGBT

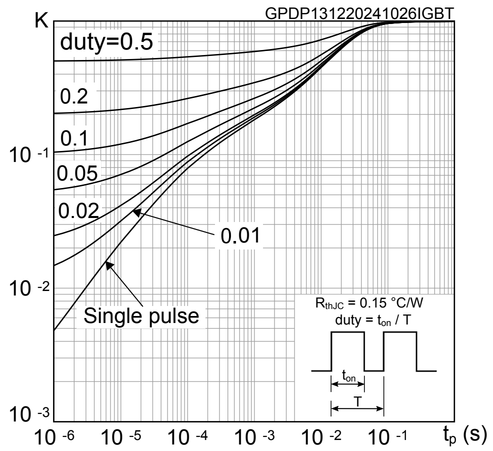
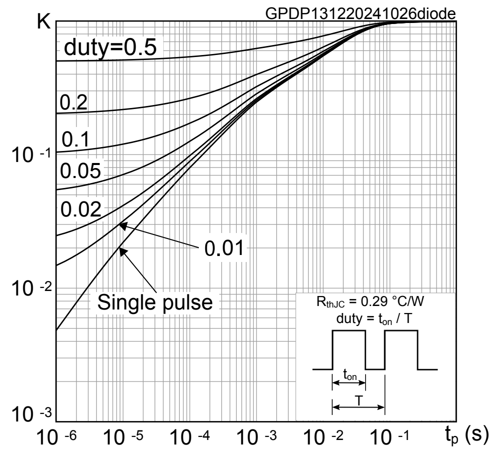


Figure 26. Normalized thermal impedance for diode



3 Test circuits

Figure 27. Test circuit for inductive load switching

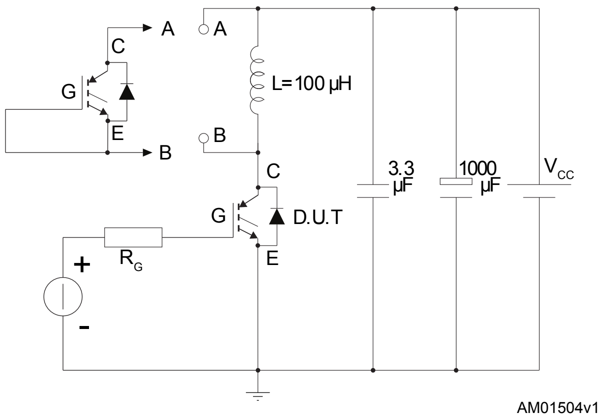


Figure 28. Gate charge test circuit

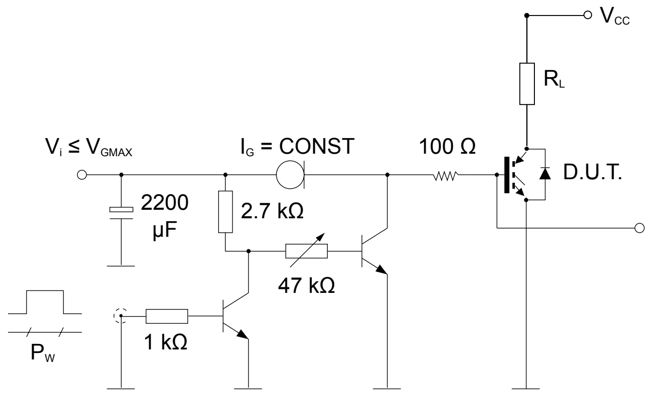


Figure 29. Switching waveform

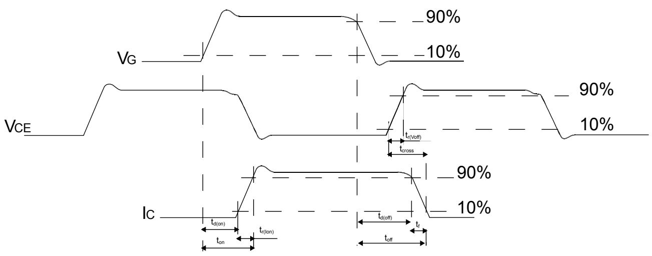
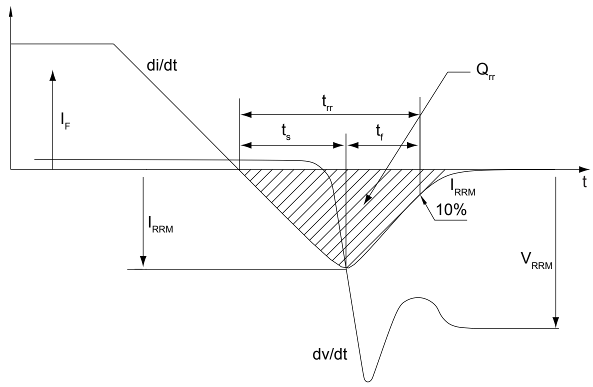


Figure 30. Diode reverse recovery waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 STPAK package information

Figure 31. STPAK package outline

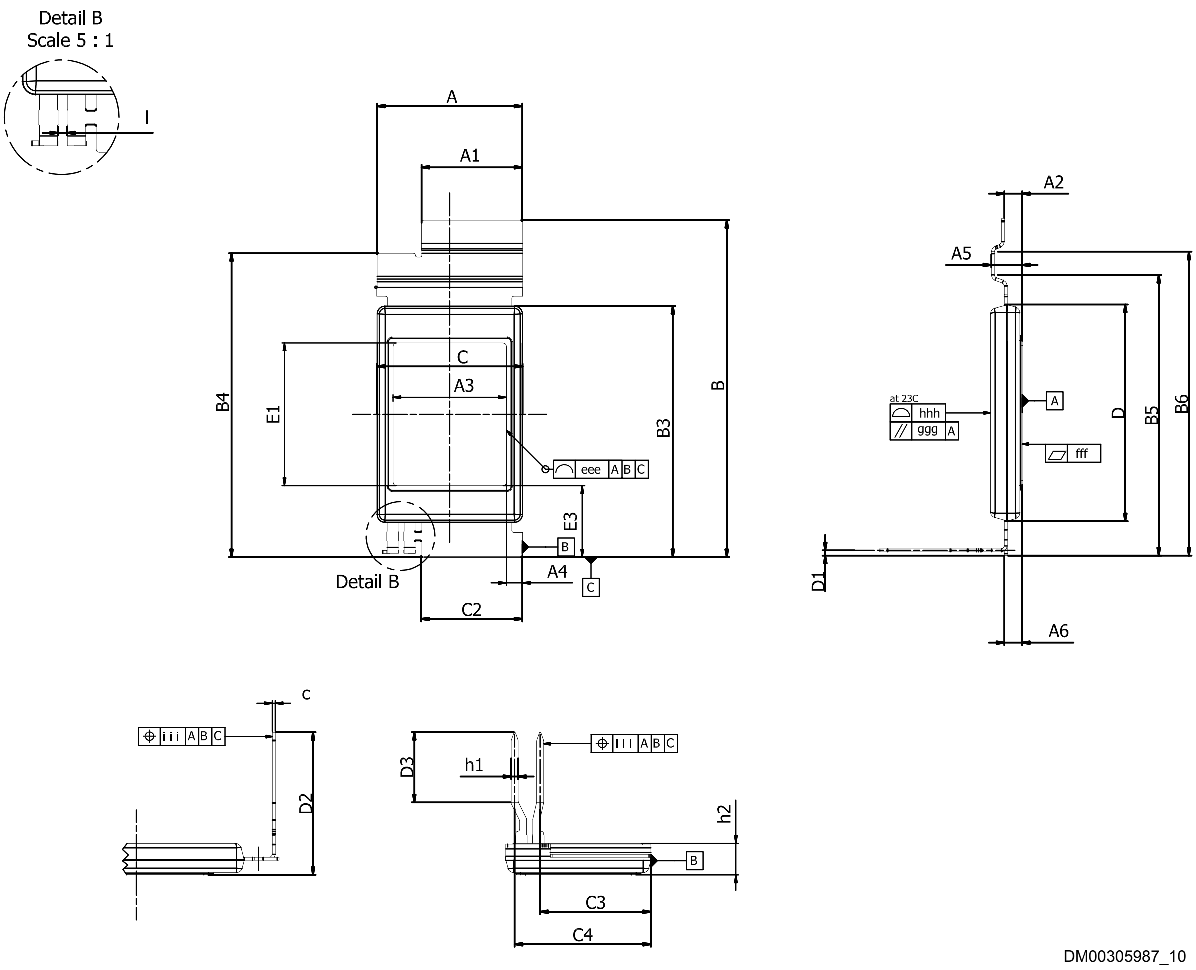


Table 7. STPAK package mechanical data

Ref.	Dimensions			Notes
	mm			
	Min.	Typ.	Max.	
A	18.60	18.80	19.00	
A1	12.85	13.05	13.25	
A2	2.00	2.30	2.60	
A3	13.40	13.90	14.40	Exposed Pad
A4	1.95	2.45	2.95	
A5	3.80	4.00	4.20	
A6	2.10	2.30	2.50	
B	43.40	43.70	44.00	
B3	32.20	32.50	32.80	
B4	39.10	39.40	39.70	
B5	36.07	36.37	36.67	
B6	39.07	39.37	39.67	
c	0.34	0.39	0.44	
C		18.55	19.10	Encompass both large and small cav.
C2	12.90	13.10	13.30	
C3		14.35		
C4		17.65		
D	27.90	28.10	28.30	
D1		0.69		
D2	18.00 (18.50)	18.50 (19.00)	19.00 (19.50)	Refer to the values in brackets for the longer pins type
D3	8.60 (9.10)	9.10 (9.60)	9.60 (10.10)	Refer to the values in brackets for the longer pins type
E1	17.20	17.70	18.20	Exposed pad
E3	9.15	9.65	10.15	
h1	0.85	0.90	0.95	x2 - Pins width
h2	4.00	4.10	4.20	
l	0.60	0.70	0.80	
eee	0.50			
fff	0.10 at 23 °C – 0.05 at 220 °C			Convex with center higher than edges
ggg	0.05			
hhh	0.10			
iii	0.60			

Revision history

Table 8. Document revision history

Date	Revision	Changes
10-Dec-2021	1	Initial release.
13-Nov-2023	2	Updated *Applications* on cover page. Updated *Figure 13. Capacitance variations*. Updated *Section 4.1 STPAK package information*. Minor text changes.
16-Dec-2024	3	Updated *Section 1: Electrical ratings*. Updated *Figure 1. Power dissipation vs case temperature, Figure 2. Collector current vs case temperature, Figure 8. Forward bias safe operating area, Figure 25. Normalized thermal impedance for IGBT* and *Figure 26. Normalized thermal impedance for diode*. Added STGST200G65DTAG order code in STPAK longer pins package. The document has been updated accordingly.
20-Feb-2025	4	Updated Section Product status link / summary.

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