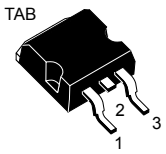
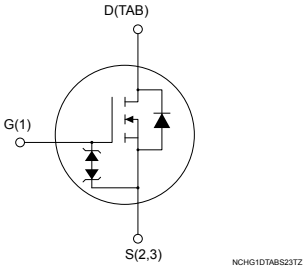
STH22N95K5-2AG

Datasheet

Automotive-grade N-channel 950 V, 280 mΩ typ., 17.5 A MDmesh K5 Power MOSFET in an H²PAK-2 package



H²PAK-2



Product status link
STH22N95K5-2AG

Product summary[1]	
Order code	STH22N95K5-2AG
Marking	22N95K5
Package	H²PAK-2
Packing	Tape and reel

1. *The HTRB test was performed at 80% $V_{(BR)DSS}$ in compliance with AEC-Q101 rev. C. All the other tests were performed according to rev. D.*

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STH22N95K5-2AG	950 V	330 mΩ	17.5 A	250 W

- AEC-Q101 qualified
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	17.5	A
I_D	Drain current (continuous) at T_C = 100 °C	11	A
I_{DM} (1)	Drain current (pulsed)	50	A
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	5	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 17.5 A, di/dt ≤ 100 A/µs; V_{DS} peak ≤ $V_{(BR)DSS}$.*
3. *V_{DS} ≤ 760 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	182	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	950			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 950 V			1	µA
		V_{GS} = 0 V, V_{DS} = 950 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A		280	330	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1550	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(er)}$ (1)	Equivalent capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 760 V	-	65	-	pF
$C_{o(tr)}$ (2)	Equivalent capacitance time related			178	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz , I_D = 0 A	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 17.5 A, V_{GS}= 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	48	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	32.5	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 475 V, I_D = 9 A, R_G = 4.7 Ω V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	18	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	65	-	ns
t_f	Fall time		-	18	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		50	A
V_{SD} (2)	Forward on voltage	I_{SD} = 17.5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 17.5 A, di/dt = 100 A/µs,V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	513		ns
Q_{rr}	Reverse recovery charge		-	12		µC
I_{RRM}	Reverse recovery current		-	46		A
t_{rr}	Reverse recovery time	I_{SD} = 17.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_J = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	670		ns
Q_{rr}	Reverse recovery charge		-	15		µC
I_{RRM}	Reverse recovery current		-	44		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

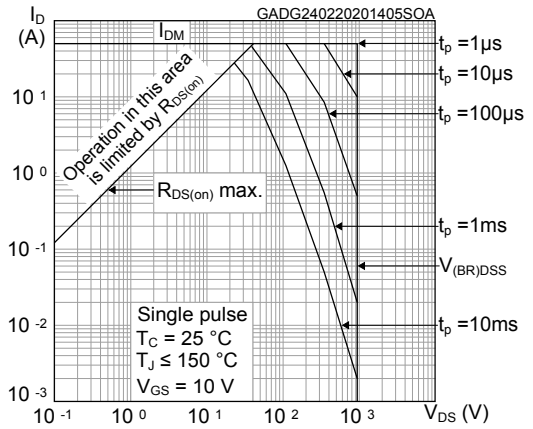


Figure 2. Maximum transient thermal impedance

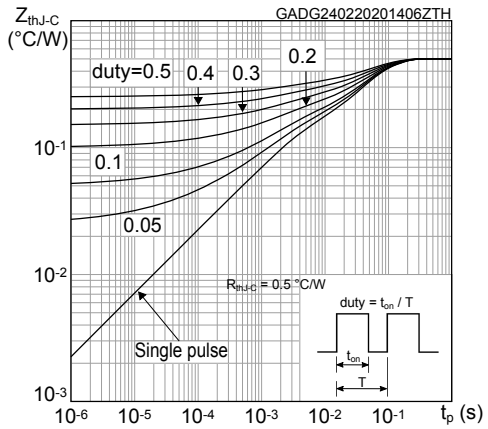


Figure 3. Typical output characteristics

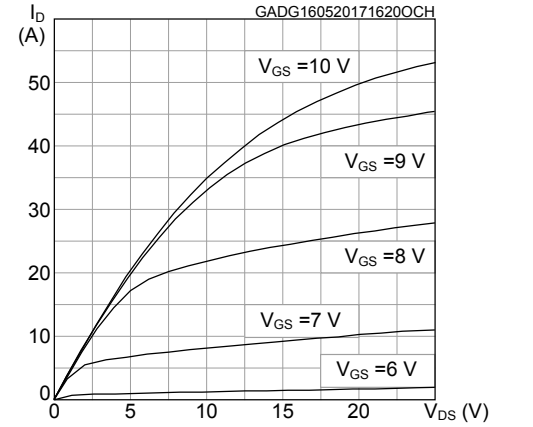


Figure 4. Typical transfer characteristics

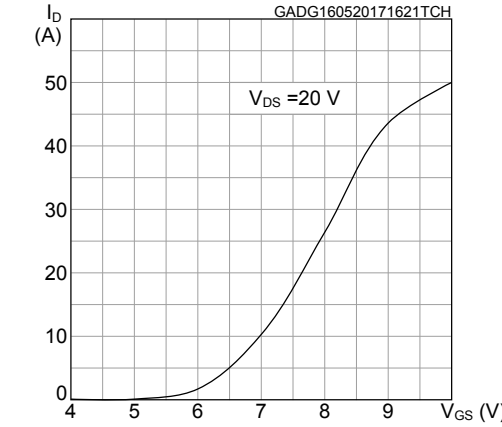


Figure 5. Typical gate charge characteristics

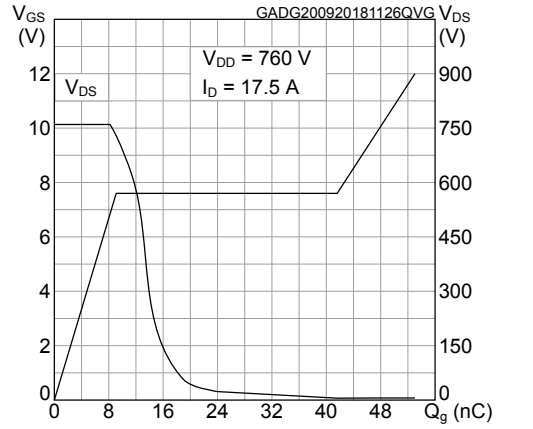


Figure 6. Typical drain-source on-resistance

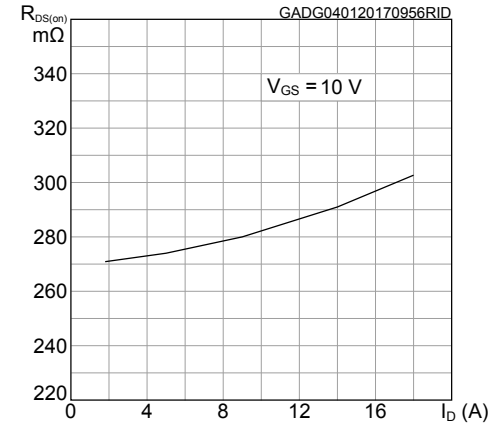


Figure 7. Typical capacitance characteristics

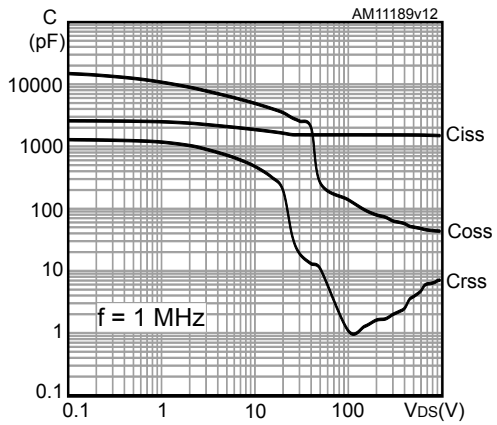


Figure 8. Typical output capacitance stored energy

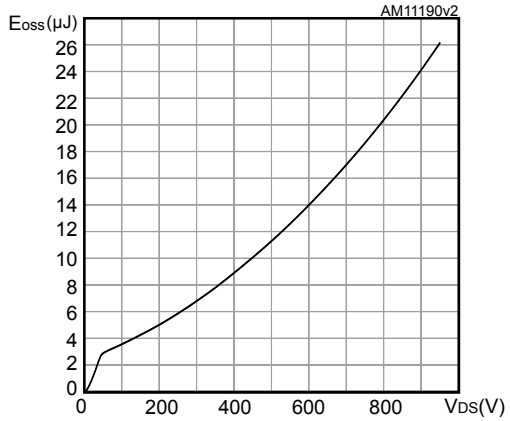


Figure 9. Normalized gate threshold vs temperature

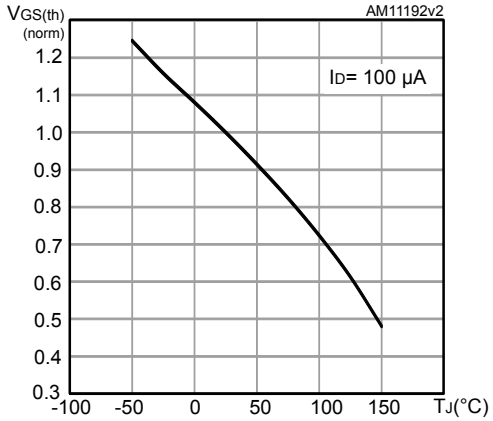


Figure 10. Normalized on-resistance vs temperature

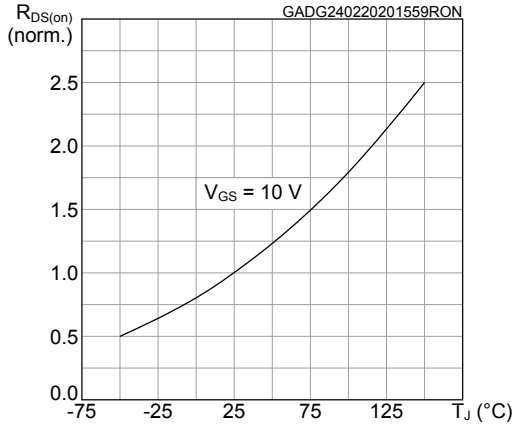


Figure 11. Maximum avalanche energy vs starting T_J

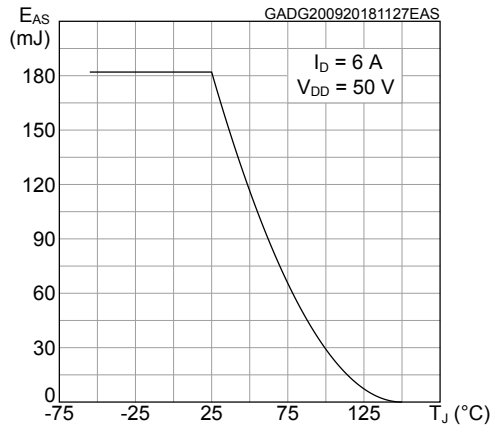


Figure 12. Normalized breakdown voltage vs temperature

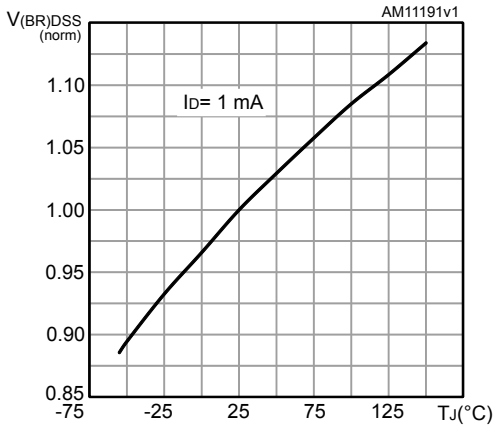
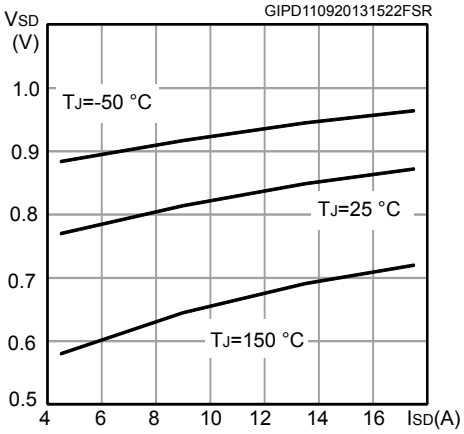


Figure 13. Typical reverse diode forward characteristics



3 Test circuits

Figure 14. Test circuit for resistive load switching times

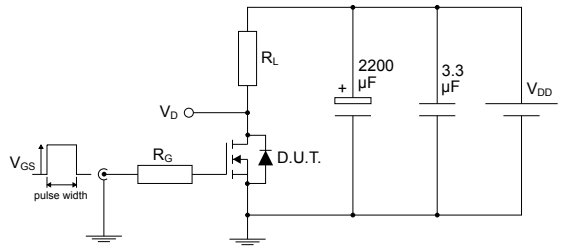


Figure 15. Test circuit for gate charge behavior

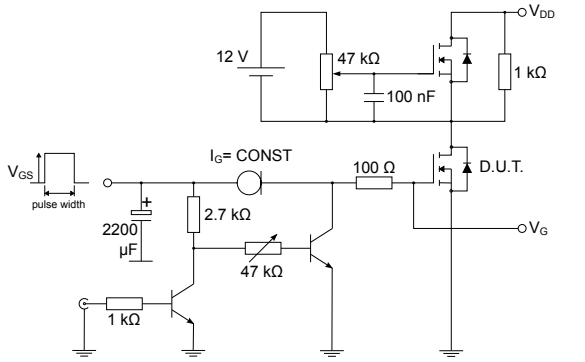


Figure 16. Test circuit for inductive load switching and diode recovery times

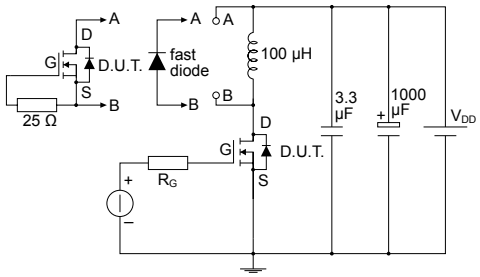


Figure 17. Unclamped inductive load test circuit

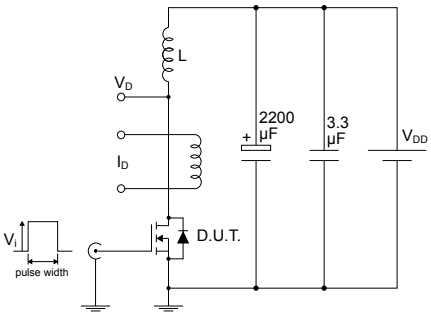


Figure 18. Unclamped inductive waveform

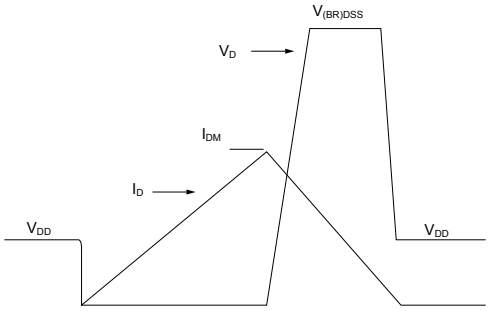
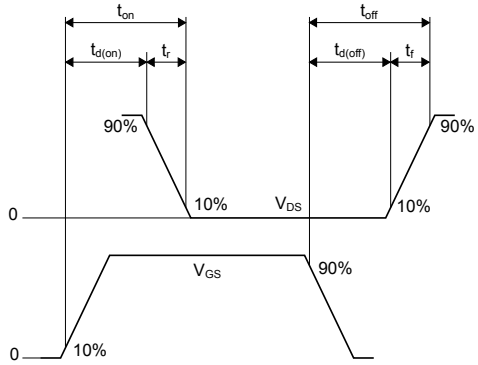


Figure 19. Switching time waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 20. H²PAK-2 package outline

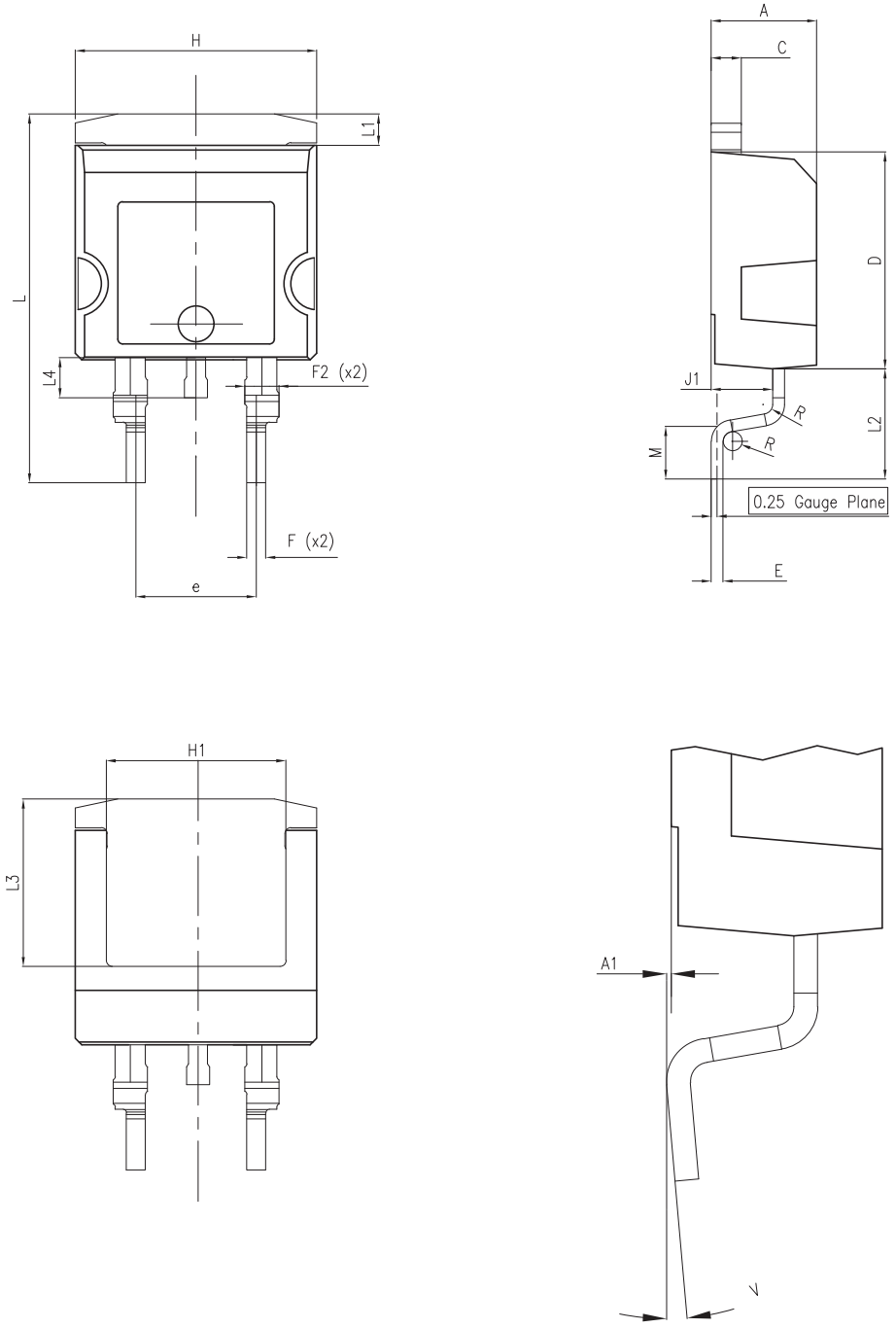
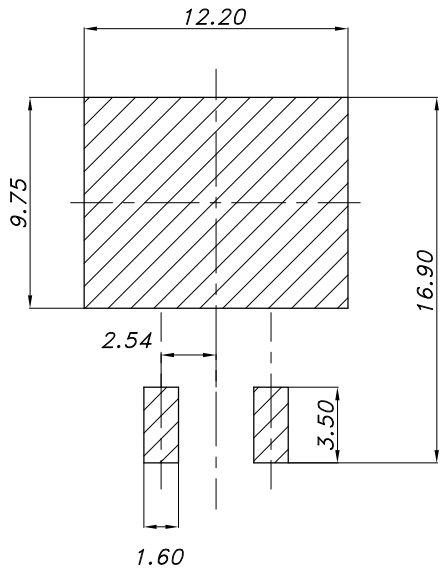


Table 8. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

Figure 21. H²PAK-2 recommended footprint



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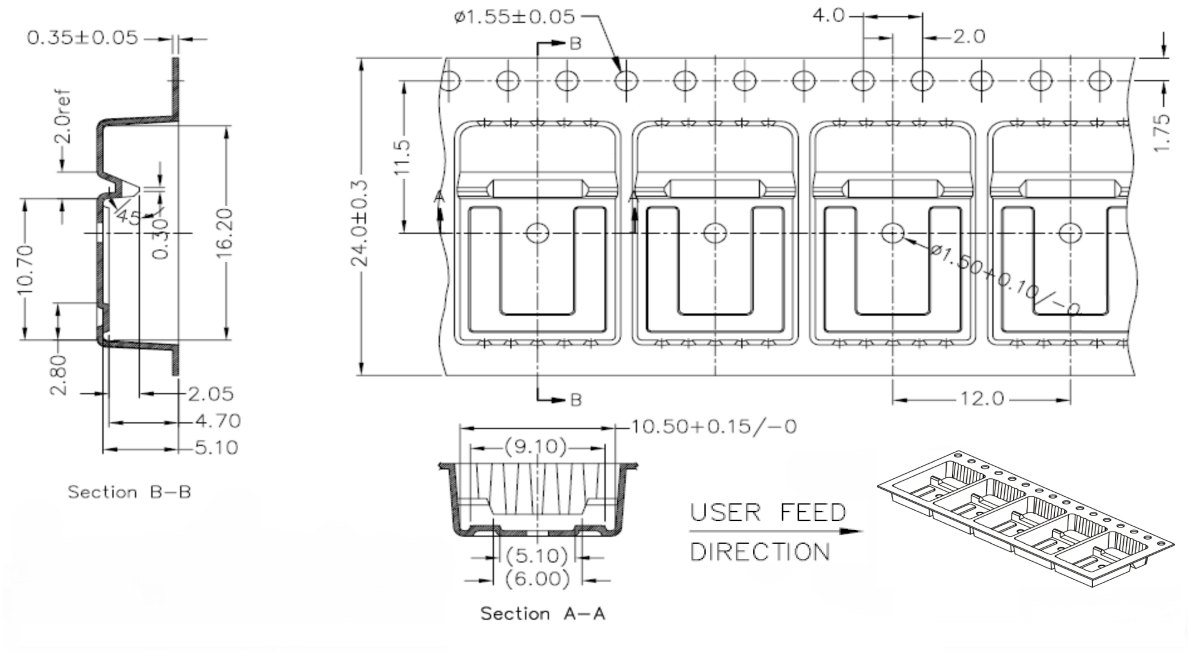
Note: Dimensions are in mm.

4.2 packing information

Figure 22. tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. Document revision history

Date	Revision	Changes
04-Jul-2017	1	First release.
20-Sep-2018	2	Updated *Table 2. Thermal data*, *Figure 5. Gate charge vs gate-source voltage* and *Figure 11. Maximum avalanche energy vs starting T_J*. Updated *Section 4.1 H²PAK-2 package information*.
07-Mar-2019	3	Modified *Table 1. Absolute maximum ratings*. Minor text changes.
4-Mar-2020	4	Updated *Section 2.1 Electrical characteristics (curves)*. Minor text changes.
23-Apr-2020	5	Updated *Section 4.1 H²PAK-2 package information*.
19-Sep-2025	6	Updated Section 4: Package information. Minor text changes.

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