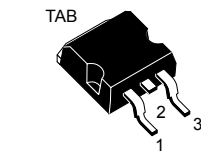
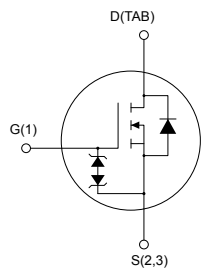


Automotive-grade N-channel 600 V, 70 mΩ typ., 36 A MDmesh™ DM6 Power MOSFET in an H²PAK-2 package


 H²PAK-2


NCHG10TAB523TZ



Product status link


[STH47N60DM6-2AG](#)

Product summary

Order code	STH47N60DM6-2AG
Marking	47N60DM6
Package	H ² PAK-2
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH47N60DM6-2AG	600 V	80 mΩ	36 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Lower R_{DS(on)} per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in R_{DS(on)} per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	36	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	23	A
$I_D^{(1)}$	Drain current (pulsed)	137	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 36\text{ A}$, $di/dt \leq 800\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 480\text{ V}$
3. $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	

1. When mounted on FR-4 board of 1 inch², 2oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{Jmax})	7	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 100\text{ V}$)	700	mJ

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified

Table 4. On/off state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^\circ\text{C}^{(1)}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 18\text{ A}$		70	80	$\text{m}\Omega$

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2350	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{riss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	416	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 36\text{ A}$,	-	55	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	12	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	31	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 18\text{ A}$,	-	23	-	ns
t_r	Rise time	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	5.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	57	-	ns
t_f	Fall time		-	9	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		36	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		137	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 36\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 36\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$	-	115		ns
Q_{rr}	Reverse recovery charge		-	0.54		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 36\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	210		ns
Q_{rr}	Reverse recovery charge		-	2.1		μC
I_{RRM}	Reverse recovery current		(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20.4	

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

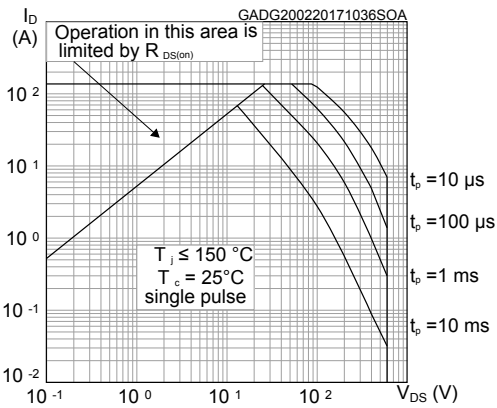


Figure 2. Thermal impedance

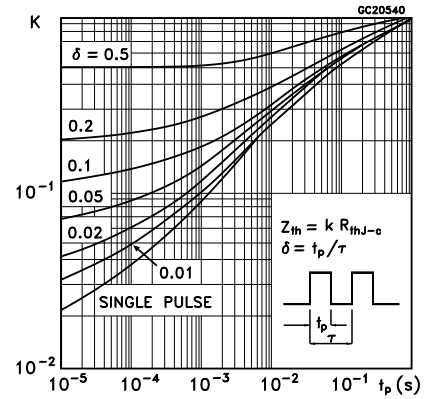


Figure 3. Output characteristics

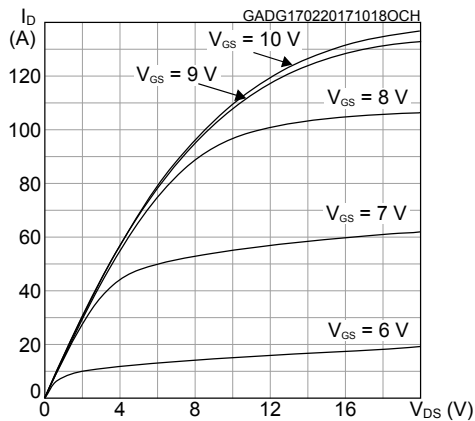


Figure 4. Transfer characteristics

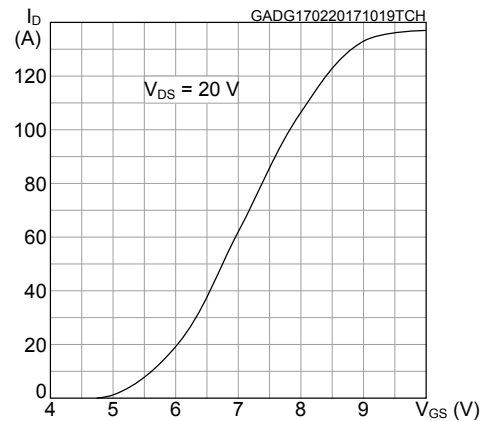


Figure 5. Gate charge vs gate-source voltage

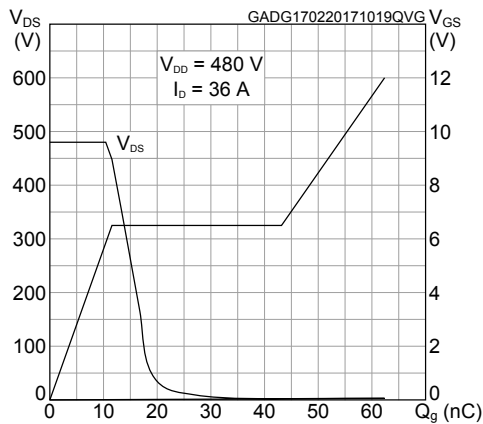


Figure 6. Static drain-source on-resistance

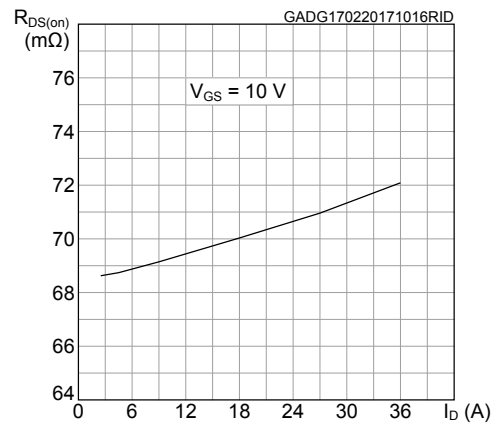


Figure 7. Capacitance variations

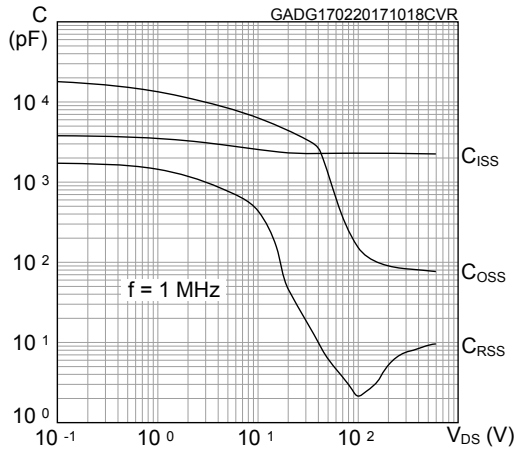


Figure 8. Normalized gate threshold voltage vs temperature

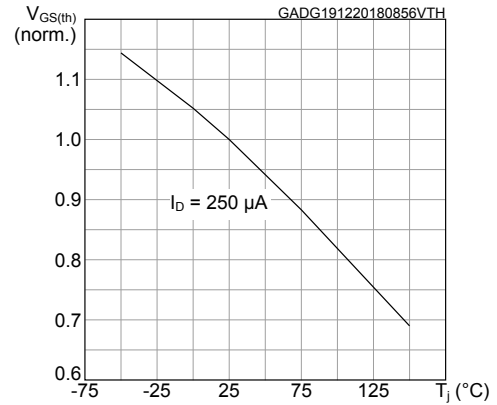


Figure 9. Normalized on-resistance vs temperature

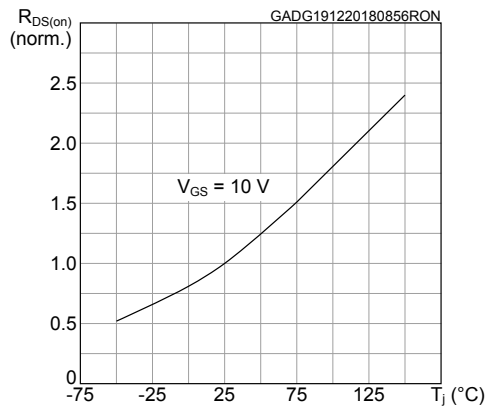


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

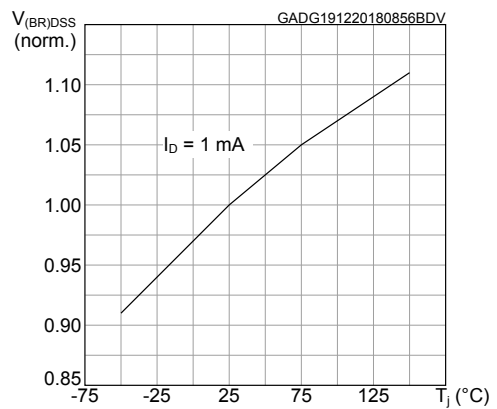


Figure 11. Source-drain diode forward characteristics

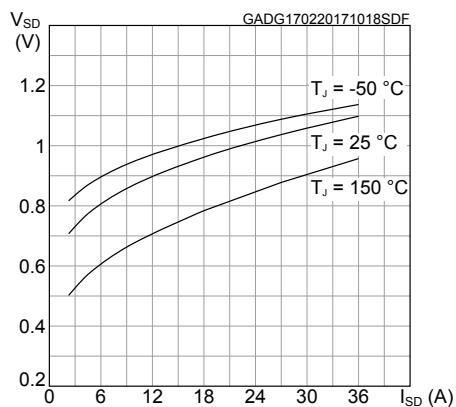
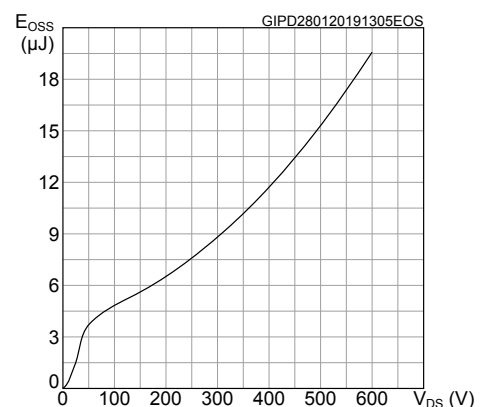


Figure 12. Output capacitance stored energy



3 Test circuits

Figure 13. Test circuit for resistive load switching times

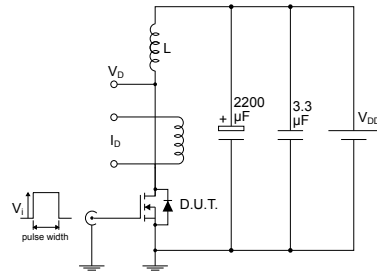

AM01468v1

Figure 14. Test circuit for gate charge behavior


AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times

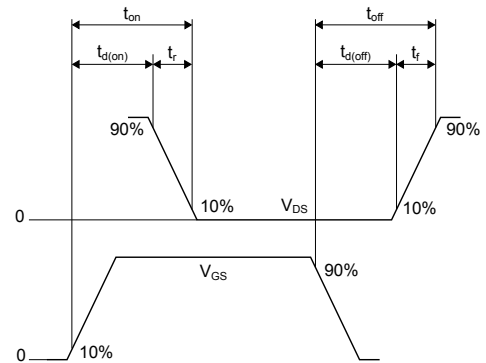

AM01470v1

Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


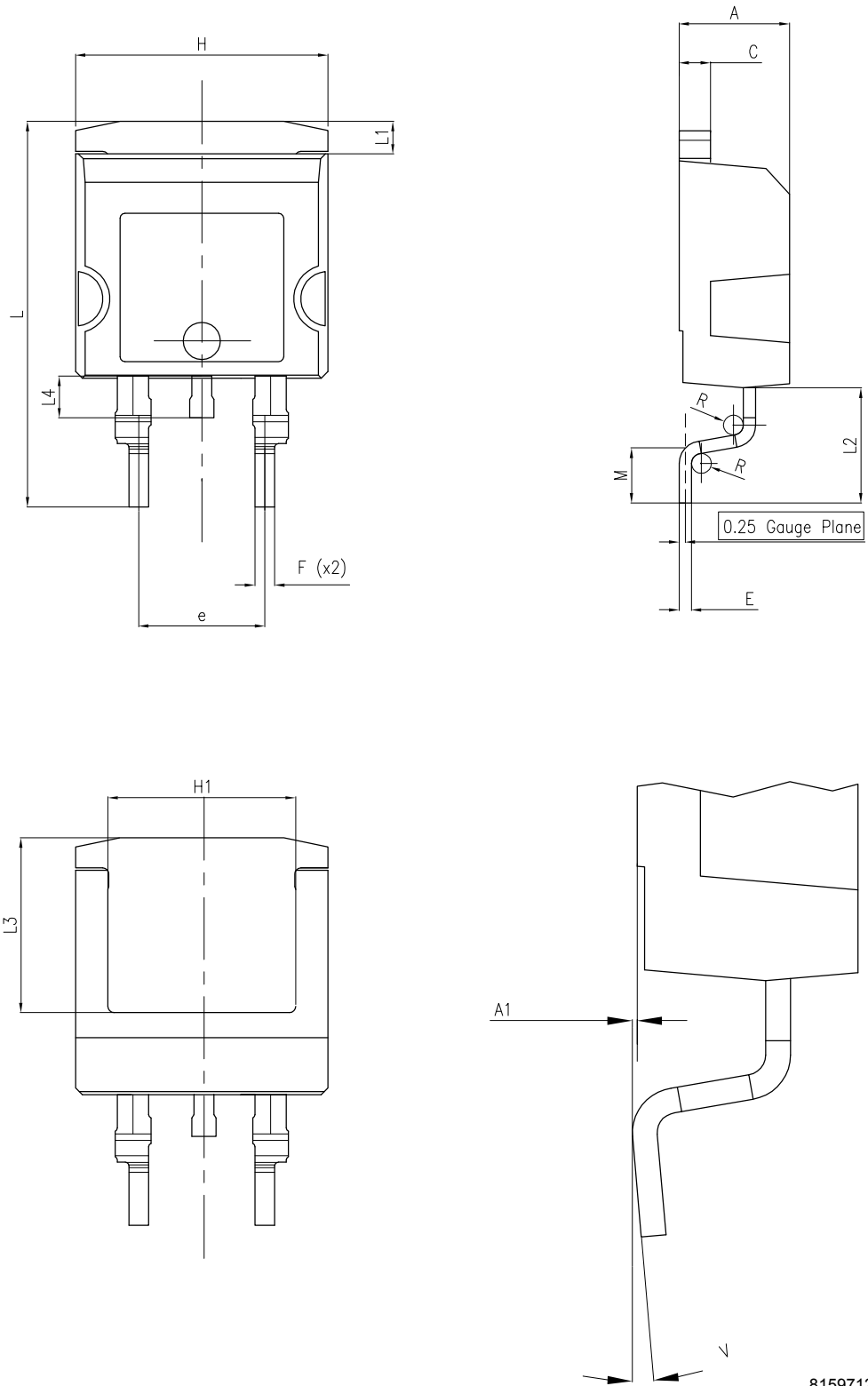
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK[®]** packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 H²PAK-2 package information

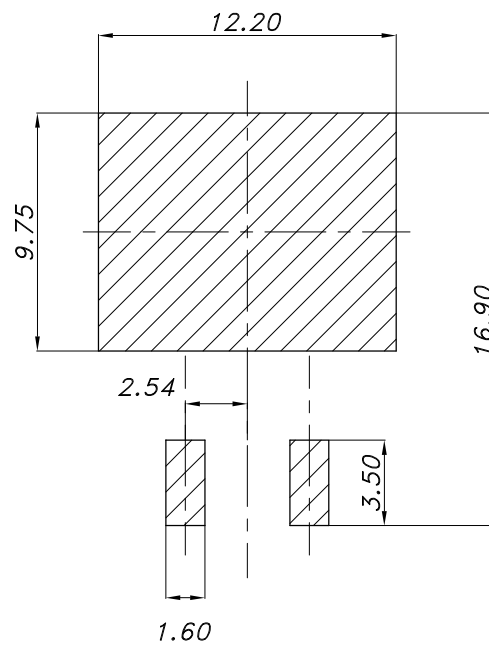
Figure 19. H²PAK-2 package outline



8159712_8

Table 9. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

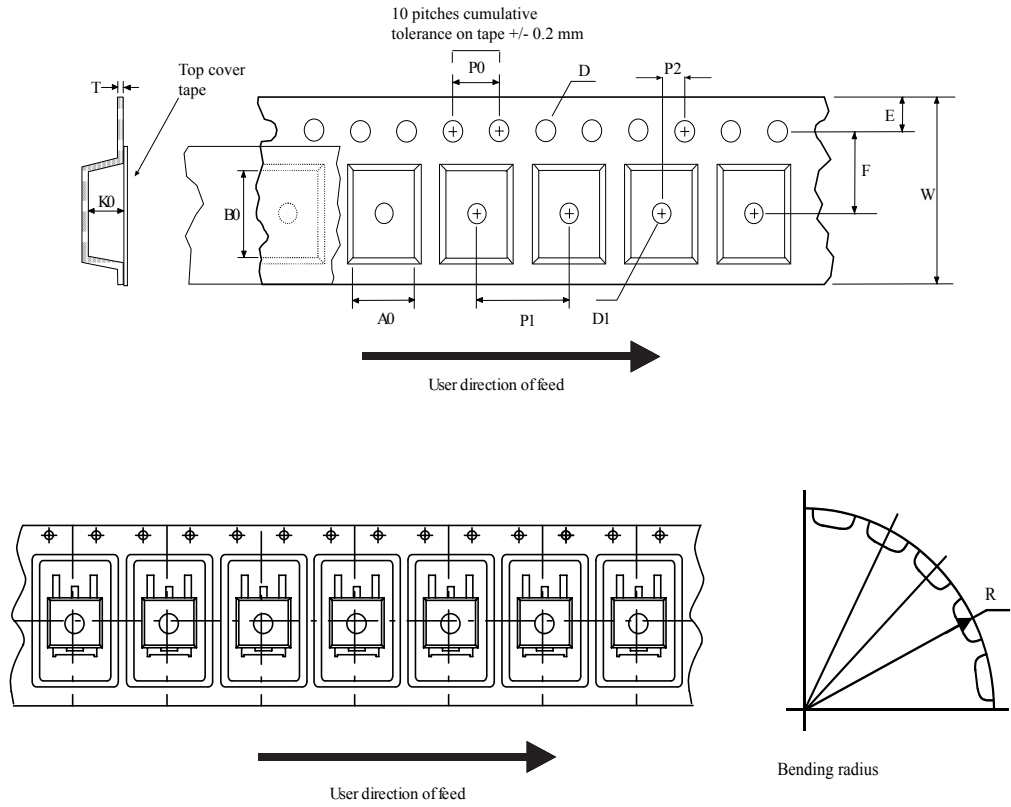
Figure 20. H²PAK-2 recommended footprint


8159712_8

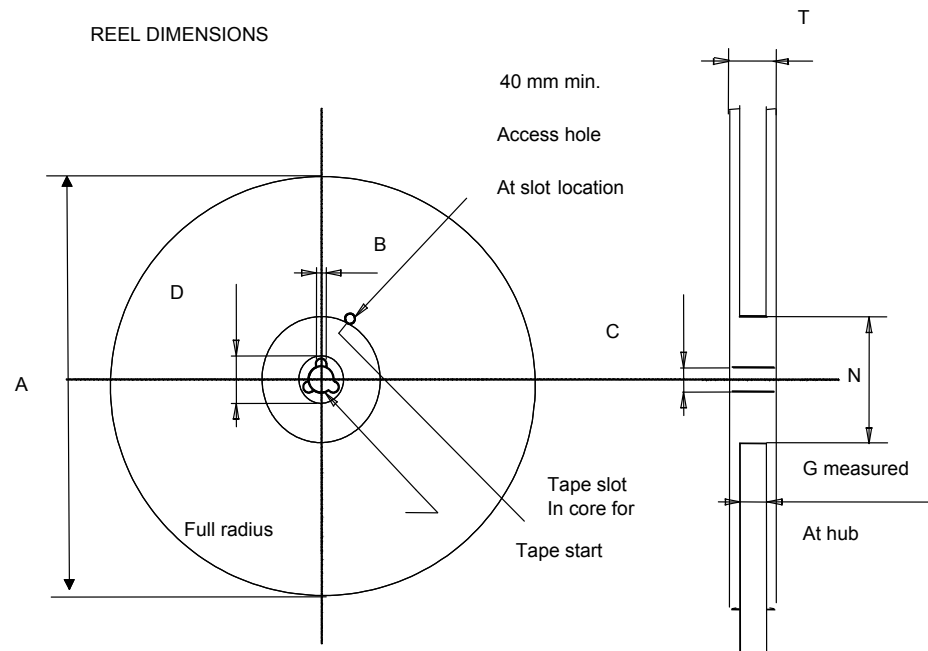
Note: Dimensions are in mm.

4.2 Packing information

Figure 21. Tape outline



AM08852v2

Figure 22. Reel outline

Table 10. Tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 11. Document revision history

Date	Revision	Changes
09-Aug-2017	1	Initial release.
11-Mar-2019	2	Modified title and features on cover page. Modified Section 1 Electrical ratings , Section 2 Electrical characteristics and Section 2.1 Electrical characteristics (curves) . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	H ² PAK-2 package information	8
4.2	Packing information	10
	Revision history	13
	Contents	14

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved