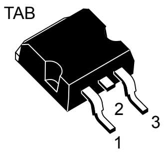
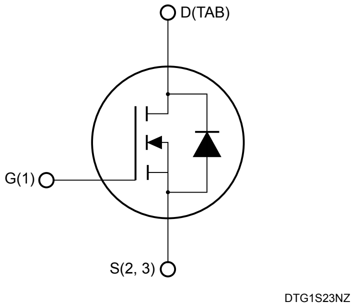
STH4N150-2AG

Datasheet

Automotive-grade N-channel 1500 V, 6 Ω typ., 2.6 A PowerMESH Power MOSFET in an H²PAK-2 package



H^{2}PAK-2



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH4N150-2AG	1500 V	10 Ω	2.6 A

- AEC-Q101 qualified
- Very low gate charge
- 100% avalanche tested

Application

- Switching applications
- Auxiliaries

Description

Very-high-voltage N-channel Power MOSFET developed by using the PowerMESH technology. This device is designed to ensure a high level of voltage and robustness for the automotive market.

Product status link
STH4N150-2AG

Product summary	
Order code	STH4N150-2AG
Marking	4A150
Package	H²PAK-2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	2.6	A
	Drain current (continuous) at T_C = 100 °C	1.6	
I_{DM}(2)	Drain current (pulsed)	10.4	A
P_{TOT}	Total power dissipation at T_C = 25 °C	208	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-247 package.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.6	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	0.8	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 100 V)	10	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. **On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1500 V			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±30 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.3 A		6	10	Ω

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 250 kHz, V_{GS} = 0 V	-	1000	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
R_g	Intrinsic gate resistance	f = 250 kHz , I_D = 0 A	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 1200 V, I_D = 2.5 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	35.1	-	nC
Q_{gs}	Gate-source charge		-	6.7	-	nC
Q_{gd}	Gate-drain charge		-	20.3	-	nC

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 750 V, I_D = 1.3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	6	-	ns
$t_{d(off)}$	Turn-off delay time		-	38	-	ns
t_f	Fall time		-	72	-	ns

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.6	A
I_{SDM} (1)	Source-drain current (pulsed)		-		10.4	A
V_{SD}(2)	Forward on voltage	I_{SD} = 2.6 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 2.6 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	670		ns
Q_{rr}	Reverse recovery charge		-	4.4		µC
I_{RRM}	Reverse recovery current		-	12.8		A
t_{rr}	Reverse recovery time	I_{SD} = 2.6 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	825		ns
Q_{rr}	Reverse recovery charge		-	5.5		µC
I_{RRM}	Reverse recovery current		-	13.4		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. **Safe operating area**

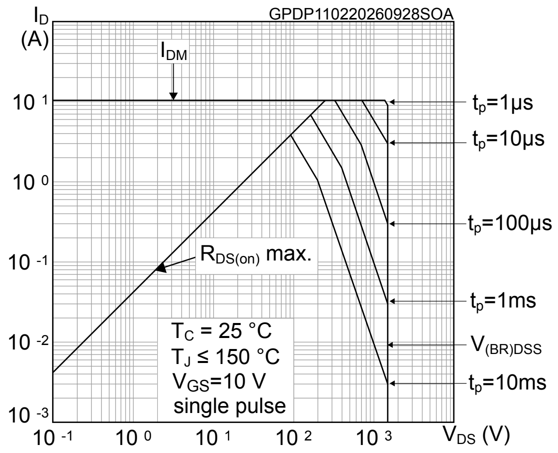


Figure 2. **Maximum transient thermal impedance**

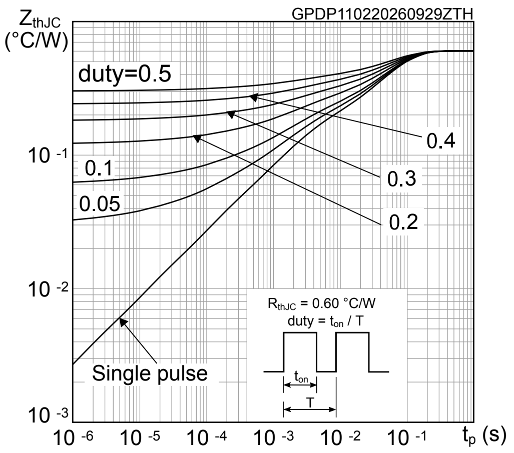


Figure 3. **Typical output characteristics**

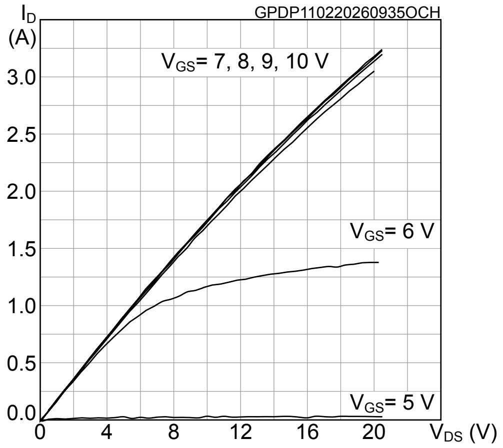


Figure 4. **Typical transfer characteristics**

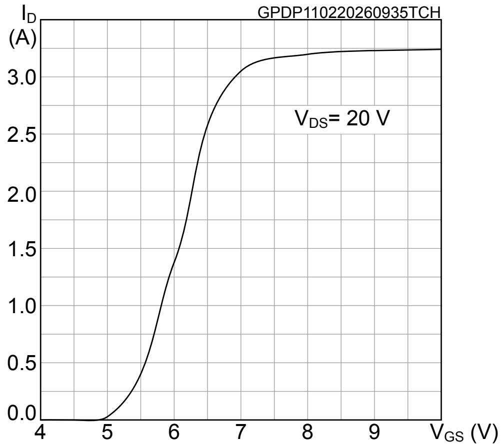


Figure 5. **Typical gate charge characteristics**

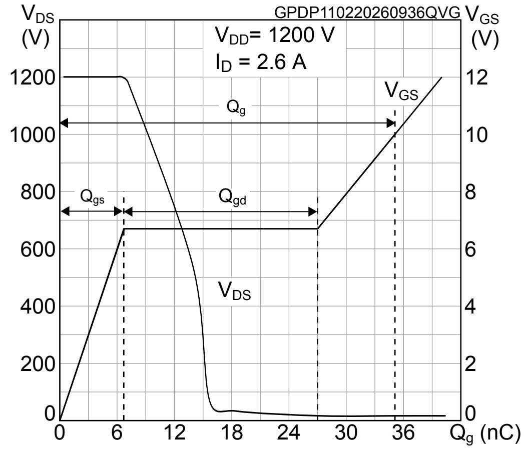


Figure 6. **Typical drain-source on-resistance**

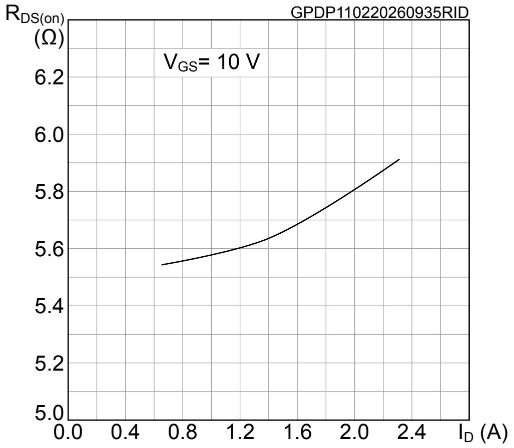


Figure 7. Typical capacitance characteristics

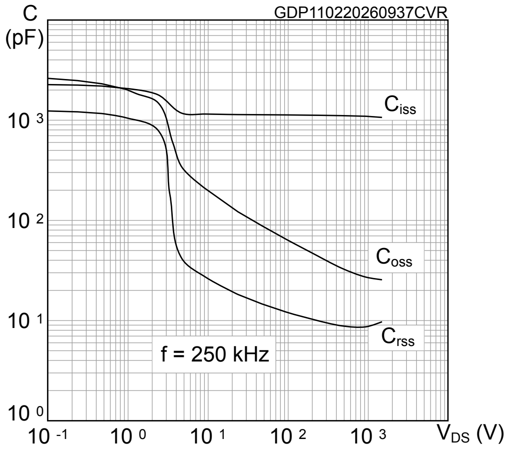


Figure 8. Normalized gate threshold vs temperature

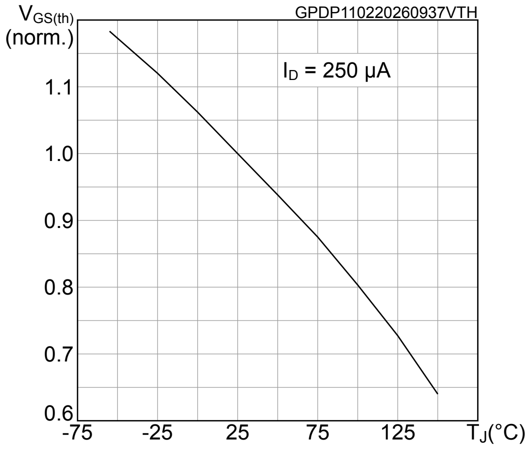


Figure 9. Normalized on-resistance vs temperature

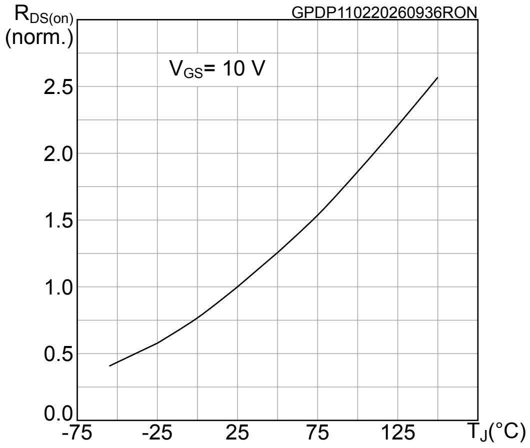


Figure 10. Normalized breakdown voltage vs temperature

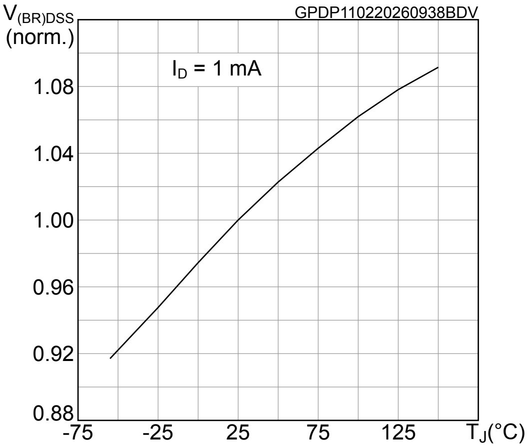
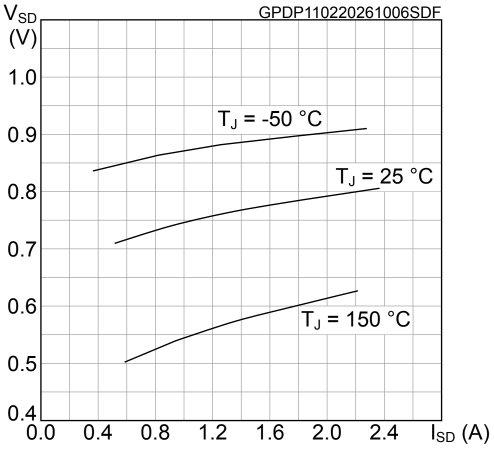


Figure 11. Typical reverse diode forward characteristics



3 Test circuits

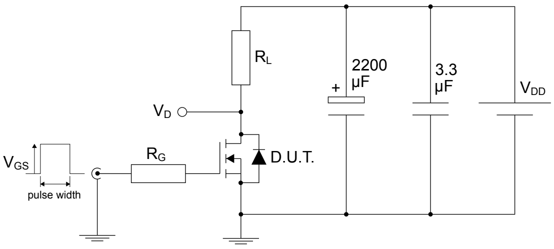


Figure 12. Test circuit for resistive load switching times

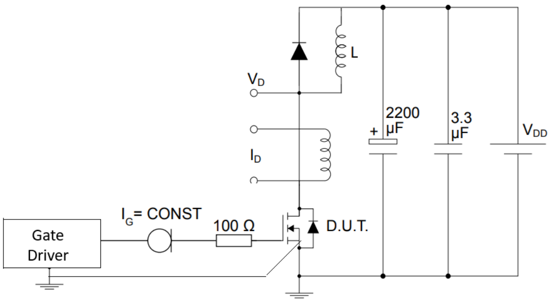


Figure 13. Test circuit for gate charge behavior

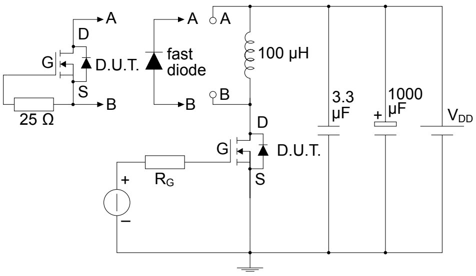


Figure 14. Test circuit for inductive load switching and diode recovery times

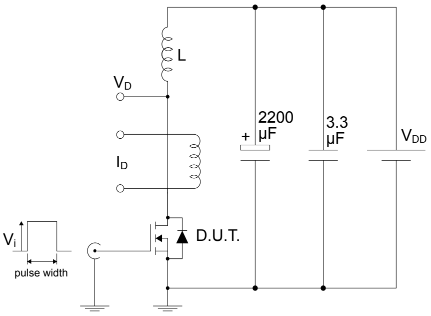


Figure 15. Unclamped inductive load test circuit

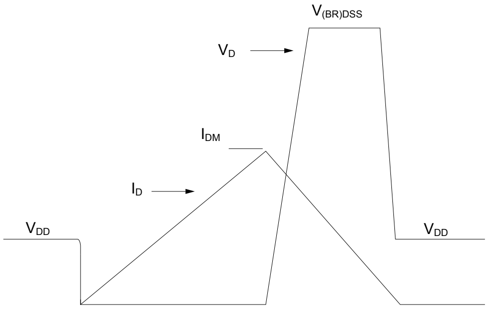


Figure 16. Unclamped inductive waveform

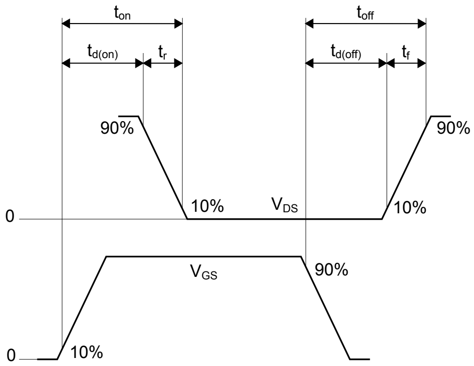


Figure 17. Switching time waveform

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 18. H²PAK-2 package outline

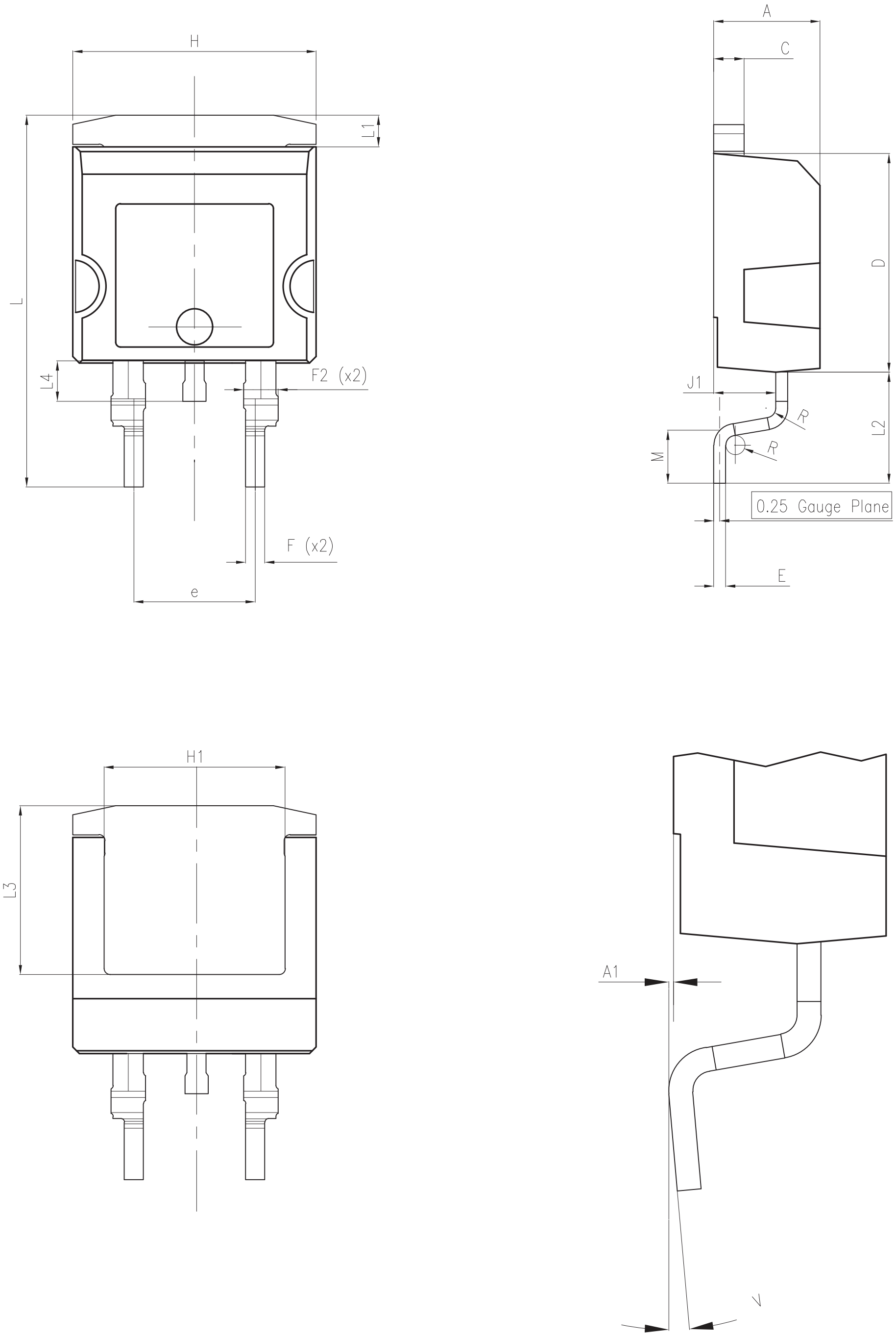
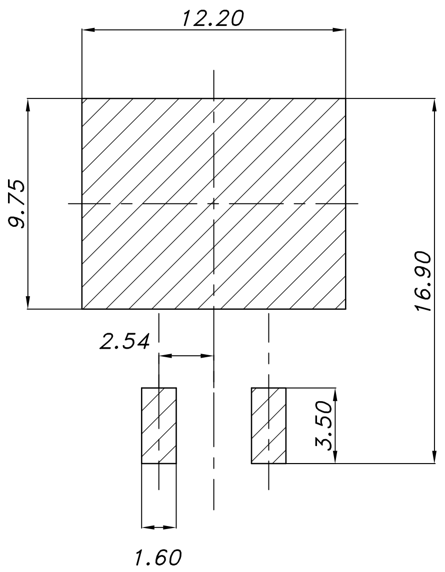


Table 8. **H²PAK-2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40		7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

Figure 19. **H²PAK-2 recommended footprint**



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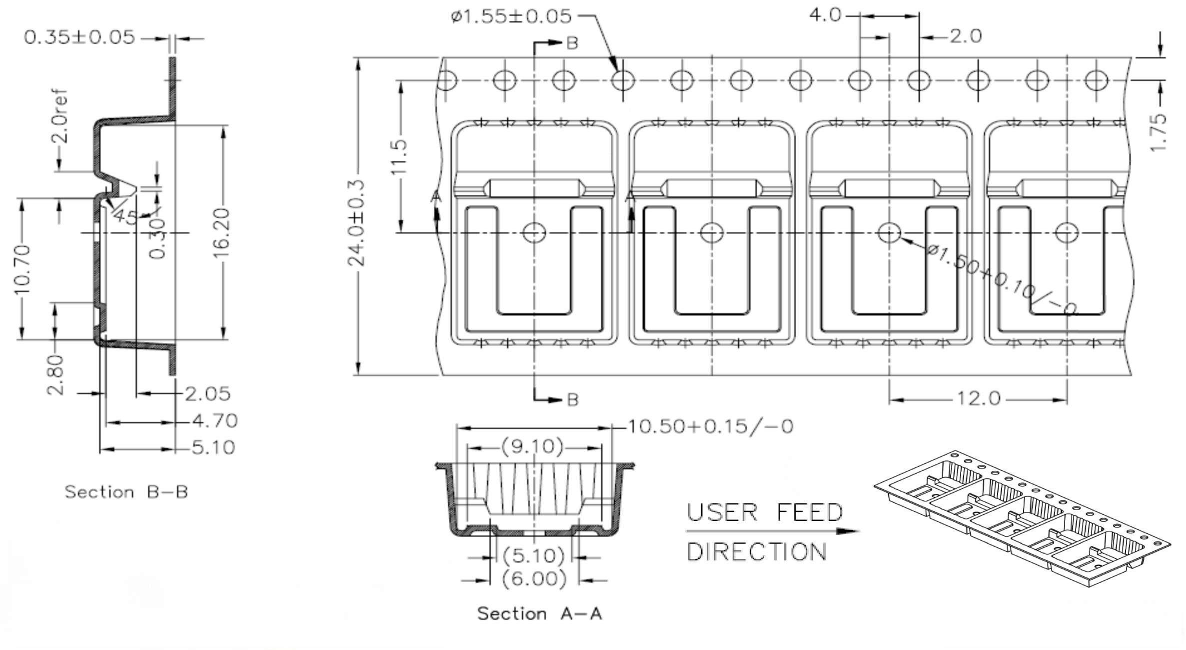
Note: *Dimensions are in mm.*

4.2 H²PAK-2 packing information

Figure 20. H²PAK-2 tape drawing (dimensions are in mm)



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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
12-Feb-2026	1	First release.

Contents

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