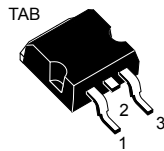
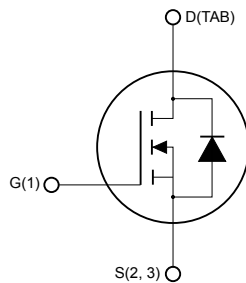


Automotive-grade N-channel 600 V, 76 mΩ typ., 27 A MDmesh DM9 Power MOSFET in an H²PAK-2 package



H²PAK-2




DTG1S23NZ



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH60N099DM9-2AG	600 V	99 mΩ	27 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Worldwide best R_{DS(on)} per area among silicon-based fast recovery devices
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low R_{DS(on)} per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and R_{DS(on)} makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link

[STH60N099DM9-2AG](#)

Product summary

Order code	STH60N099DM9-2AG
Marking	60A099DM9
Package	H ² PAK-2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	27	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	17	
$I_{DM}^{(1)}$	Drain current (pulsed)	105	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	179	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	120	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	1300	A/ μs
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 13.5\text{ A}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.7	$^\circ\text{C/W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	333	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			5	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			200	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$, $I_D = 13.5\text{ A}$		76	99	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2140	-	pF
C_{oss}	Output capacitance		-	45	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	420	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, open drain	-	2	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 13.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	44	-	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 13.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	18	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	58	-	ns
t_f	Fall time		-	5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		27	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		105	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 27\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 27\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	130		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	0.8		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 27\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	200		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	2		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	17		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

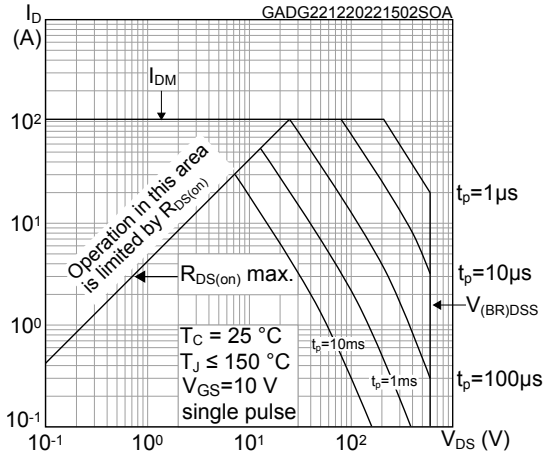


Figure 2. Maximum transient thermal impedance

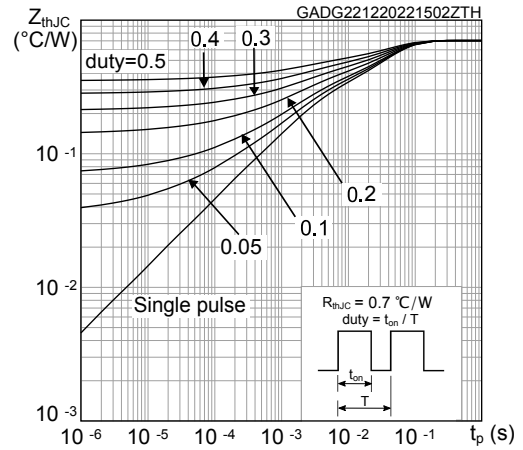


Figure 3. Typical output characteristics

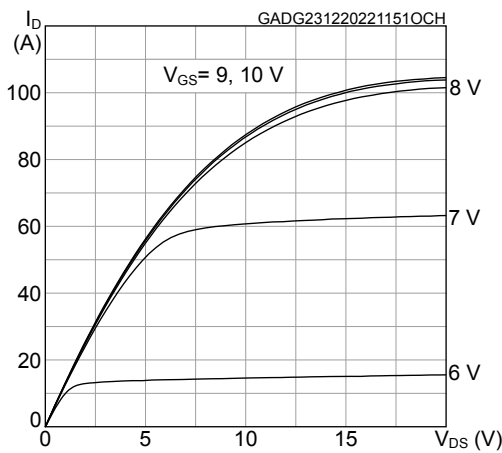


Figure 4. Typical transfer characteristics

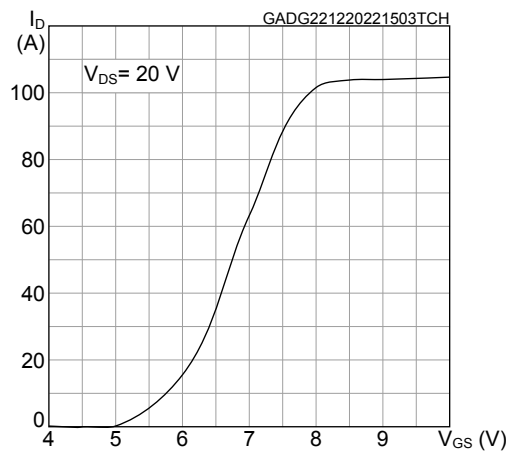


Figure 5. Typical gate charge characteristics

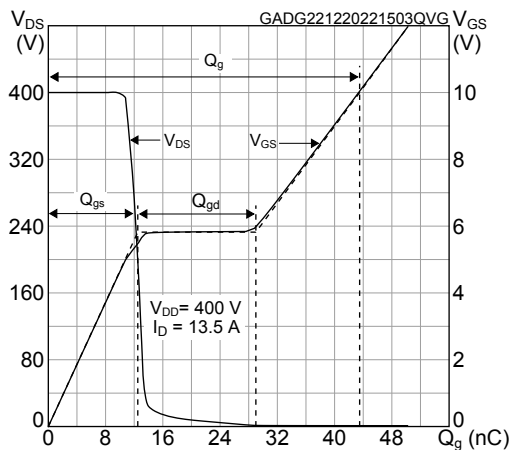


Figure 6. Typical drain-source on-resistance

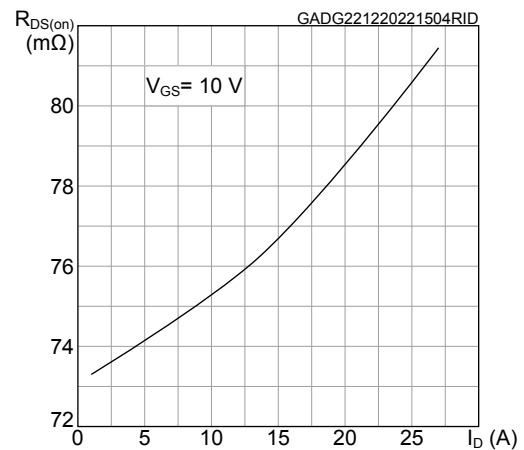
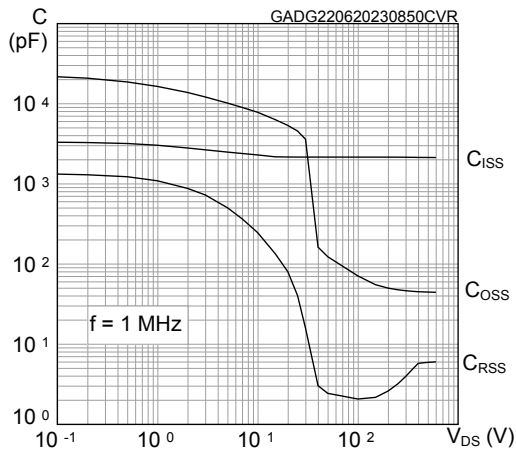
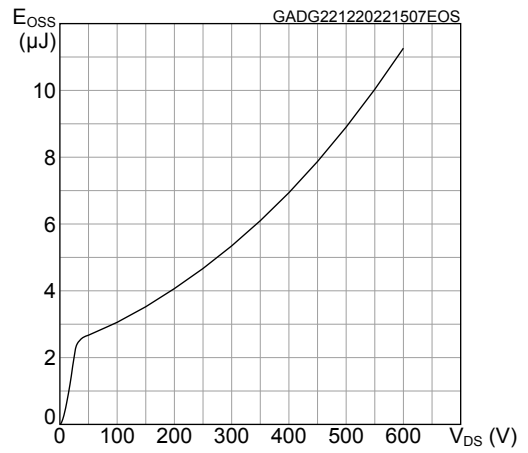
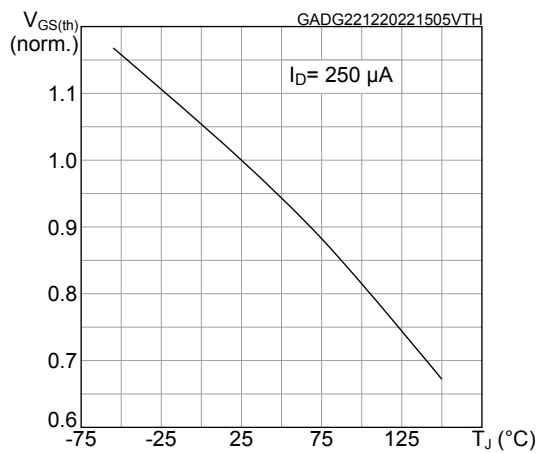
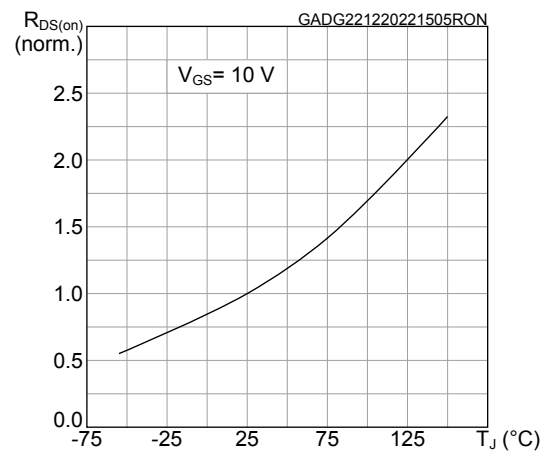
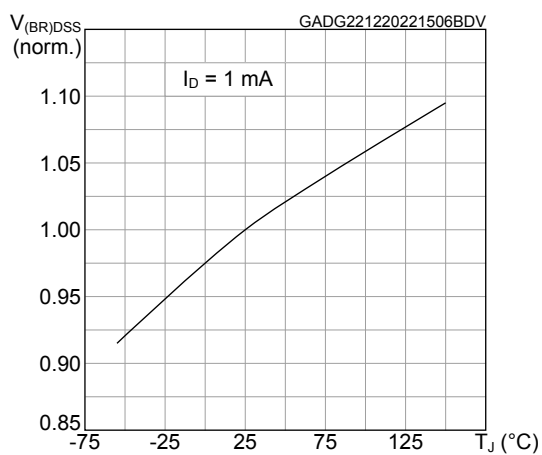
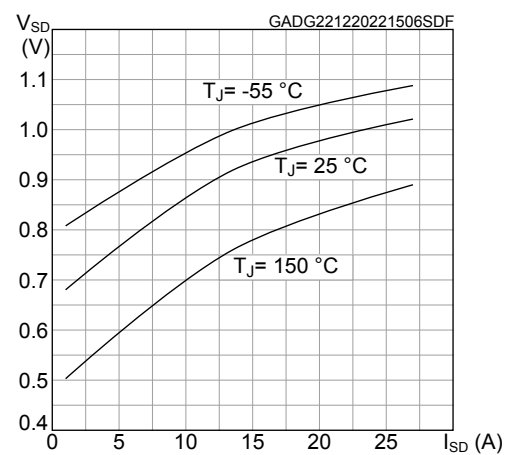
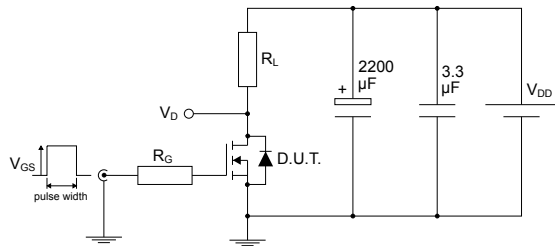
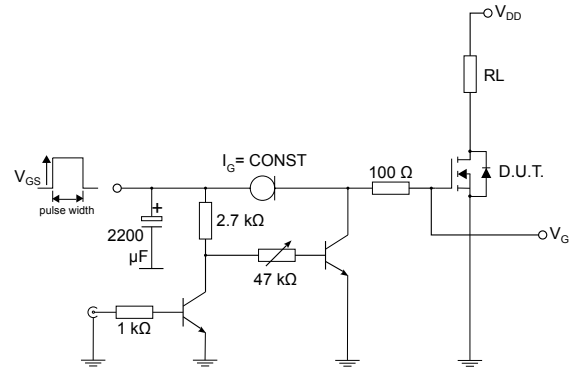


Figure 7. Typical capacitance characteristics

Figure 8. Typical output capacitance stored energy

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Normalized breakdown voltage vs temperature

Figure 12. Typical reverse diode forward characteristics


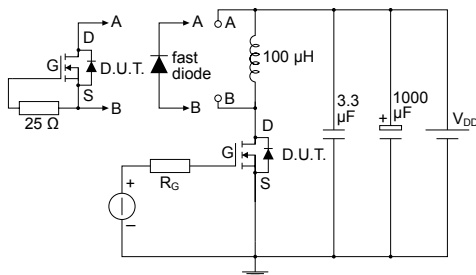
3 Test circuits

Figure 13. Test circuit for resistive load switching times


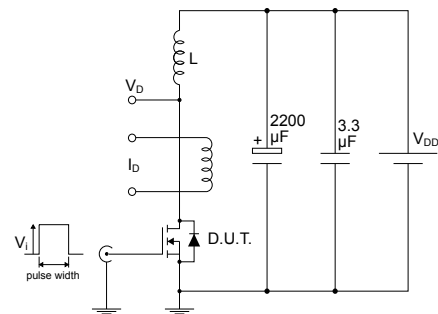
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Figure 14. Test circuit for gate charge behavior


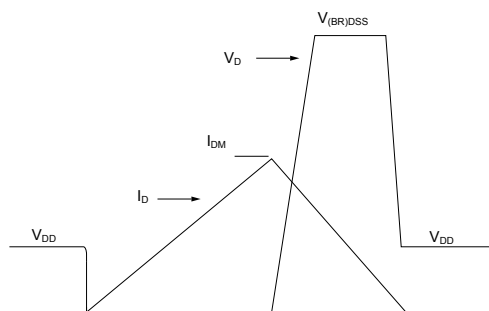
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Figure 15. Test circuit for inductive load switching and diode recovery times


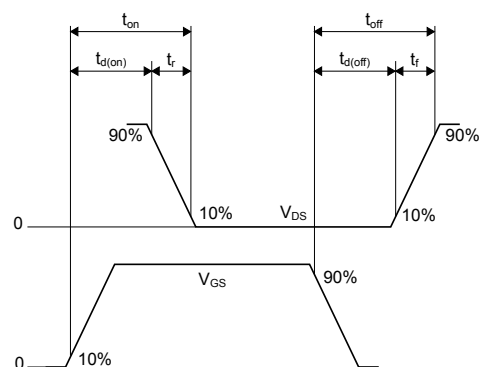
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


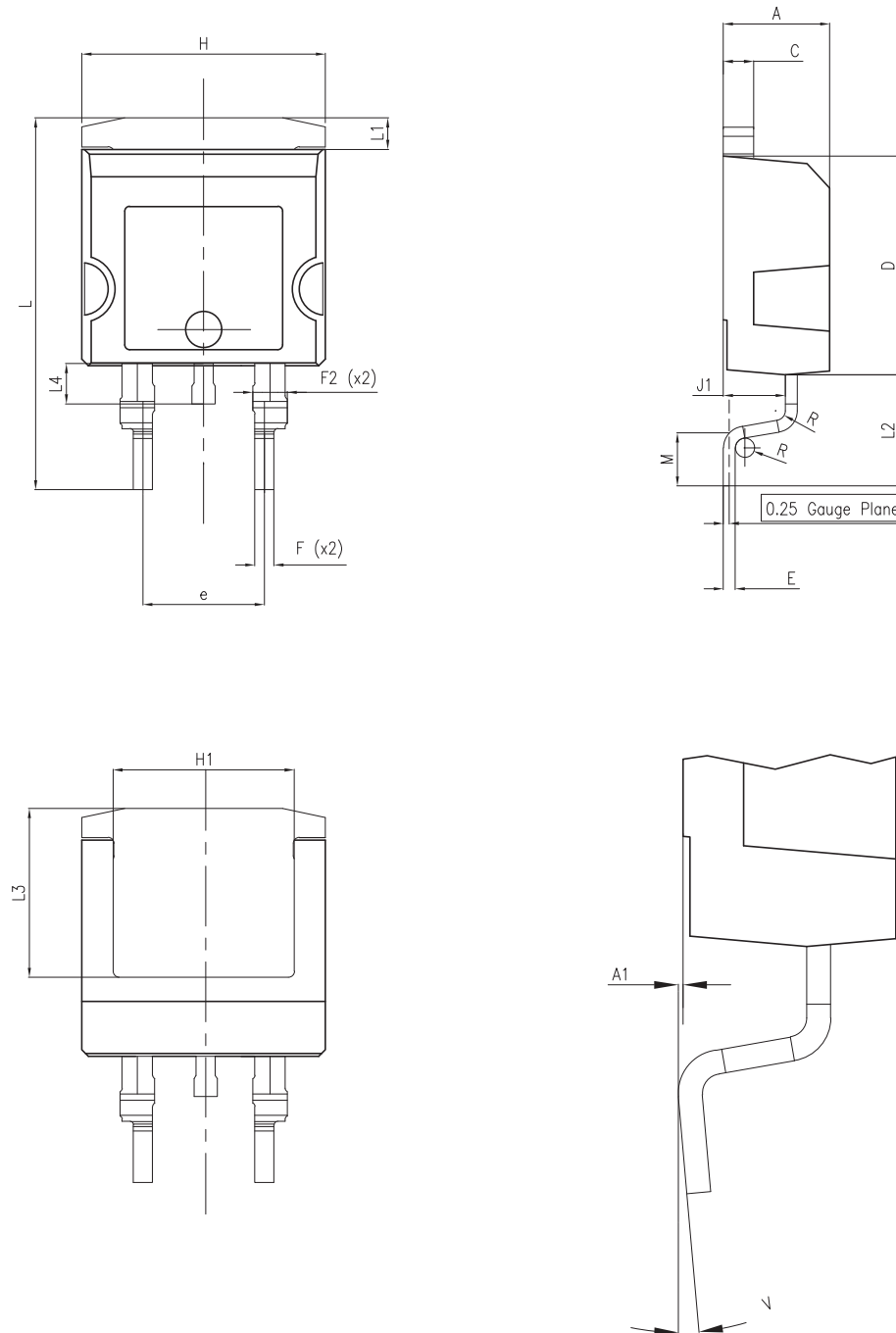
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 19. H²PAK-2 package outline

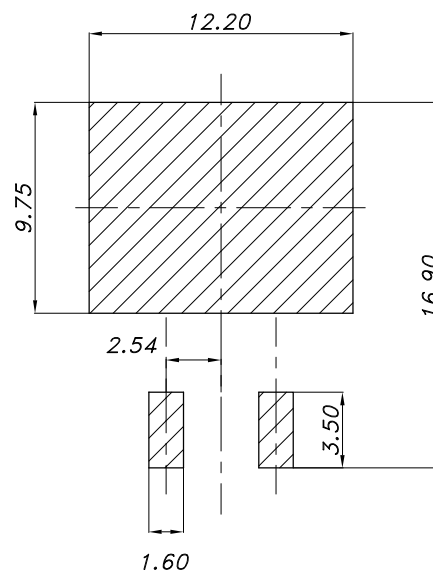


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Table 8. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

Figure 20. H²PAK-2 recommended footprint

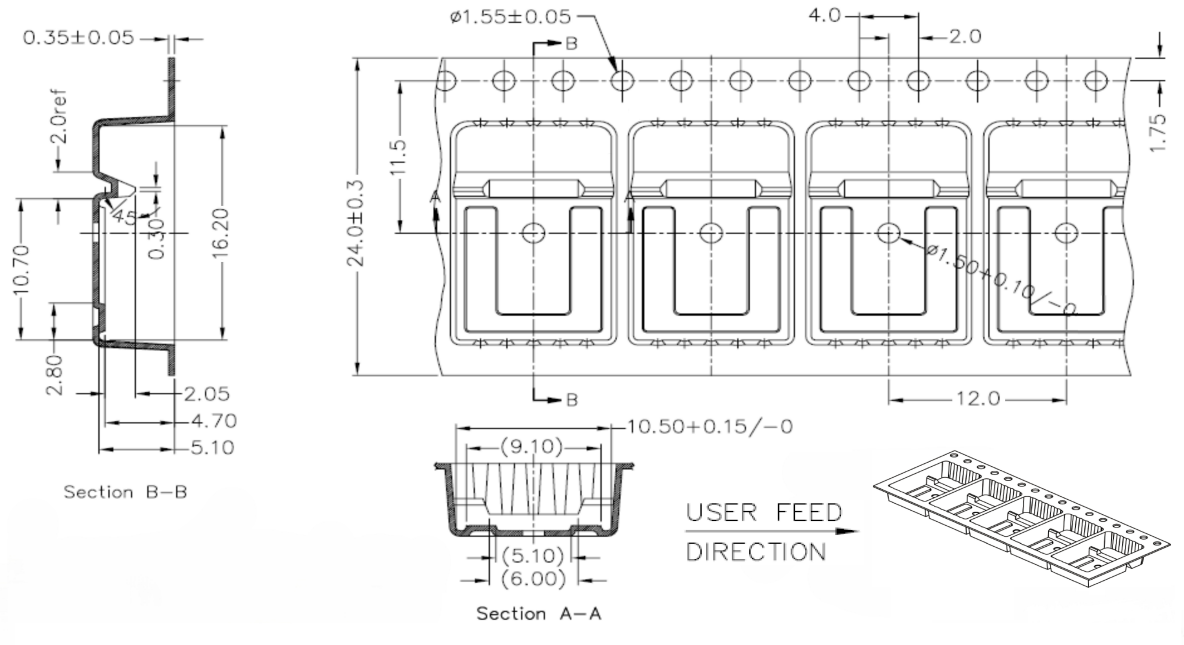


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Note: Dimensions are in mm.

4.2 H²PAK-2 packing information

Figure 21. H²PAK-2 tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Jan-2023	1	First release.
01-Mar-2023	2	Updated <i>Table 6. Switching times</i> .
22-Jun-2023	3	Updated <i>Table 5. Dynamic characteristics</i> , <i>Table 6. Switching times</i> and <i>Section 3 Test circuits</i> . Updated <i>Figure 7. Typical capacitance characteristics</i> . Minor text changes.
16-Aug-2023	4	Updated <i>Table 5. Dynamic characteristics</i> and <i>Table 7. Source-drain diode</i> . Updated <i>Figure 9. Normalized gate threshold vs temperature</i> , <i>Figure 11. Normalized breakdown voltage vs temperature</i> and <i>Figure 12. Typical reverse diode forward characteristics</i> .
02-Jul-2024	5	Updated <i>Features</i> on cover page. Minor text changes.
19-Aug-2025	6	Updated Section 4.2: H²PAK-2 packing information .

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