

Automotive-grade N-channel 40 V, 2.1 mΩ typ., 120 A STripFET™ F3 Power MOSFET in an I²PAK package

Datasheet - production data

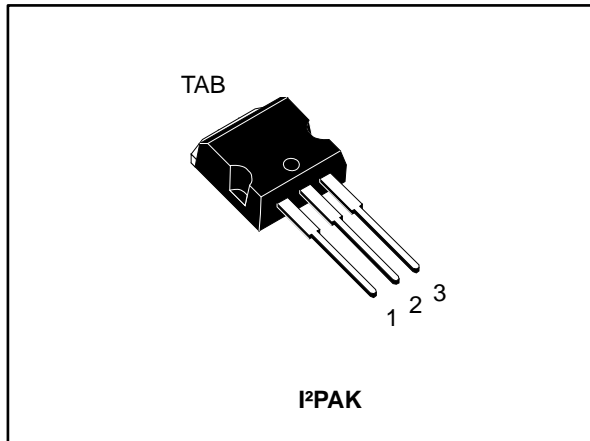
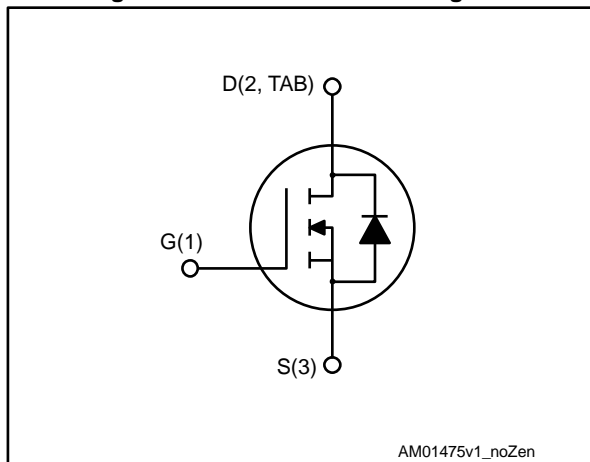


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STI270N4F3	40 V	2.6 mΩ	120 A	330 W



- AEC-Q101 qualified
- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STI270N4F3	270N4F3	I ² PAK	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	330	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	3.5	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	1	J
T_j	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

- (1) Current limited by package.
- (2) Pulse width limited by safe operating area.
- (3) $I_{SD} \leq 120\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
- (4) Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 80\text{ A}$, $V_{DD} = 32\text{ V}$.

Table 3: Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.45	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$,			10	μA
		$V_{DS} = 40\text{ V}$, $T_j = 125\text{ °C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$		2.1	2.6	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} ⁽¹⁾	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 80\text{ A}$	-	200	-	S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	7400	-	pF
C_{oss}	Output capacitance		-	1800	-	
C_{rss}	Reverse transfer capacitance		-	47	-	
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 160\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	110	150	nC
Q_{gs}	Gate-source charge		-	27	-	
Q_{gd}	Gate-drain charge		-	25	-	

Notes:

⁽¹⁾Pulsed: pulse duration=300 μs , duty cycle 1.5%.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 80\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	22	-	ns
t_r	Rise time		-	180	-	
$t_{d(off)}$	Turn-off delay time		-	110	-	
t_f	Fall time		-	45	-	

Table 7: Source-drain diode

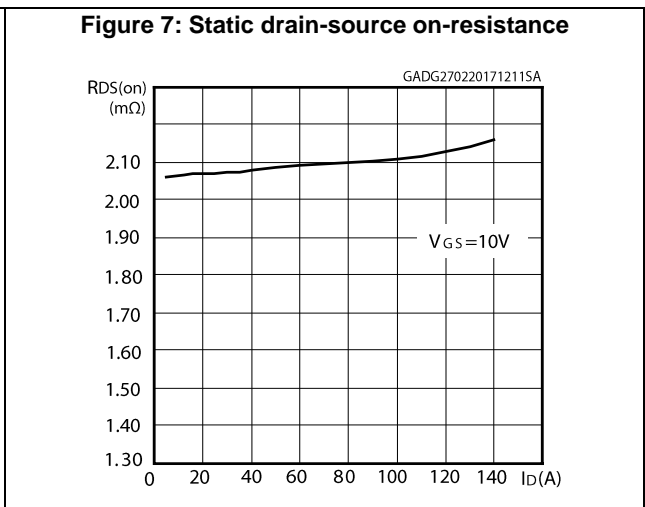
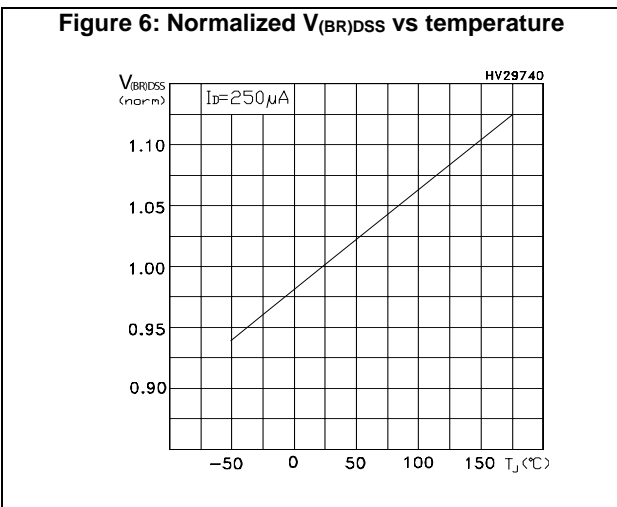
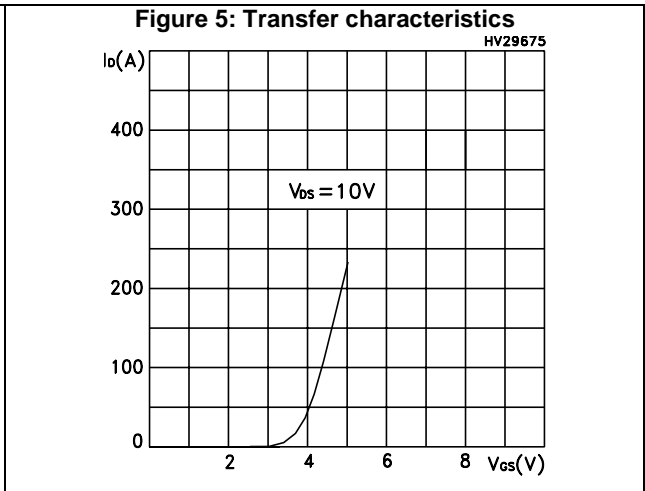
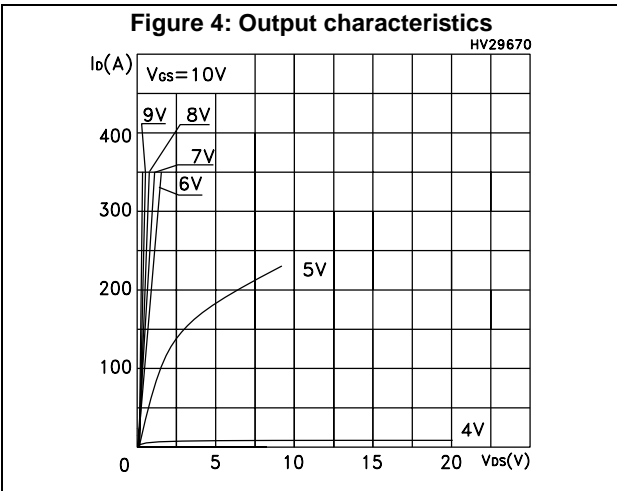
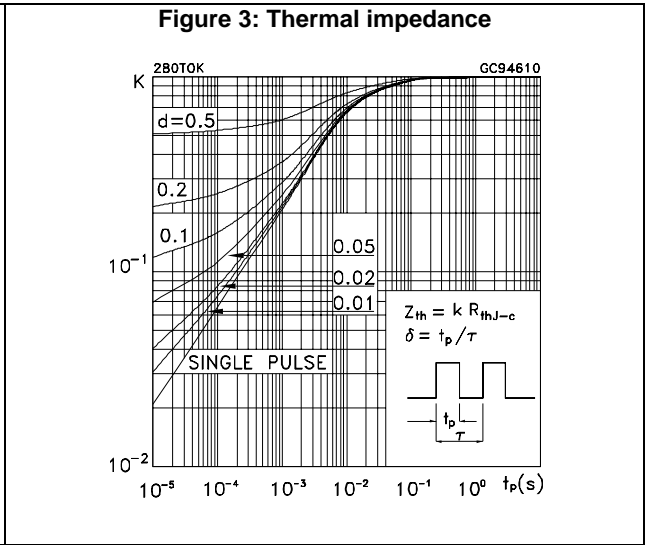
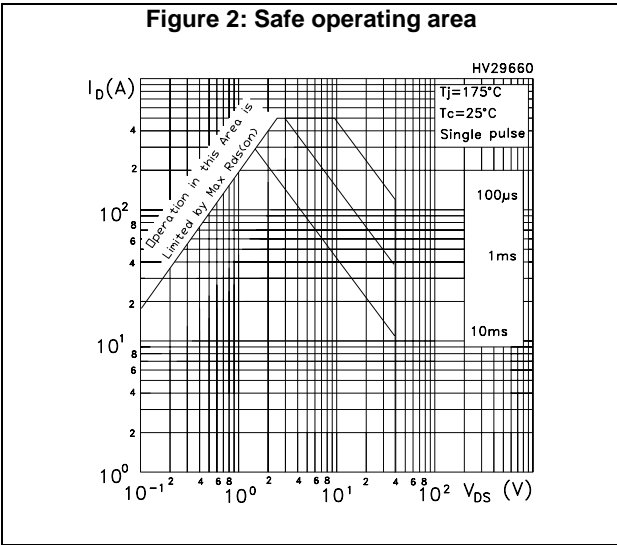
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{DS} = 80 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 160 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 32 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	70		ns
Q_{rr}	Reverse recovery charge		-	225		nC
I_{RRM}	Reverse recovery current		-	3.2		A

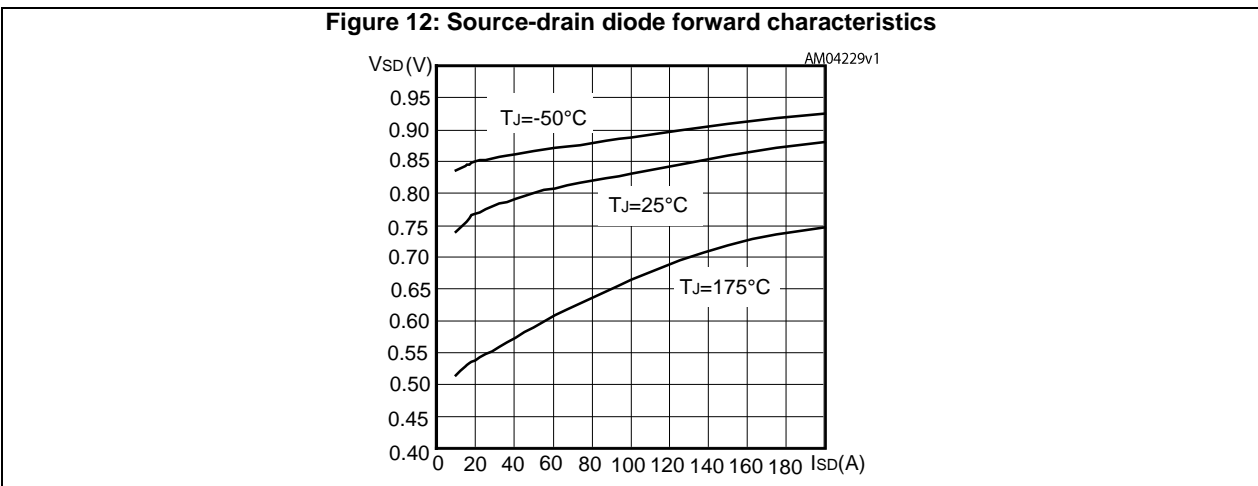
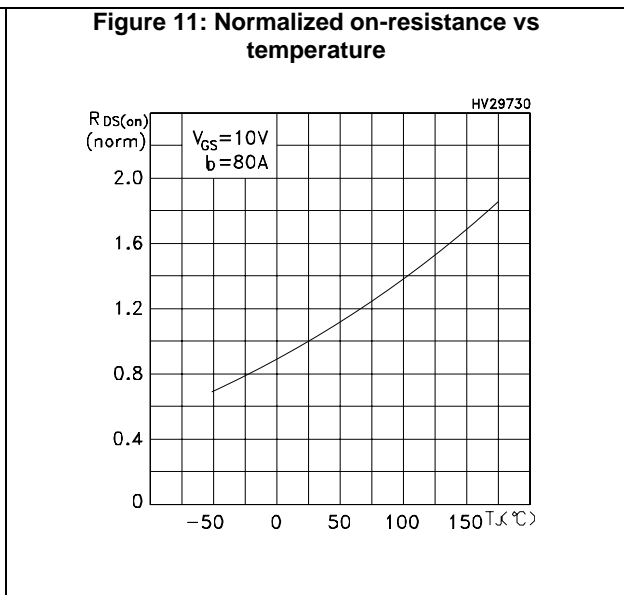
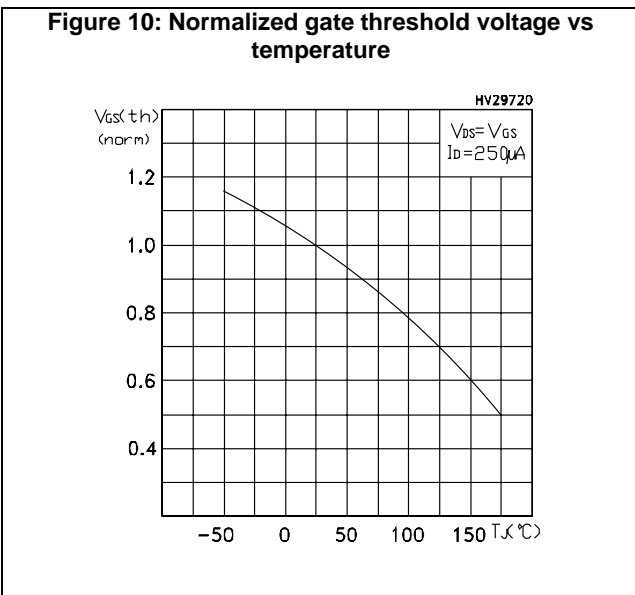
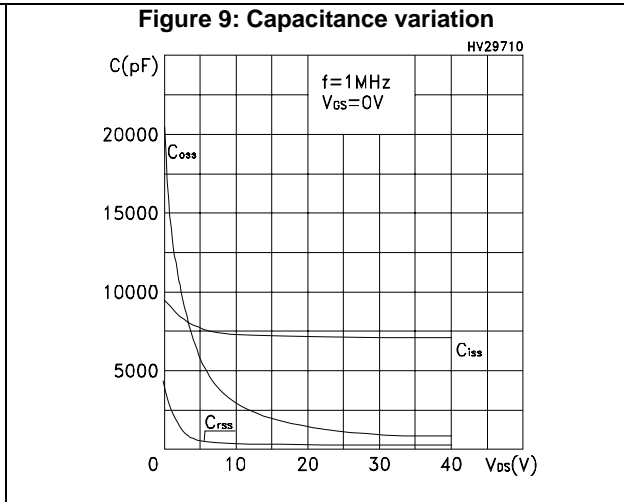
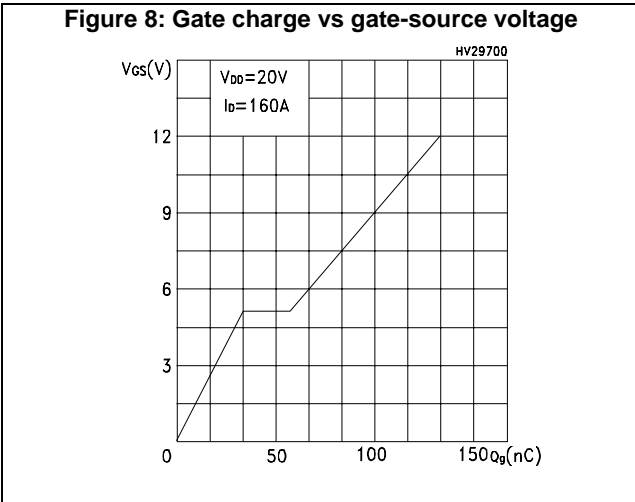
Notes:

⁽¹⁾Pulse width limited by safe operating area

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Test circuit for resistive load switching times



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Figure 14: Test circuit for gate charge behavior



AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



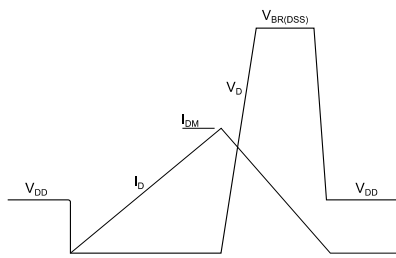
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Figure 16: Unclamped inductive load test circuit



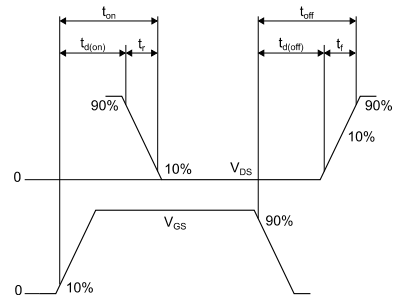
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 19: I²PAK package outline

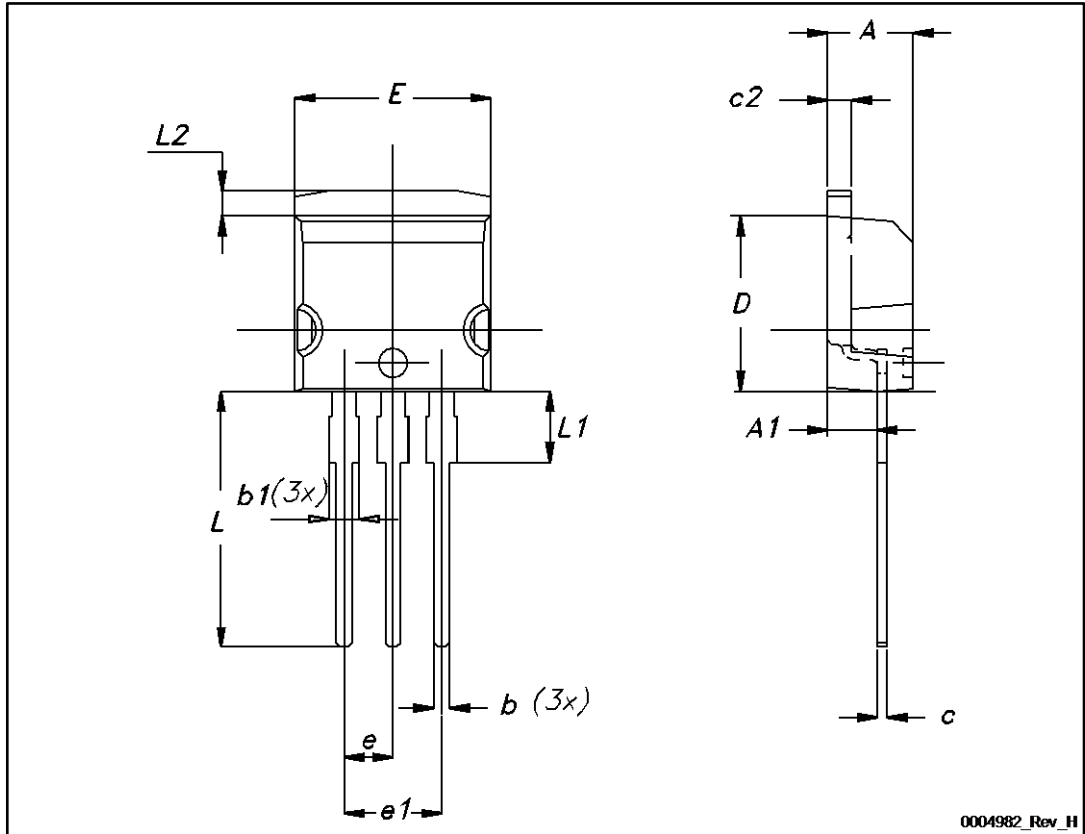


Table 8: I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
01-Mar-2017	1	First release.

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