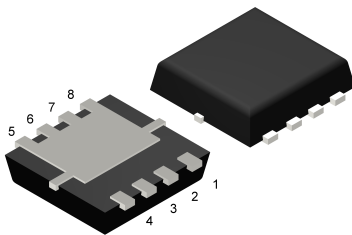
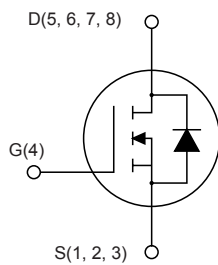


N-channel logic level 40 V, 2.3 mΩ max., 124 A, STripFET F8 Power MOSFET in a PowerFLAT 3.3x3.3 package



PowerFLAT 3.3x3.3



AM15810v1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL130N4LF8	40 V	2.3 mΩ	124 A

- MSL1 grade
- 150 °C operating temperature
- 100% avalanche tested
- Low gate charge Q_g

Applications

- Industrial tools, motor drives and equipment
- Industrial motor control
- Power supplies and converters

Description

The **STL130N4LF8** is a 40 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure. It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.



Product status link

[STL130N4LF8](#)

Product summary

Order code	STL130N4LF8
Marking	1304L
Package	PowerFLAT 3.3x3.3
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings (at $T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}^{(1)}$	124	A
	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}^{(2)}$	45	
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}^{(1)}$	78	
$I_{DM}^{(1)(3)(4)}$	Drain current (pulsed), $t_p = 10\text{ }\mu\text{s}$	496	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	64	W
I_{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	22	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 22\text{ A}$, $R_{Gmin} = 25\text{ }\Omega$)	290	mJ
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. This is the theoretical current value only related to the silicon.
2. This current value is limited by package.
3. Pulse width is limited by safe operating area.
4. Specified by design, not tested in production.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	18.8	$^{\circ}\text{C/W}$
R_{thJC}	Thermal resistance, junction-to-case	1.95	$^{\circ}\text{C/W}$

1. Defined according to JEDEC standards (JESD51-5, -7).

2 Electrical characteristics

($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	40	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾	-	-	100	
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	-	-	100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.2	-	2.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 22\text{ A}$	-	1.8	2.3	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 22\text{ A}$	-	2.5	3.3	
$R_G^{(1)}$	Gate resistance		-	0.7	-	Ω

1. Specified by design and evaluated by characterization, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}^{(1)}$	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2600	-	pF
$C_{oss}^{(1)}$	Output capacitance		-	680	-	pF
$C_{rss}^{(1)}$	Reverse transfer capacitance		-	18	-	pF
$Q_g^{(1)}$	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 22\text{ A}$, $V_{GS} = 0\text{ to }4.5\text{ V}$	-	16	-	nC
		$V_{DD} = 20\text{ V}$, $I_D = 22\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$	-	34.5	-	
$Q_{gs}^{(1)}$	Gate-source charge	$V_{DD} = 20\text{ V}$, $I_D = 22\text{ A}$, $V_{GS} = 0\text{ to }4.5\text{ V}$	-	7	-	nC
$Q_{gd}^{(1)}$	Gate-drain charge		-	3.5	-	
$Q_{g(sync)}^{(1)}$	Total gate charge, sync. MOSFET	$V_{DS} = 0.1\text{ V}$, $V_{GS} = 0\text{ to }4.5\text{ V}$	-	10	-	nC
$Q_{oss}^{(1)}$	Output charge	$V_{DD} = 25\text{ V}$, $V_{GS} = 0\text{ V}$	-	39	-	nC

1. Specified by design and evaluated by characterization, not tested in production.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	8.4	-	ns
$t_r^{(1)}$	Rise time		-	2.95	-	ns
$t_{d(off)}^{(1)}$	Turn-off delay time		-	27.6	-	ns
$t_f^{(1)}$	Fall time		-	3.96	-	ns

1. Specified by design and evaluated by characterization, not tested in production.

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)(2)}$	Forward on current (continuous)	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	80	A
V_{SD}	Forward on voltage	$I_{SD} = 22\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1	V
$t_{rr}^{(1)}$	Reverse recovery time	$I_D = 22\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 24\text{ V}$	-	36	-	ns
$Q_{rr}^{(1)}$	Reverse recovery charge		-	26	-	nC
$I_{RRM}^{(1)}$	Reverse recovery current		-	1.46	-	A

1. This is the theoretical current value only related to the silicon.
2. Specified by design and evaluated by characterization, not tested in production.

2.1 Electrical characteristics (curves)

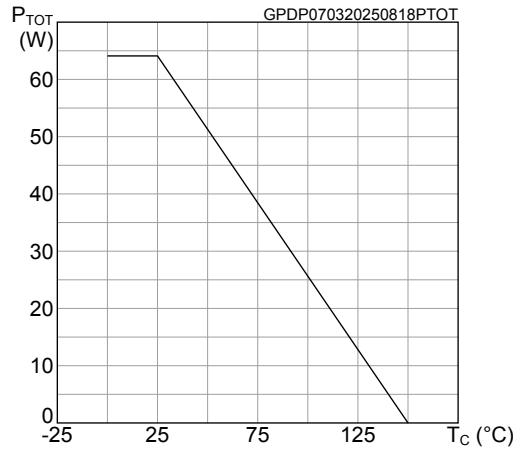
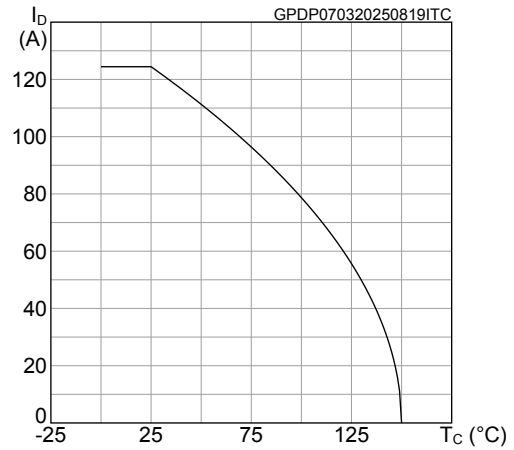
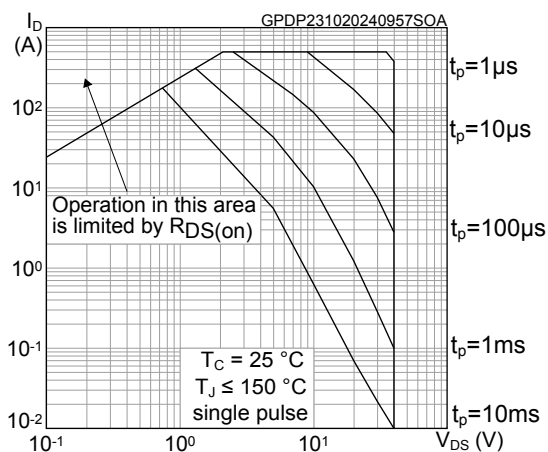
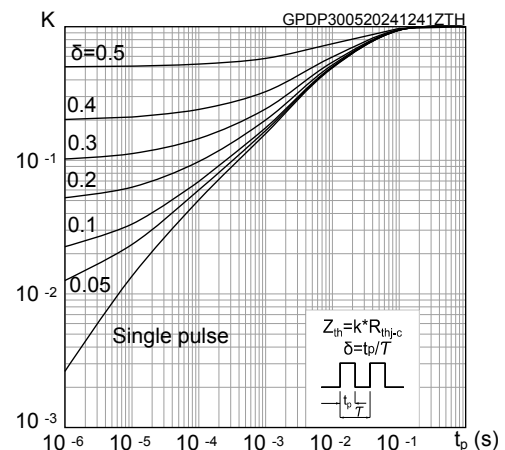
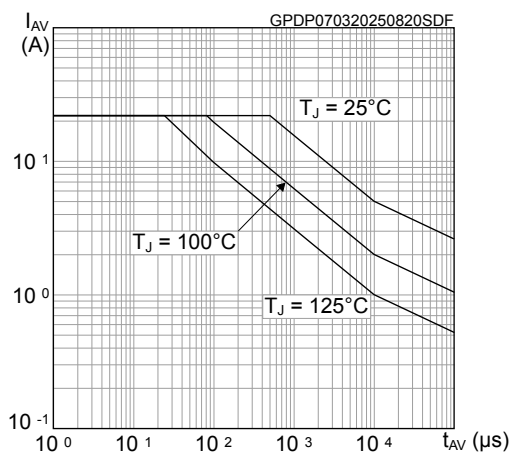
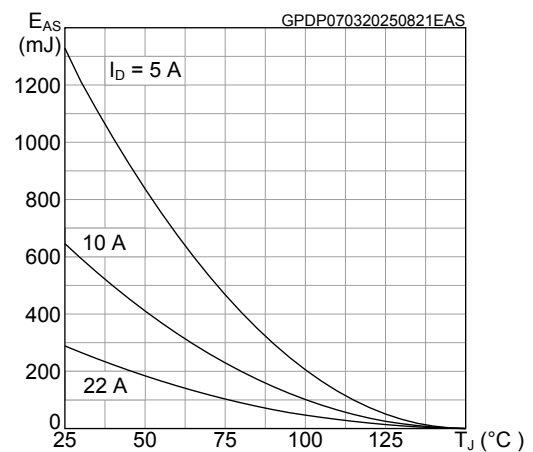
Figure 1. Total power dissipation

Figure 2. Drain current vs case temperature

Figure 3. Safe operating area

Figure 4. Normalized transient thermal impedance

Figure 5. Avalanche characteristics

Figure 6. Avalanche energy


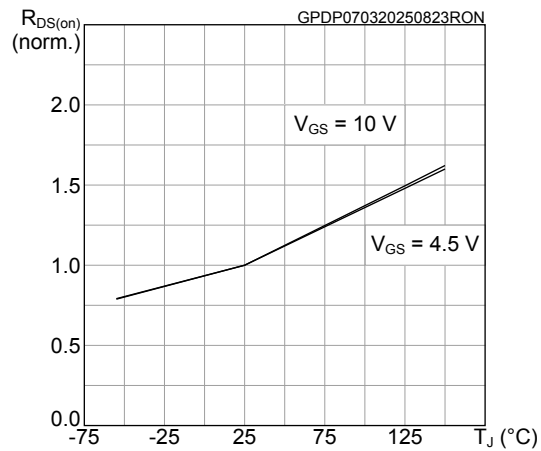
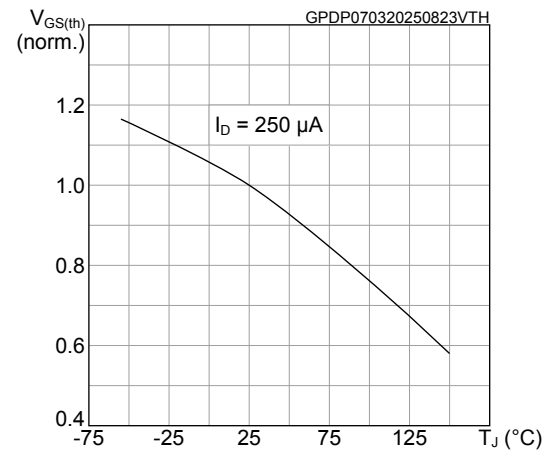
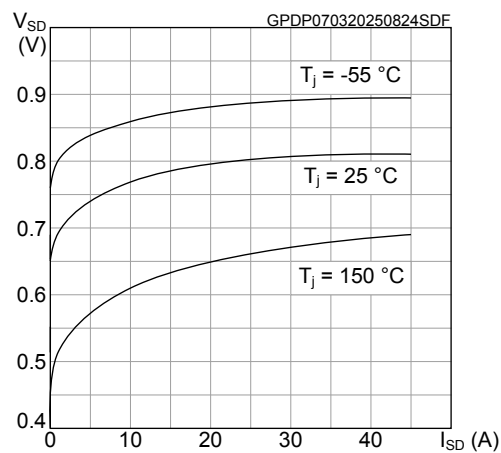
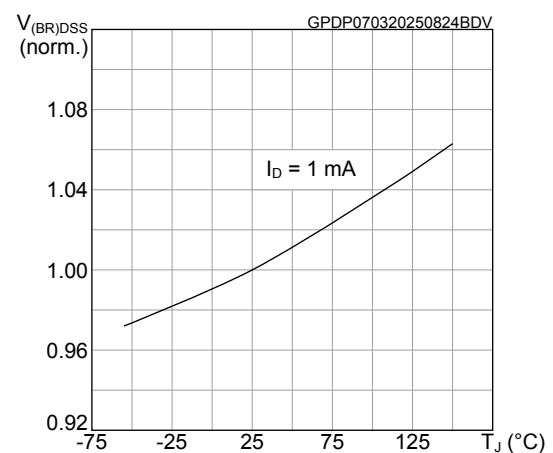
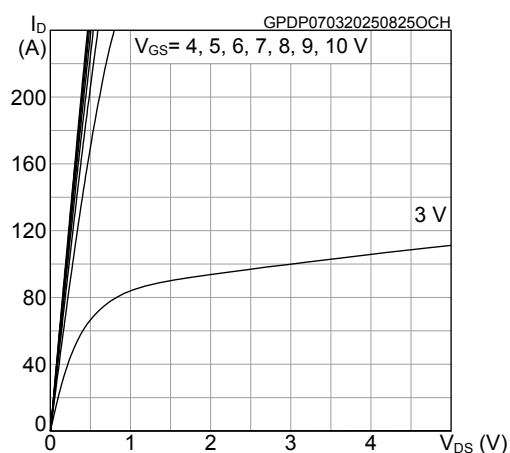
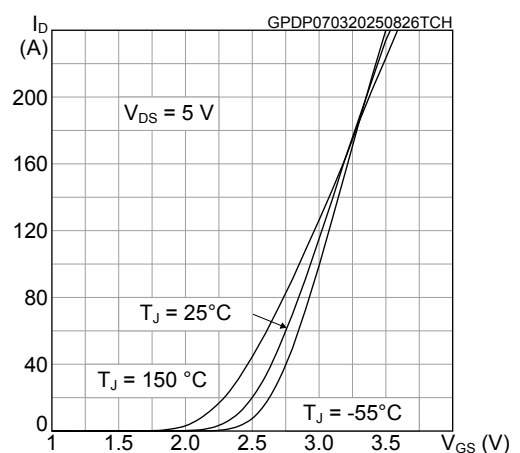
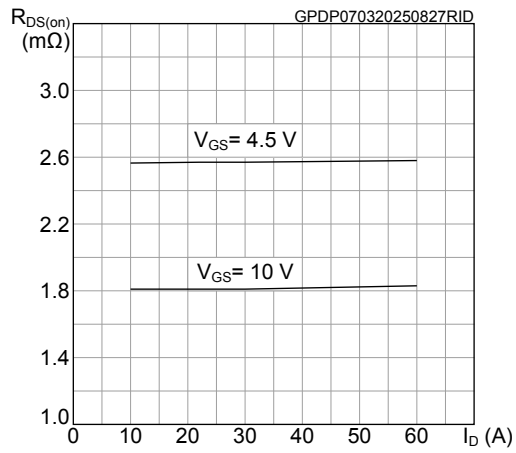
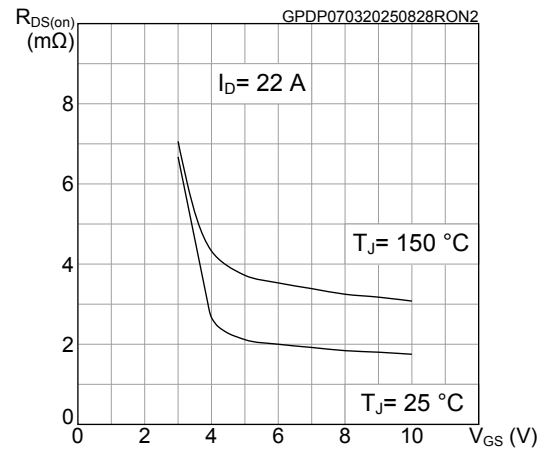
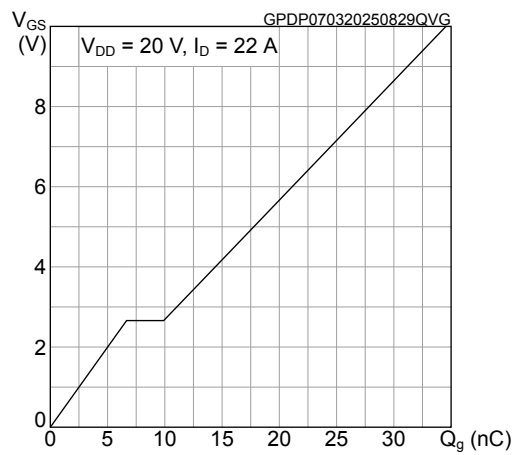
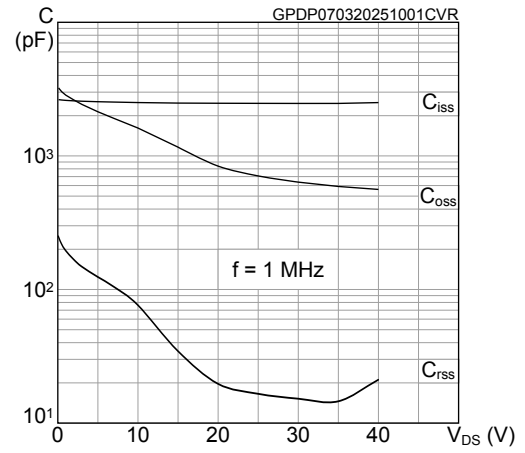
Figure 7. Normalized on-resistance vs temperature

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Typical reverse diode forward characteristics

Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

Figure 11. Typical output characteristics

Figure 12. Typical transfer characteristics


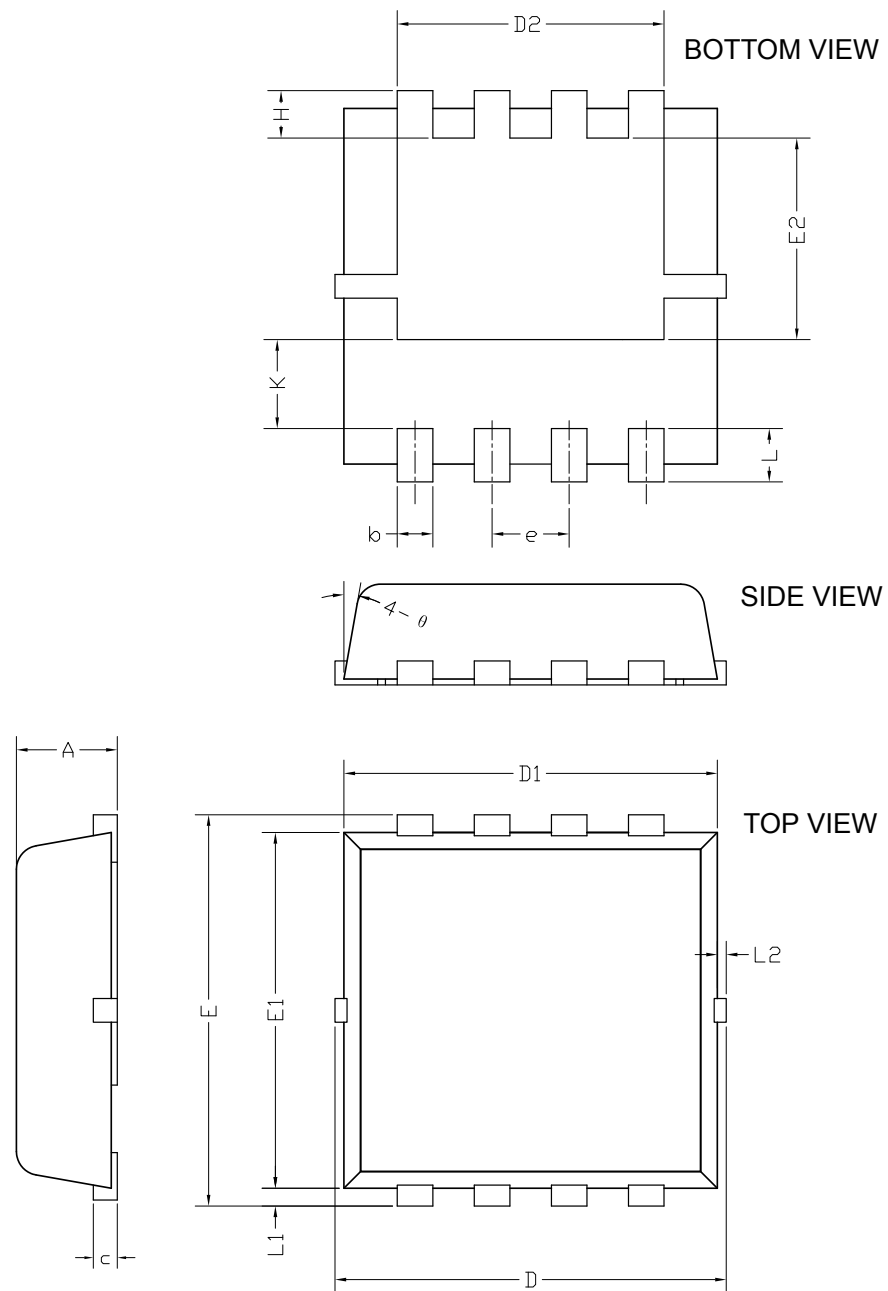
Figure 13. Typical drain-source on-resistance

Figure 14. Typical on-resistance vs gate-source voltage

Figure 15. Typical gate charge characteristics

Figure 16. Typical capacitance characteristics


3 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 PowerFLAT 3.3x3.3 package information

Figure 17. PowerFLAT 3.3x3.3 package outline



8465286_2

Table 7. PowerFLAT 3.3x3.3 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Technical drawing of a mechanical part, likely a bracket or support, showing dimensions in inches. The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 3.800
- Overall height: 2.400
- Distance from left edge to centerline: 0.53 (x2)
- Distance from centerline to right edge: 2.45
- Distance from top edge to centerline: 1.700
- Distance from centerline to right edge (bottom): 0.40 (x2)
- Distance from bottom edge to centerline: 0.65
- Distance from left edge to centerline (bottom): 0.25 MIN
- Distance from centerline to right edge (bottom): 0.65
- Distance from right edge to centerline (bottom): 0.40 MAX

Side View Dimensions:

- Overall height: 0.75
- Distance from top edge to centerline: 0.25 MIN
- Distance from centerline to right edge: 0.65
- Distance from right edge to centerline: 0.40 MAX

The drawing shows a central rectangular area with diagonal hatching, indicating a specific material or finish. The dimensions are provided in inches, and the drawing is labeled with a part number 8465286.

Revision history

Table 8. Document revision history

Date	Version	Changes
04-Dec-2023	1	Initial release.
04-Jun-2024	2	Updated "applications" in cover page, <i>Section 1: Electrical ratings</i> and <i>Section 2: Electrical characteristics</i> . Added <i>Section 2.1: Electrical characteristics (curves)</i> . Minor text changes.
25-Sep-2024	3	Updated <i>Section Features</i> on cover page. Updated <i>Table 6. Source-drain diode</i> and <i>Section 2.1: Electrical characteristics (curves)</i> .
19-Nov-2024	4	Updated <i>Figure 3. Safe operating area</i> .
14-Apr-2025	5	Updated <i>Figure 1. Total power dissipation</i> , <i>Figure 2. Drain current vs case temperature</i> , <i>Figure 5. Avalanche characteristics</i> , <i>Figure 6. Avalanche energy</i> , <i>Figure 7. Normalized on-resistance vs temperature</i> , <i>Figure 8. Normalized gate threshold voltage vs temperature</i> , <i>Figure 9. Typical reverse diode forward characteristics</i> , <i>Figure 10. Normalized $V_{(BR)DSS}$ vs temperature</i> , <i>Figure 11. Typical output characteristics</i> , <i>Figure 12. Typical transfer characteristics</i> , <i>Figure 13. Typical drain-source on-resistance</i> , <i>Figure 14. Typical on-resistance vs gate-source voltage</i> , <i>Figure 15. Typical gate charge characteristics</i> and <i>Figure 16. Typical capacitance characteristics</i> . Minor text changes in <i>Table 1. Absolute maximum ratings</i> (at $T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise specified).

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves)	5
3	Package information.....	8
3.1	PowerFLAT 3.3x3.3 package information	8
	Revision history	11

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved