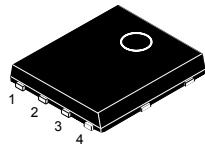
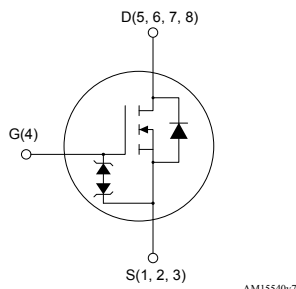


## N-channel 600 V, 295 mΩ typ., 8.5 A, MDmesh DM6 Power MOSFET in a PowerFLAT 5x6 HV package



PowerFLAT 5x6 HV



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STL15N60DM6	600 V	372 mΩ	8.5 A	64 W

- Fast-recovery body diode
- Lower  $R_{DS(on)}$  per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge ( $Q_{rr}$ ), recovery time ( $t_{rr}$ ) and excellent improvement in  $R_{DS(on)}$  per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.



#### Product status link

[STL15N60DM6](#)

#### Product summary

<b>Order code</b>	STL15N60DM6
<b>Marking</b>	15N60DM6
<b>Package</b>	PowerFLAT™ 5x6 HV
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	8.5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	64	W
$I_{AR}^{(2)}$	Avalanche current, repetitive or not repetitive	3	A
$E_{AS}^{(3)}$	Single pulse avalanche energy	240	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(4)}$	Peak diode recovery current slope	1000	A/ $\mu\text{s}$
$dv/dt^{(5)}$	MOSFET $dv/dt$ ruggedness	100	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. Pulse width limited by  $T_J$  max.
3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .
4.  $I_{SD} \leq 8.5\text{ A}$ ,  $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
5.  $V_{DS} \leq 480\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.96	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.8\text{ A}$		295	372	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	607	-	$\text{pF}$
$C_{oss}$	Output capacitance		-	40	-	
$C_{rss}$	Reverse transfer capacitance		-	4	-	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	100	-	$\text{pF}$
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	5.7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 12\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	15.3	-	$\text{nC}$
$Q_{gs}$	Gate-source charge		-	4.1	-	
$Q_{gd}$	Gate-drain charge		-	7.7	-	

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 6\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	8.8	-	$\text{ns}$
$t_r$	Rise time		-	7.4	-	
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	29.2	-	
$t_f$	Fall time		-	7.2	-	

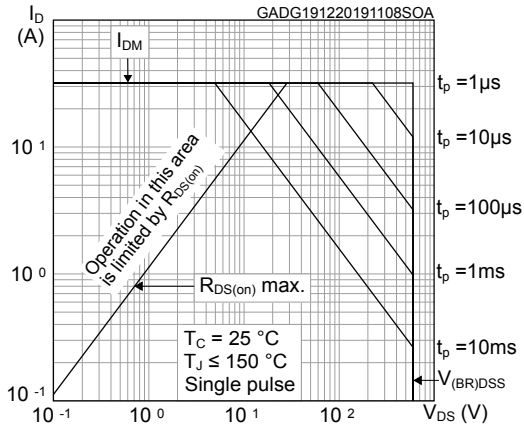
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 8.5\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	85		ns
$Q_{rr}$	Reverse recovery charge		-	0.268		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	6.3		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	147		ns
$Q_{rr}$	Reverse recovery charge		-	0.661		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	9		A

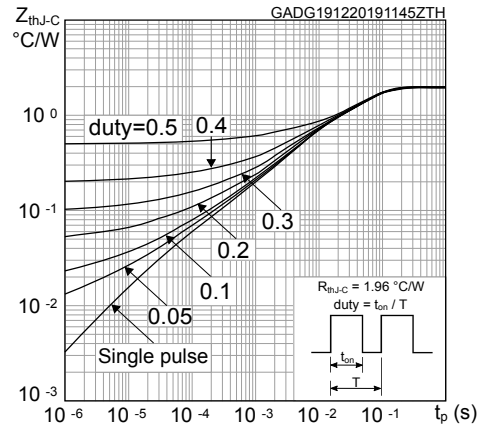
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

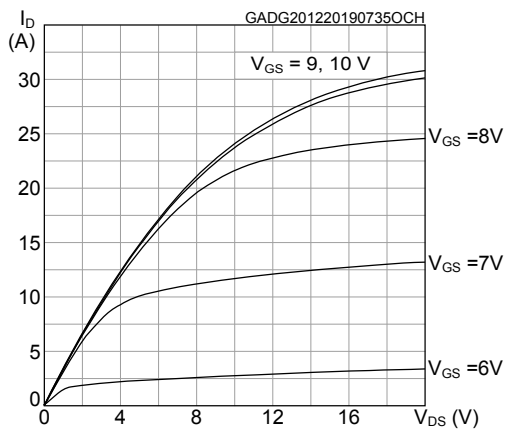
**Figure 1. Safe operating area**



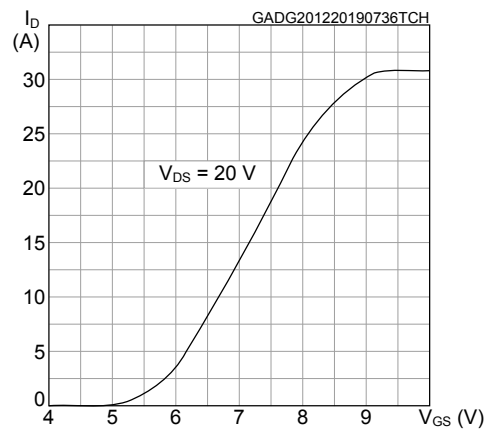
**Figure 2. Maximum transient thermal impedance**



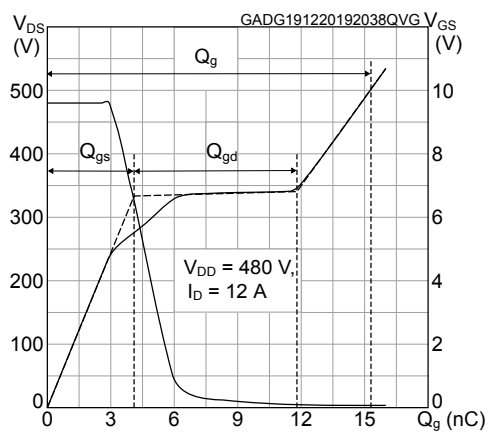
**Figure 3. Typical output characteristics**



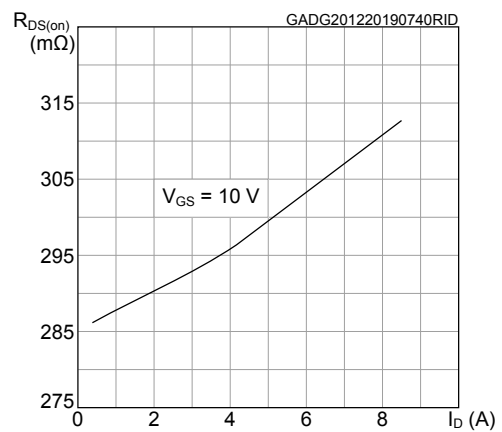
**Figure 4. Typical transfer characteristics**



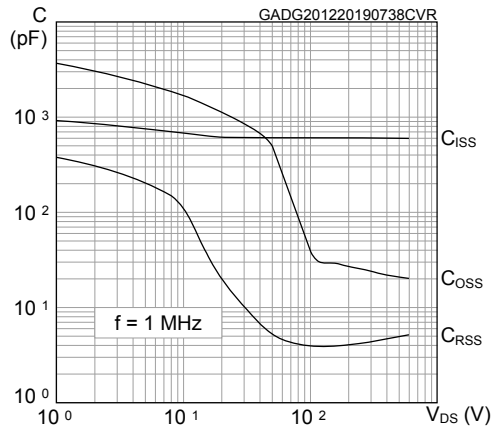
**Figure 5. Typical gate charge characteristics**



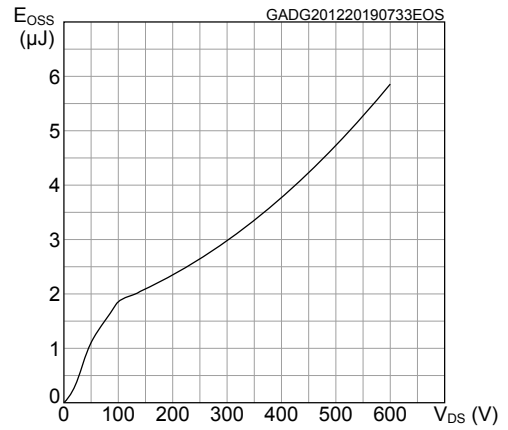
**Figure 6. Typical drain-source on-resistance**



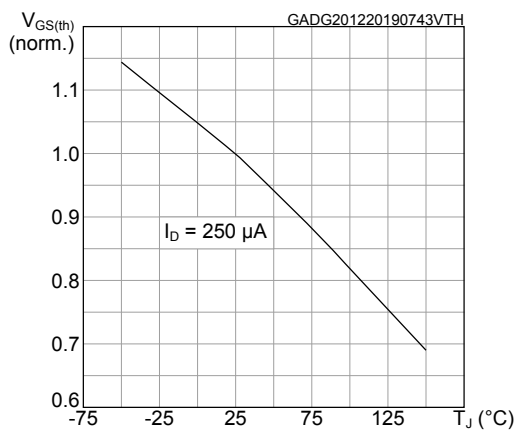
**Figure 7. Typical capacitance characteristics**



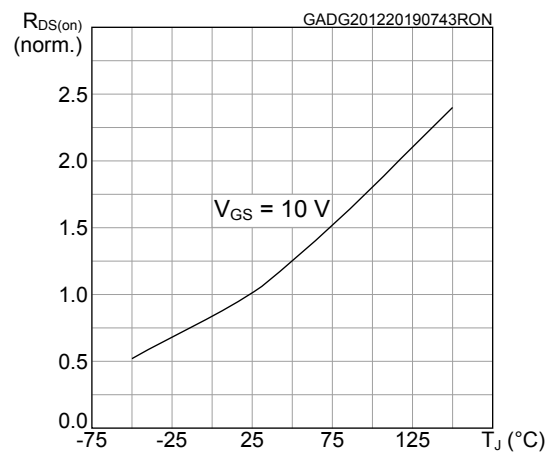
**Figure 8. Typical output capacitance stored energy**



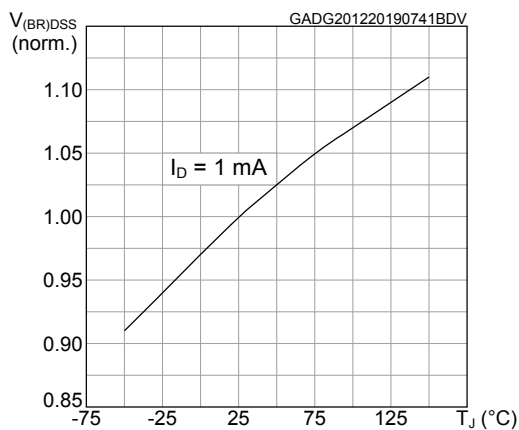
**Figure 9. Normalized gate threshold vs temperature**



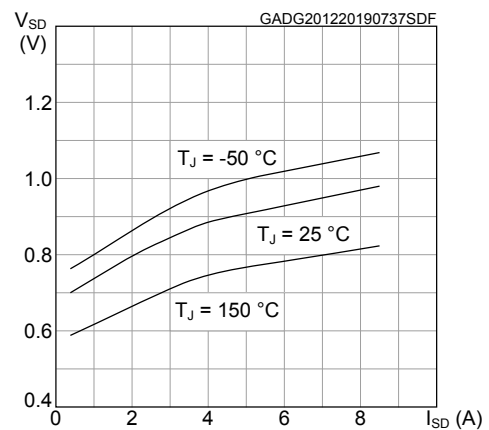
**Figure 10. Normalized on-resistance vs temperature**



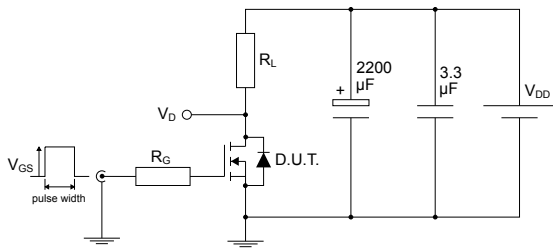
**Figure 11. Normalized breakdown voltage vs temperature**



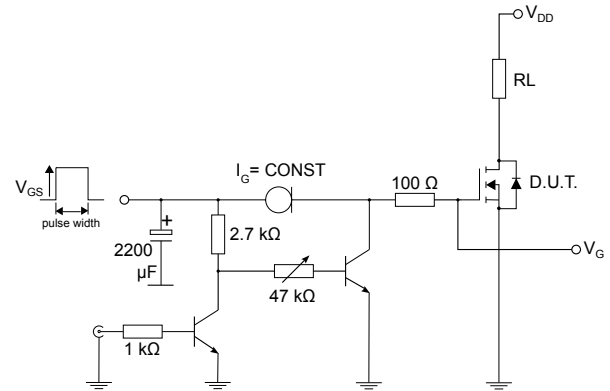
**Figure 12. Typical reverse diode forward characteristics**



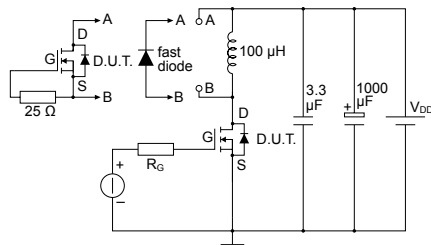
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


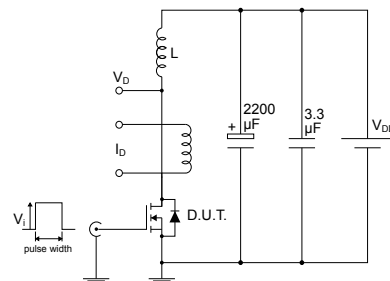
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


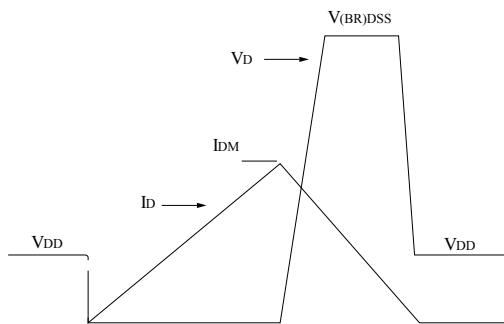
AM01469v10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


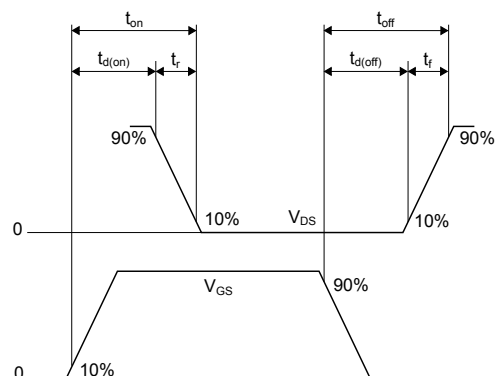
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

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## 4 Package information

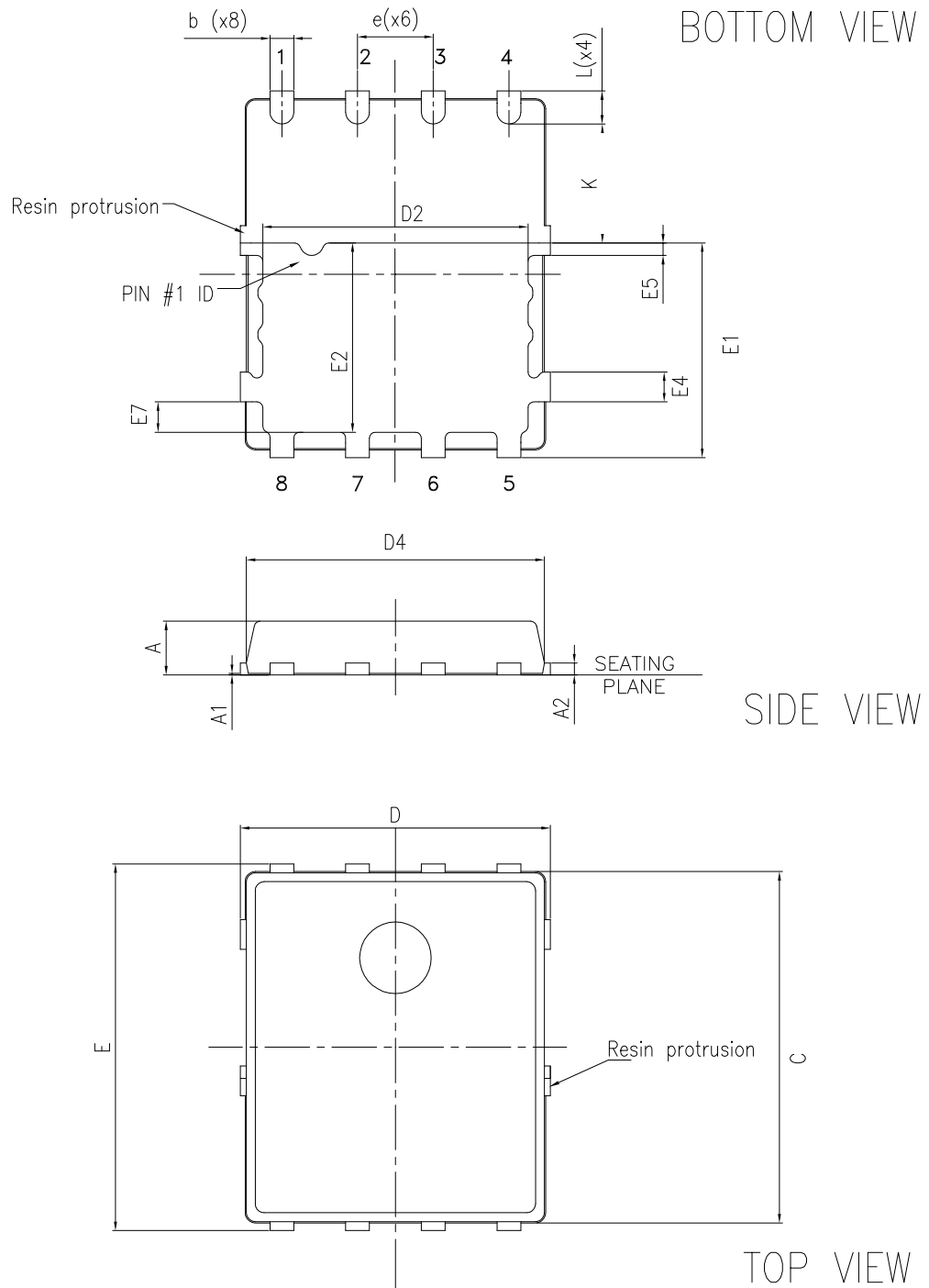
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



### 4.1 PowerFLAT 5x6 HV package information

Figure 19. PowerFLAT 5x6 HV package outline

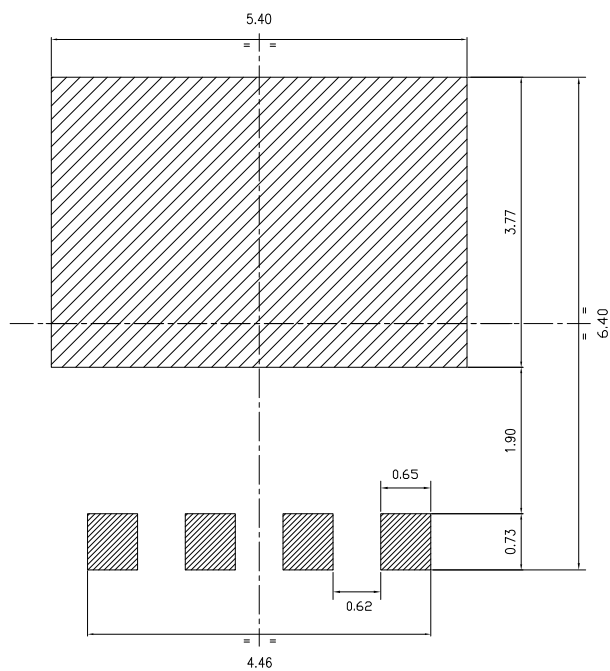


8368143\_Rev\_4

**Table 7. PowerFLAT 5x6 HV mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

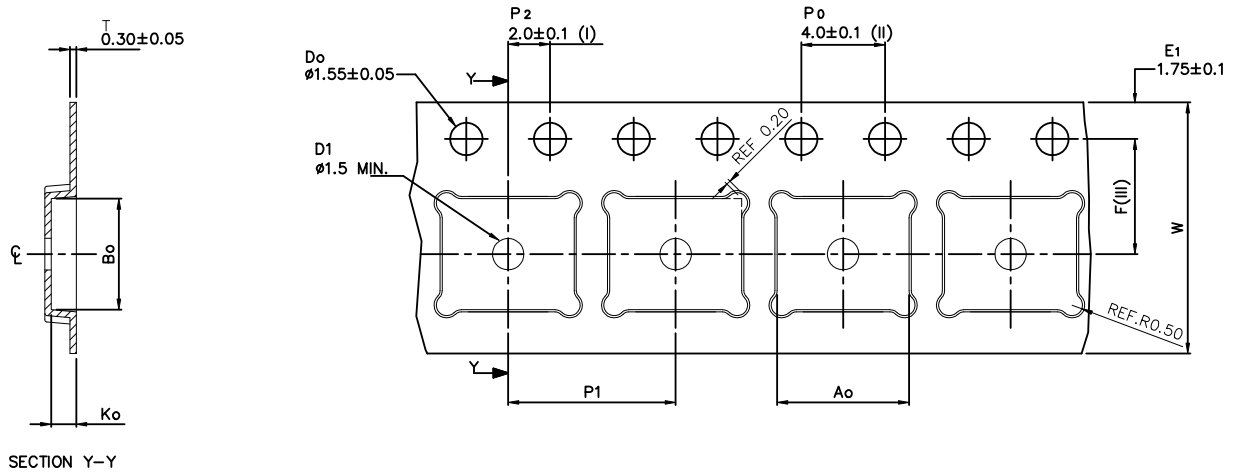
**Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)**



8368143\_Rev\_4\_footprint

## 4.2 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



A <sub>0</sub>	6.30 +/- 0.1
B <sub>0</sub>	5.30 +/- 0.1
K <sub>0</sub>	1.20 +/- 0.1
F	5.50 +/- 0.1
P <sub>1</sub>	8.00 +/- 0.1
W	12.00 +/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

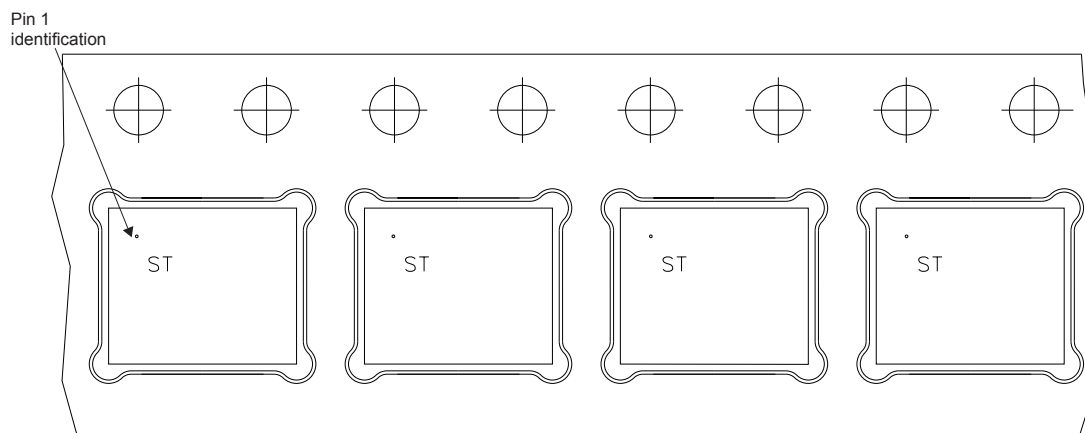
(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

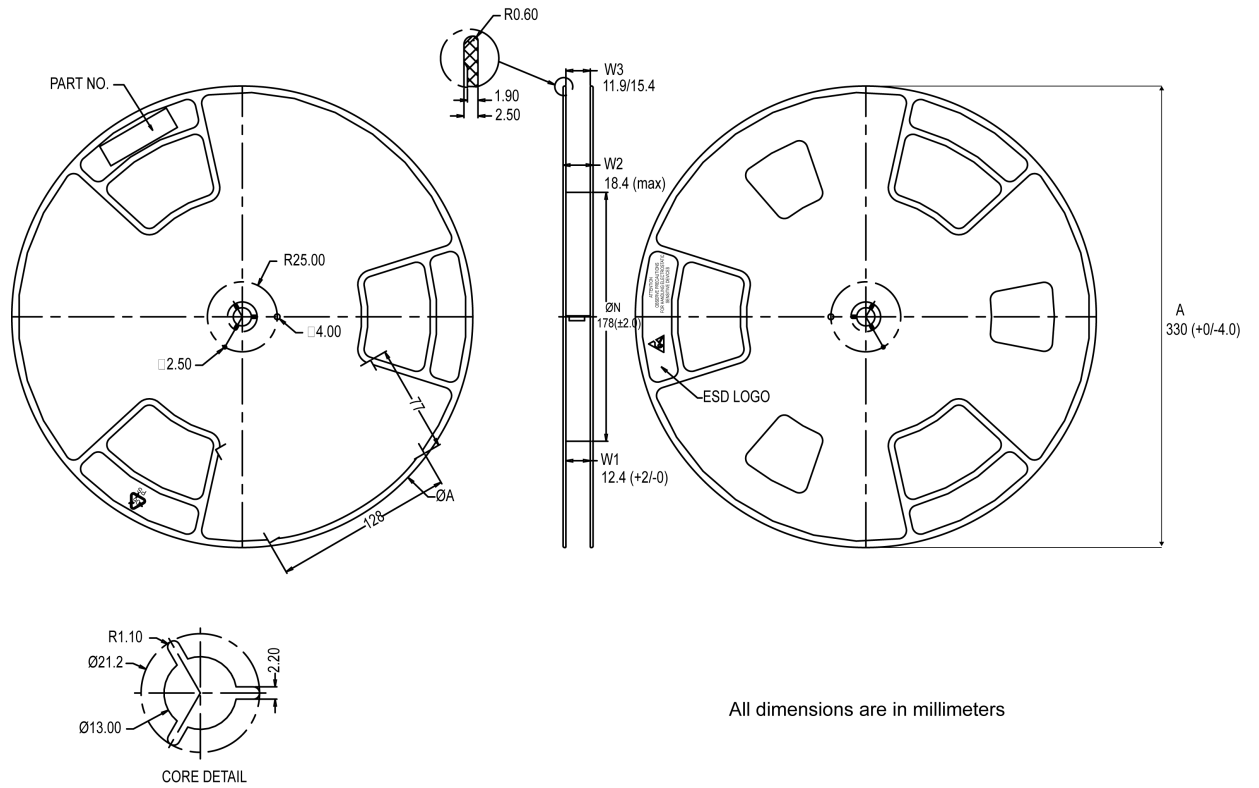
Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

8234350\_Tape\_rev\_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape



**Figure 23. PowerFLAT 5x6 reel**



All dimensions are in millimeters

8234350\_Reel\_rev\_C

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
07-Jan-2020	1	First release.
03-Jul-2020	2	Updated Table 1. Absolute maximum ratings.

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