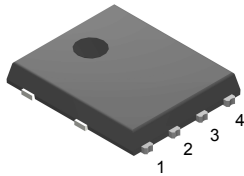
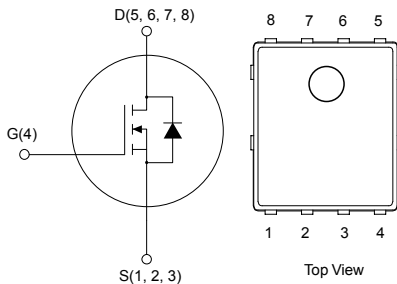


Automotive-grade N-channel 30 V, 23 mΩ typ., 10 A, STripFET™ H6 Power MOSFET in a PowerFLAT 5x6 package


PowerFLAT™ 5x6


NG405678S123



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL19N3LLH6AG	30 V	33 mΩ	10 A	50 W

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Product status link

[STL19N3LLH6AG](#)

Product summary

Order code	STL19N3LLH6AG
Marking	19N3LLH6
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	10	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	10	
$I_{DM}^{(2)}$	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	50	W
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature range		

1. Current limited by package. At $T_{case} = 25\text{ }^\circ\text{C}$ the silicon is able to sustain 30 A.
2. Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

1. When mounted on an 1-inch² FR-4, 2 Oz copper board, $t < 10\text{ s}$.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AV}^{(1)}$	Avalanche current, repetitive or not repetitive	10	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	130	mJ

1. Pulse width limited by T_{jmax}
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 25\text{ V}$

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 5\text{ A}$		23	33	m Ω
		$V_{\text{GS}} = 4.5\text{ V}$, $I_{\text{D}} = 5\text{ A}$		33	43	

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	321	-	pF
C_{oss}	Output capacitance		-	68	-	
C_{rss}	Reverse transfer capacitance		-	34	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 10\text{ A}$, $V_{\text{GS}} = 0\text{ to }4.5\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	3.7	-	nC
Q_{gs}	Gate-source charge		-	1	-	
Q_{gd}	Gate-drain charge		-	1.7	-	

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 5\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	2.4	-	ns
t_{r}	Rise time		-	2.5	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	12.8	-	
t_{f}	Fall time		-	2.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
$I_{\text{SDM}}^{(1)}$	Source-drain current (pulsed)		-		40	A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 10\text{ A}$	-		1.12	V
t_{rr}	Reverse recovery time	$I_{SD} = 1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 24\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	15.1		ns
Q_{rr}	Reverse recovery charge		-	7.5		nC
I_{RRM}	Reverse recovery current		-	1		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

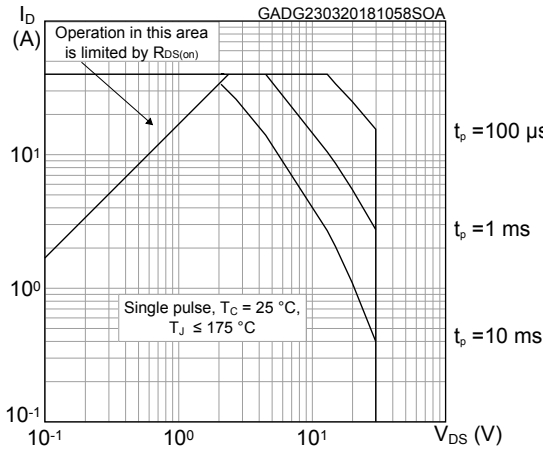


Figure 2. Thermal impedance

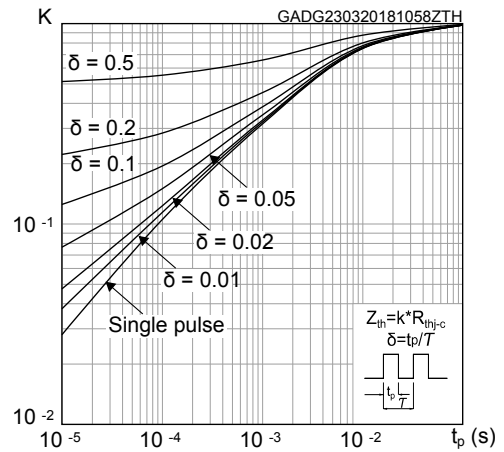


Figure 3. Output characteristics

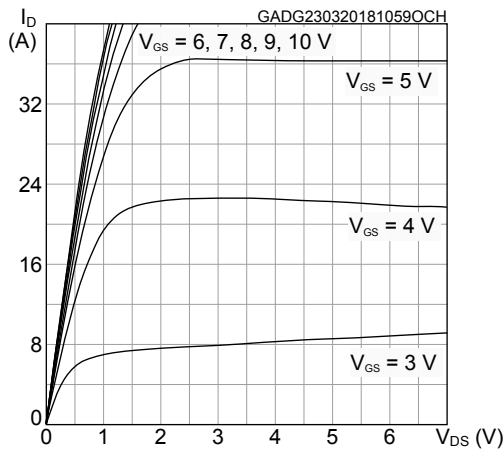


Figure 4. Transfer characteristics

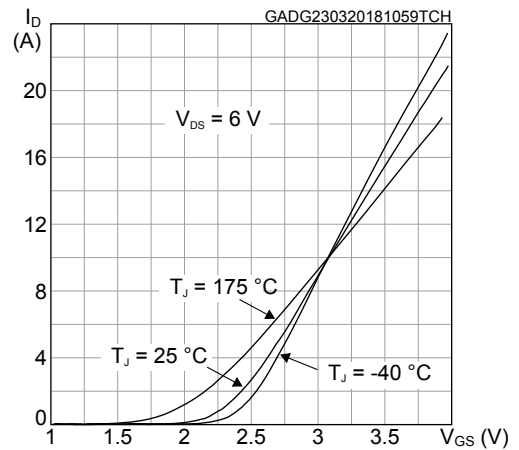


Figure 5. Gate charge vs gate-source voltage

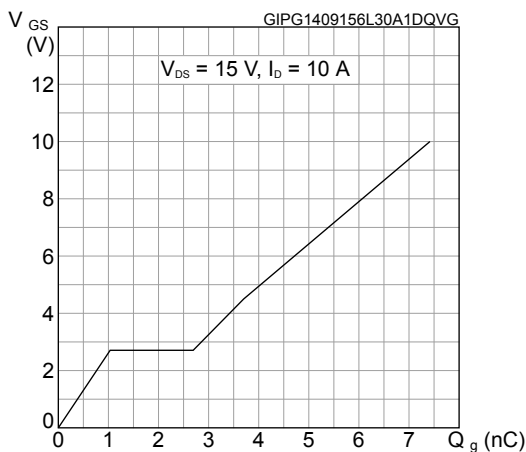


Figure 6. Static drain-source on-resistance

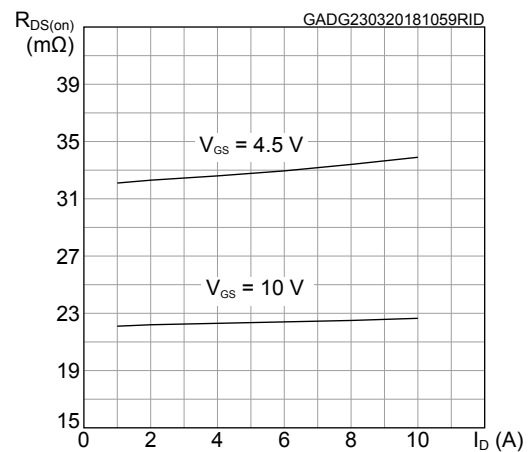


Figure 7. Capacitance variations

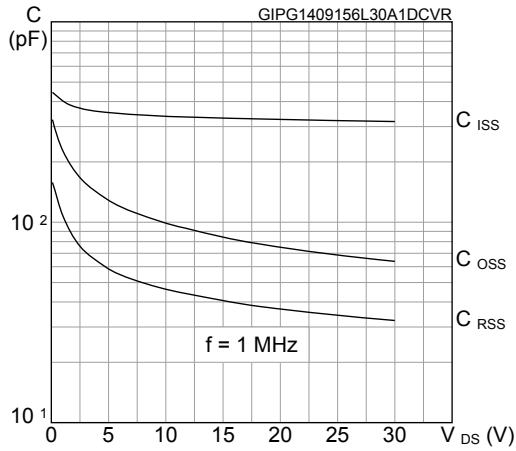


Figure 8. Normalized gate threshold voltage vs temperature

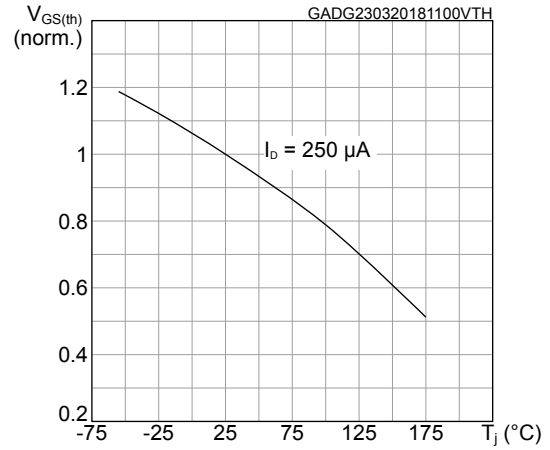


Figure 9. Normalized on-resistance vs temperature

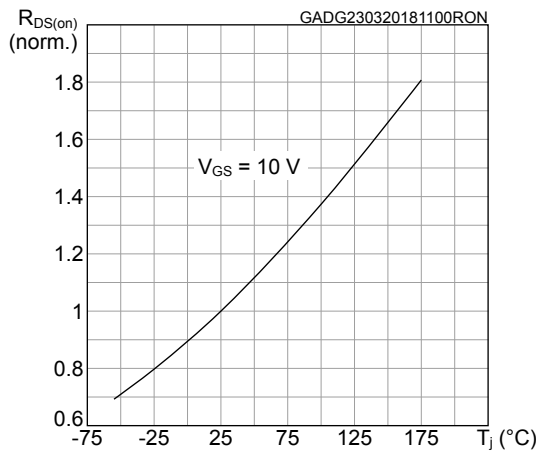


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

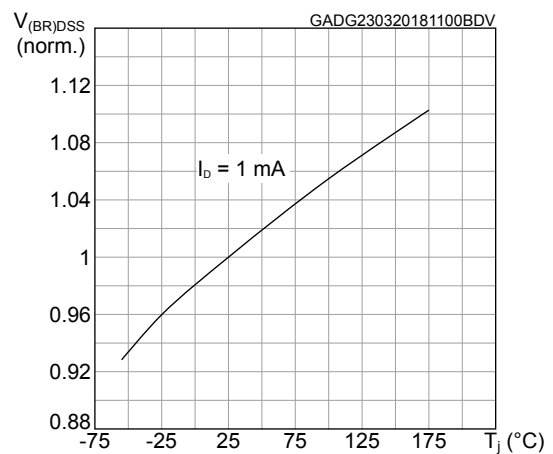
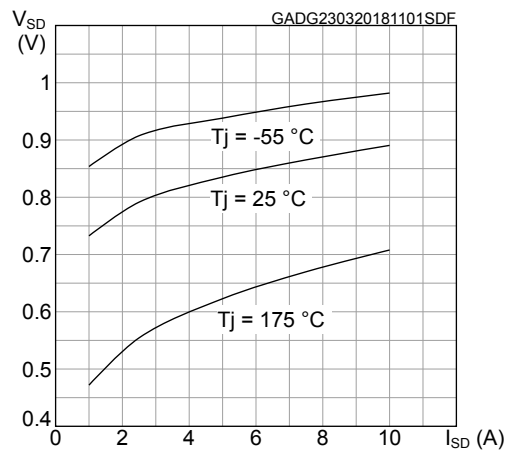
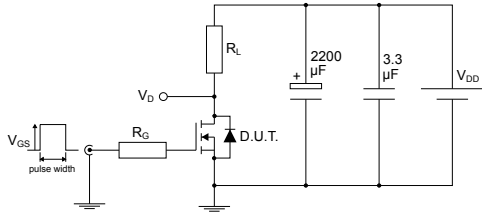


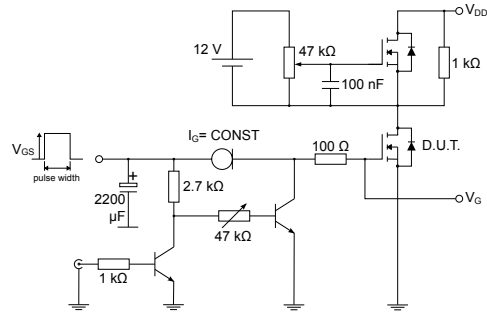
Figure 11. Source-drain diode forward characteristics



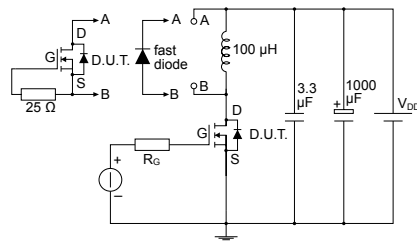
3 Test circuits

Figure 12. Test circuit for resistive load switching times


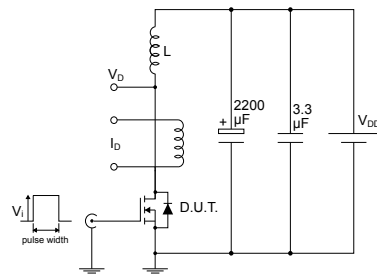
AM01468v1

Figure 13. Test circuit for gate charge behavior


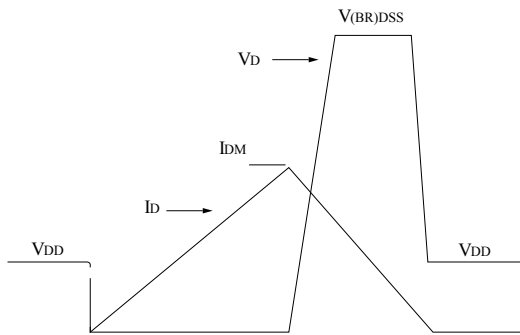
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Figure 14. Test circuit for inductive load switching and diode recovery times


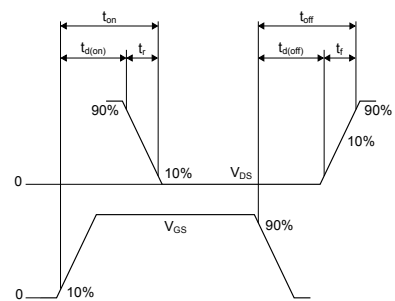
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform


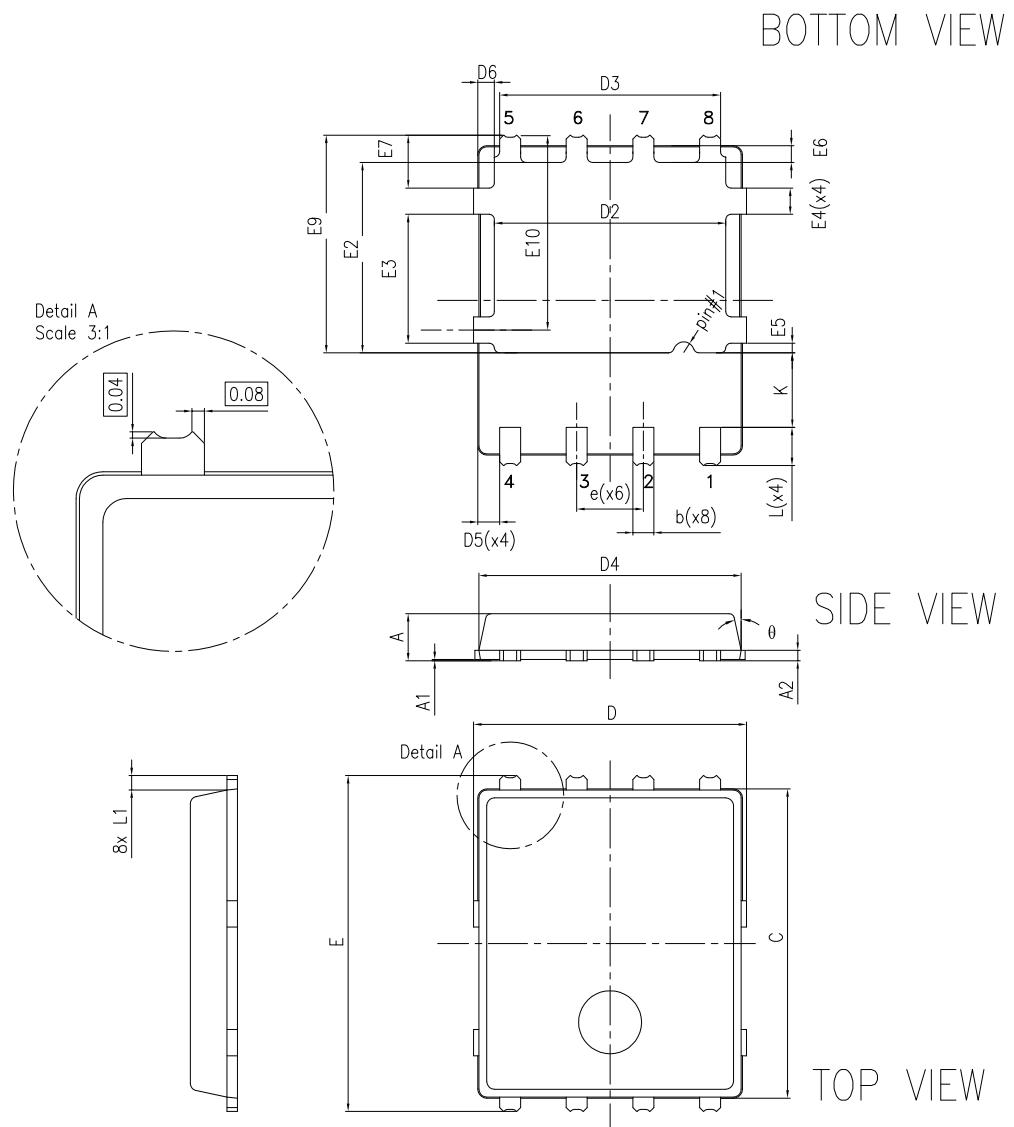
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 18. PowerFLAT™ 5x6 WF type R package outline



8231817_R_WF_Rev_15

Table 8. PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

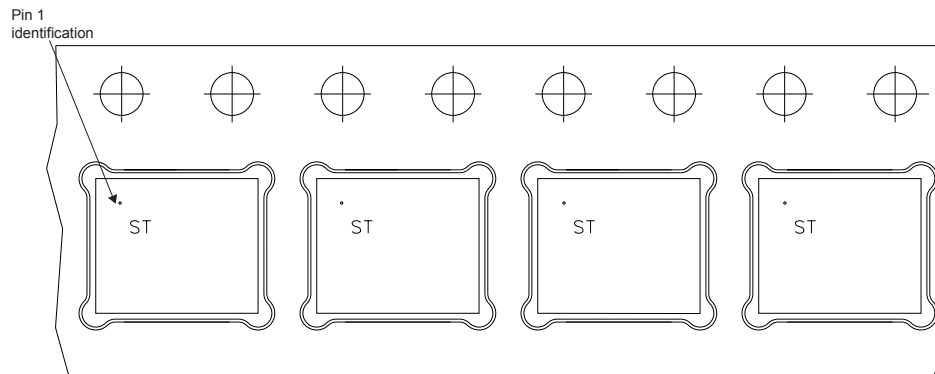
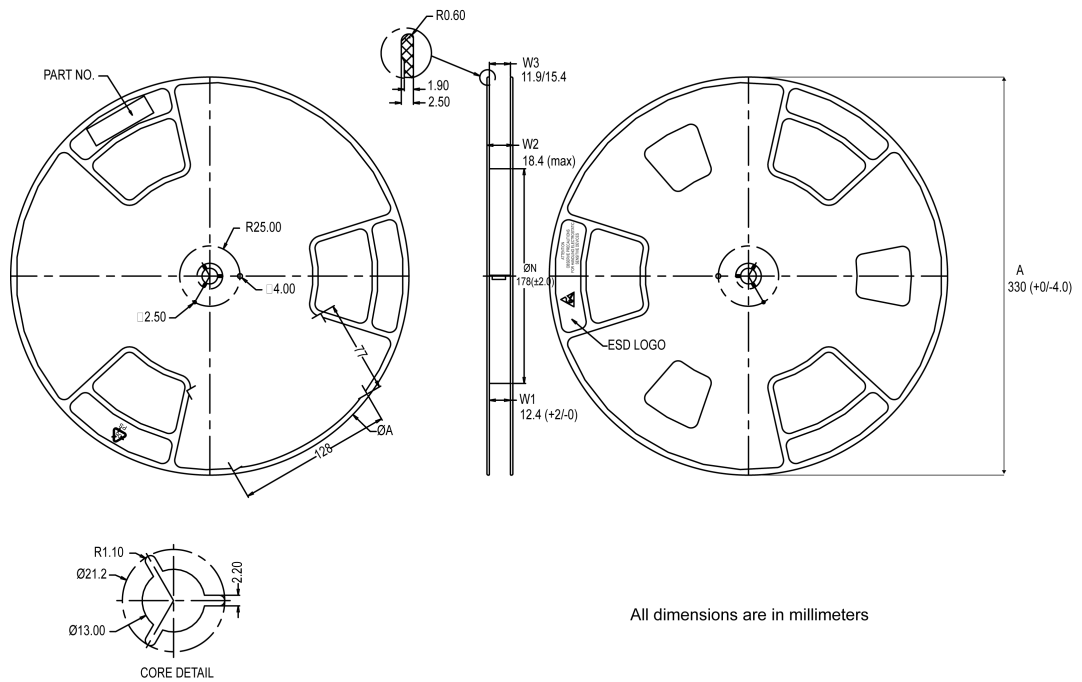


Figure 22. PowerFLAT™ 5x6 reel (dimensions are in mm)



8234350_Reel_rev_C

Revision history

Table 9. Document revision history

Date	Version	Changes
05-Apr-2018	1	Initial release. The document status is production data.

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