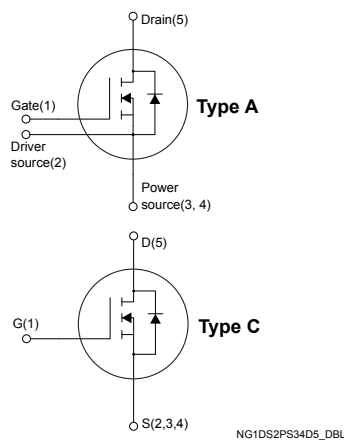
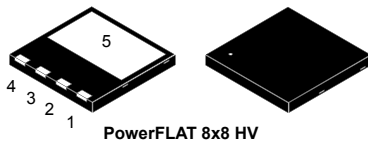


N-channel 650 V, 180 mΩ typ., 15 A, MDmesh M5 Power MOSFET in a PowerFLAT 8x8 HV package



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)}$ max.	I_D
STL22N65M5	710 V	210 mΩ	15 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.



Product status link

[STL22N65M5](#)

Product summary

Order code	STL22N65M5
Marking	22N65M5
Package	PowerFLAT 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	9.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	60	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 15\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	$^\circ\text{C}/\text{W}$

1. When mounted on an 1-inch² FR-4, 2oz Cu board

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	4	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	270	mJ

1. Pulse width limited by T_{jmax}
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$, $T_{\text{case}} = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 100	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 8.5\text{ A}$		180	210	$\text{m}\Omega$

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	1434	-	pF
C_{oss}	Output capacitance		-	38	-	
C_{rss}	Reverse transfer capacitance		-	3.7	-	
$C_{\text{o(er)}^{(1)}}$	Equivalent output capacitance energy related	$V_{\text{DS}} = 0\text{ to }520\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	35	-	pF
$C_{\text{o(tr)}^{(2)}}$	Equivalent output capacitance time related		-	118	-	
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 520\text{ V}$, $I_{\text{D}} = 9\text{ A}$,	-	36	-	nC
Q_{gs}	Gate-source charge	$V_{\text{GS}} = 0\text{ to }10\text{ V}$	-	7.5	-	
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	18	-	

1. $C_{\text{o(er)}}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{\text{o(tr)}}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(v)}}$	Voltage delay time	$V_{\text{DD}} = 400\text{ V}$, $I_{\text{D}} = 12\text{ A}$,	-	43	-	ns
$t_{\text{r(v)}}$	Voltage rise time	$R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$	-	7.5	-	
$t_{\text{f(i)}}$	Current fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	7.5	-	
$t_{\text{c(off)}}$	Crossing time		-	11.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 15\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	272		ns
Q_{rr}	Reverse recovery charge		-	3.4		μC
I_{RRM}	Reverse recovery current		-	25		A
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	336		ns
Q_{rr}	Reverse recovery charge		-	4.3		μC
I_{RRM}	Reverse recovery current		-	25.6		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area

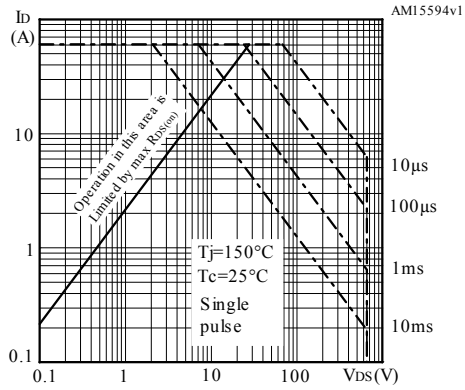


Figure 2. Thermal impedance

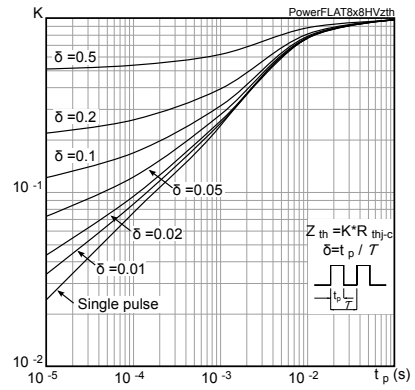


Figure 3. Output characteristics

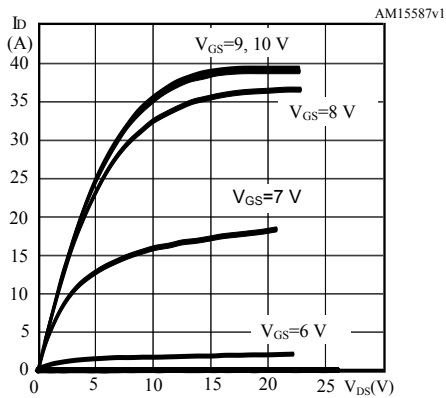


Figure 4. Transfer characteristics

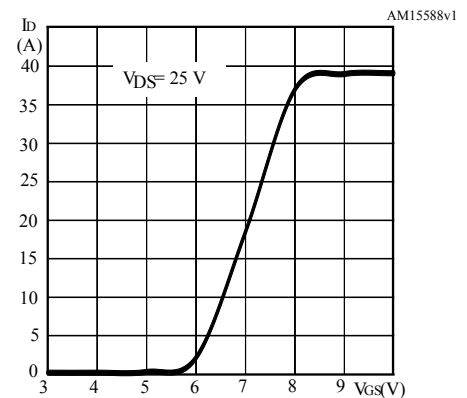


Figure 5. Gate charge vs gate-source voltage

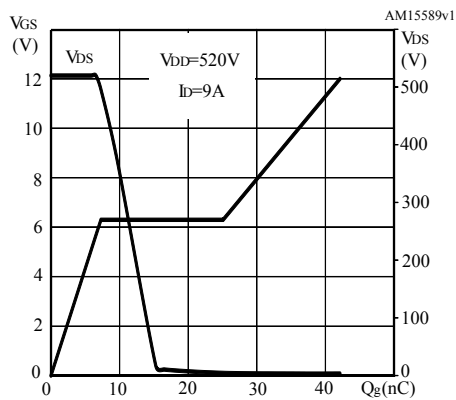


Figure 6. Static drain-source on-resistance

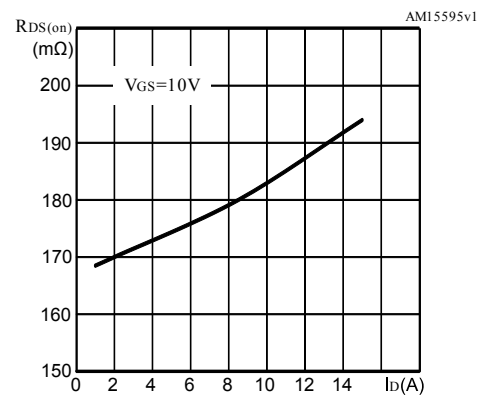


Figure 7. Capacitance variations

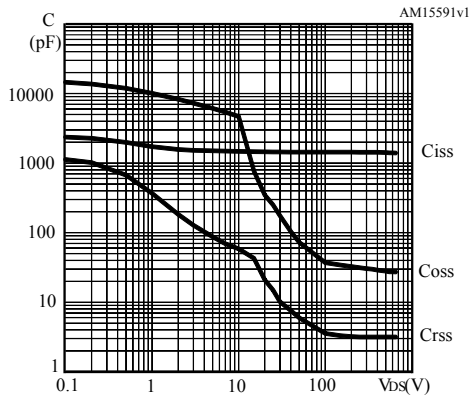


Figure 8. Output capacitance stored energy

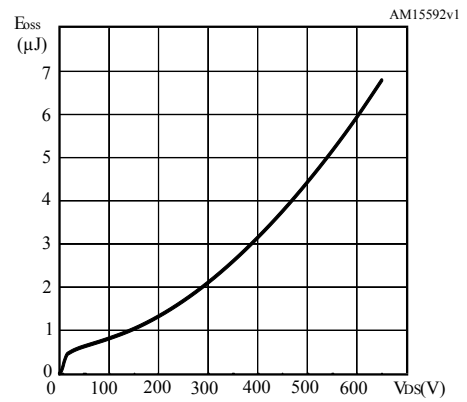


Figure 9. Normalized gate threshold voltage vs temperature

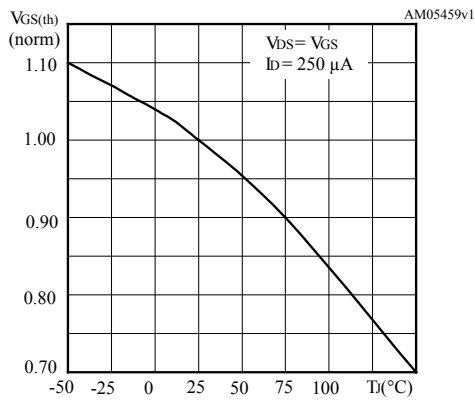


Figure 10. Normalized on-resistance vs temperature

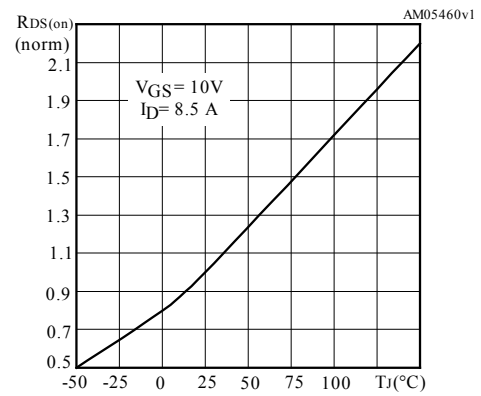


Figure 11. Normalized breakdown voltage vs temperature

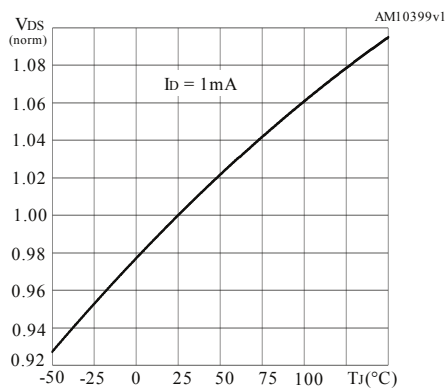


Figure 12. Drain-source diode forward characteristics

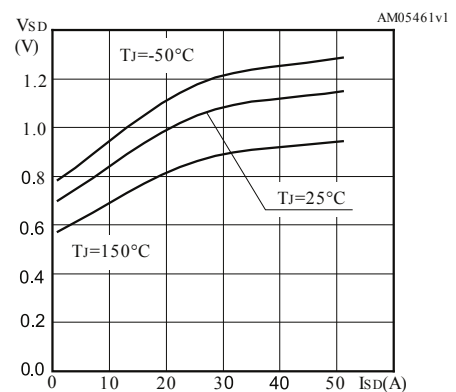
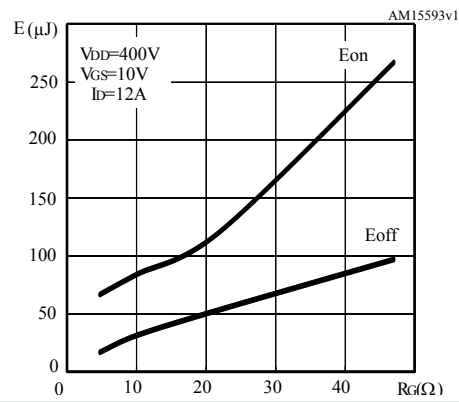
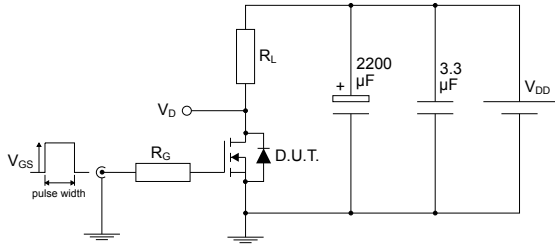


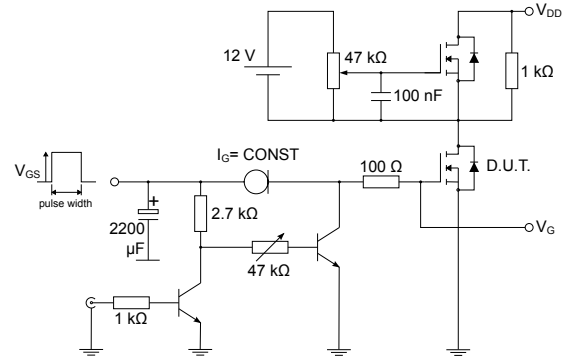
Figure 13. Switching energy vs gate resistance



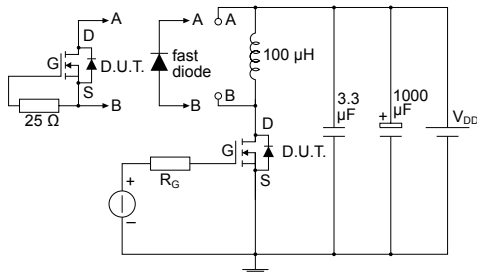
3 Test circuits

Figure 14. Test circuit for resistive load switching times


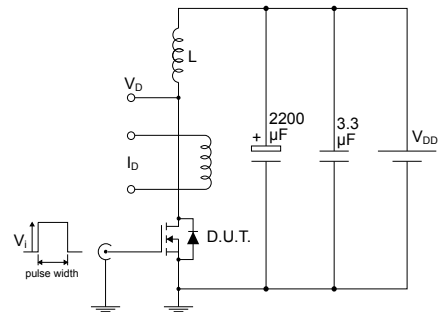
AM01468v1

Figure 15. Test circuit for gate charge behavior


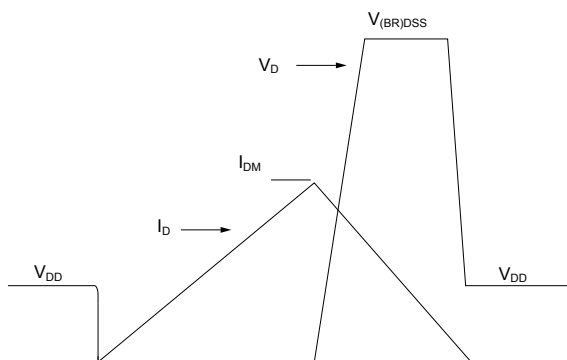
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Figure 16. Test circuit for inductive load switching and diode recovery times


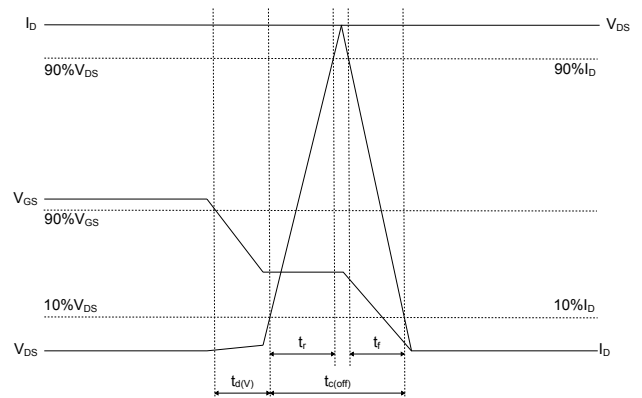
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


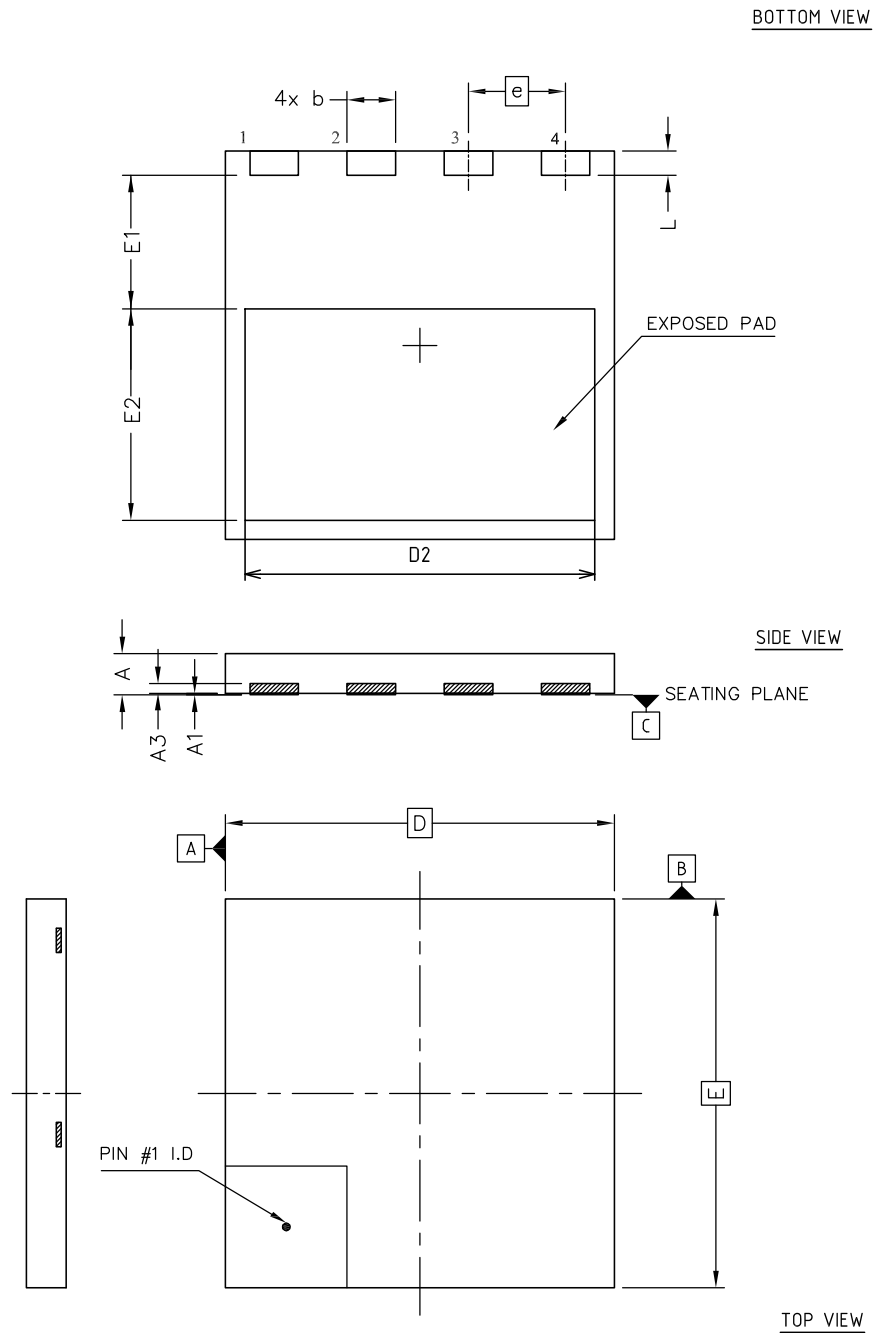
AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV type A package information

Figure 20. PowerFLAT 8x8 HV type A package outline



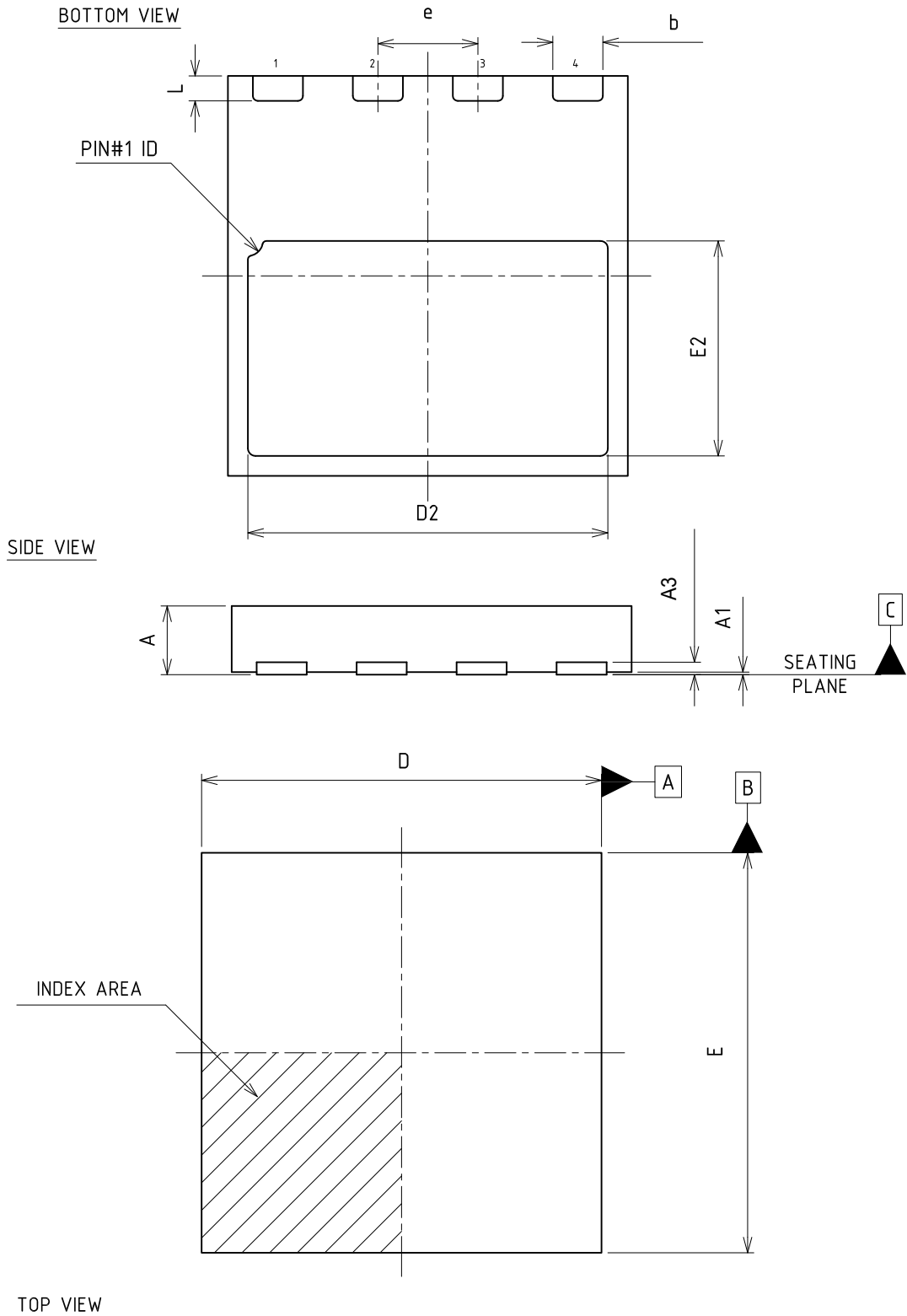
8222871_Rev_4

Table 8. PowerFLAT 8x8 HV type A mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

4.2 PowerFLAT 8x8 HV type C package information

Figure 21. PowerFLAT 8x8 HV type C package outline

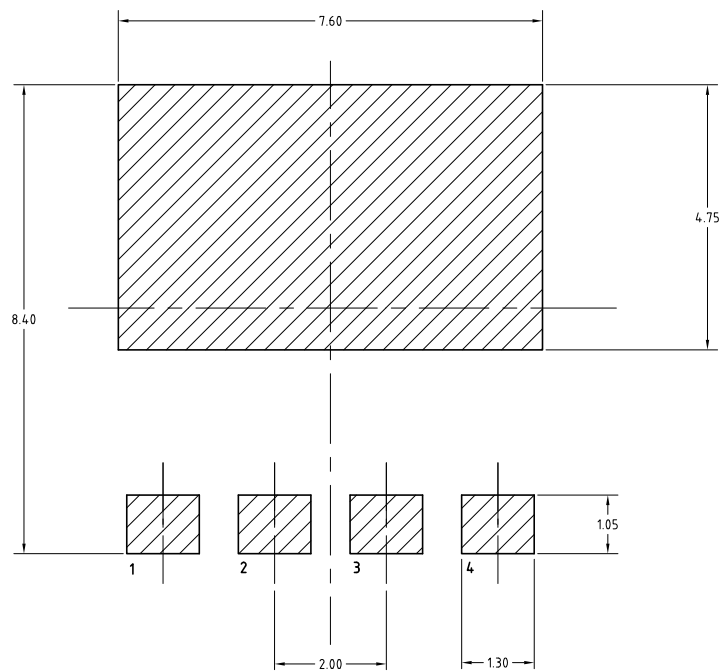


8222871_Rev4_typeC

Table 9. PowerFLAT 8x8 HV type C mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.10	0.20	0.30
b	0.95	1.00	1.05
D		8.00	
D2	7.05	7.20	7.30
E		8.00	
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 22. PowerFLAT 8x8 HV footprint

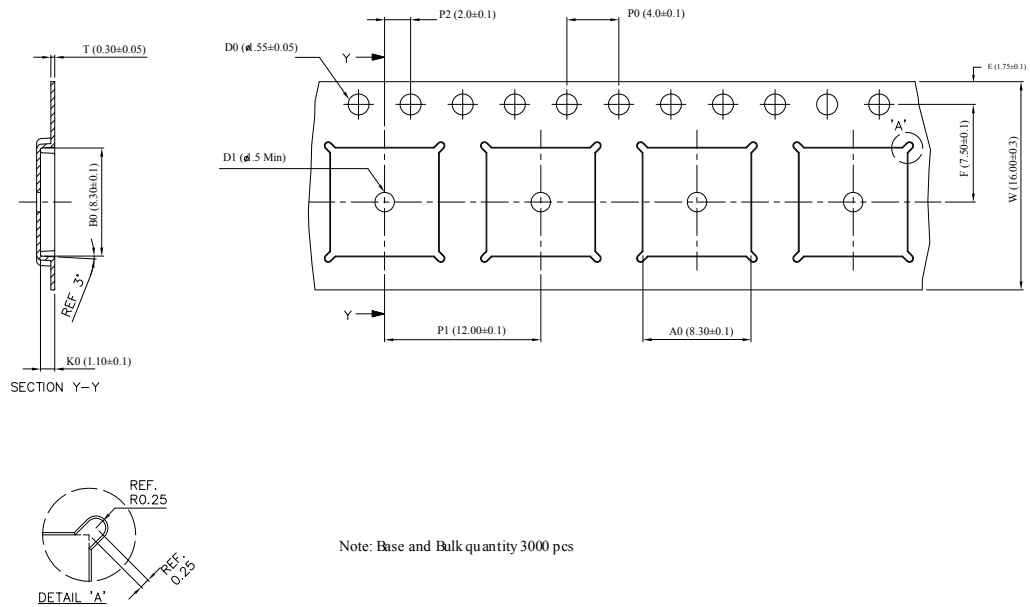


8222871_REV_4_footprint

Note: All dimensions are in millimeters.

4.3 PowerFLAT 8x8 HV packing information

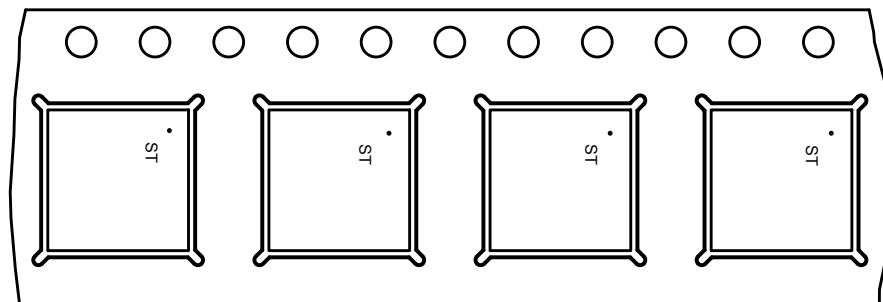
Figure 23. PowerFLAT 8x8 HV tape



8229819_Tape_revA

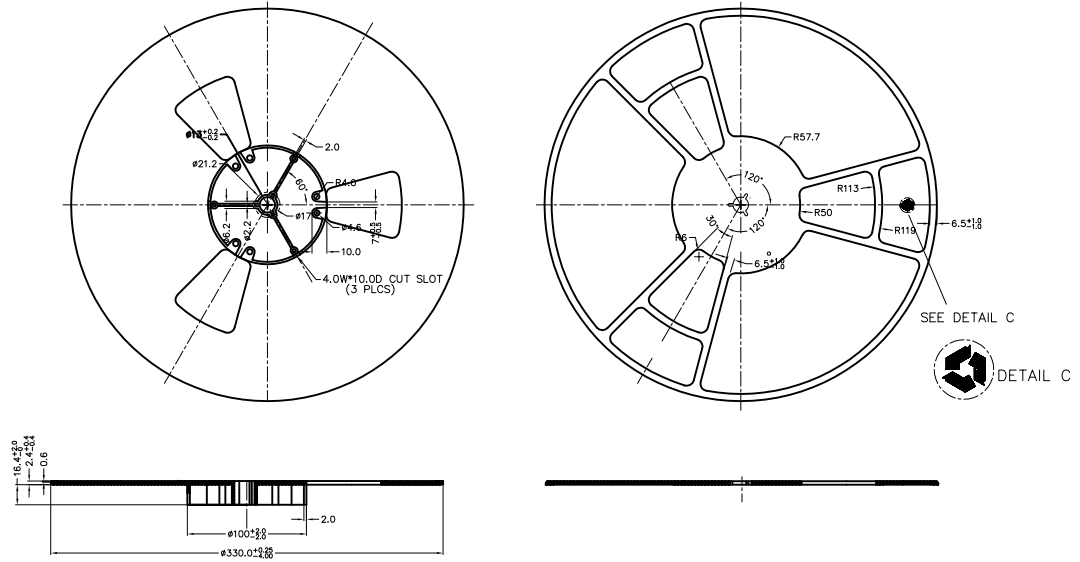
Note: All dimensions are in millimeters.

Figure 24. PowerFLAT 8x8 HV package orientation in carrier tape



Note: According to JEDEC standard.

Figure 25. PowerFLAT 8x8 HV reel



8229819_Reel_revA

Note: All dimensions are in millimeters.

Revision history

Table 10. Document revision history

Date	Version	Changes
06-Aug-2012	1	First release.
01-Feb-2013	2	<ul style="list-style-type: none"> – Document status promoted from preliminary data to production data – Modified: <i>Figure 1</i>, IDM, IAR, dv/dt values on <i>Table 2</i>, <i>note 4</i>, RDS(on) value on <i>Table 4</i>, typical values on <i>Table 5</i>, <i>6</i> and <i>7</i> and ISDM max value on <i>Table 7</i> – Inserted: <i>Section 2.1: Electrical characteristics (curves)</i> – Minor text changes
21-Oct-2020	3	<ul style="list-style-type: none"> Modified title, description and internal schematic diagram in cover page. Updated Section 1 Electrical ratings and Section 2 Electrical characteristics. Added Section 4.2 PowerFLAT 8x8 HV type C package information. Modified Figure 24. PowerFLAT 8x8 HV package orientation in carrier tape. Minor text changes.

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