STL35N3LH8

N-channel 30 V, 0.9 mΩ typ., 35 A STripFET™ H8 Power MOSFET in a PowerFLAT™ 3.3 x 3.3 package

Datasheet - preliminary data

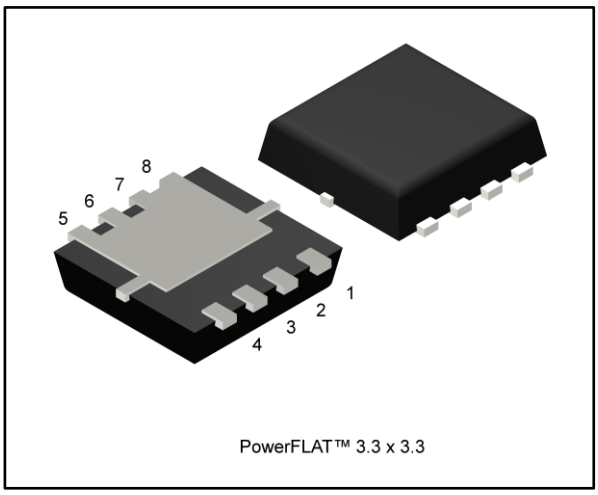
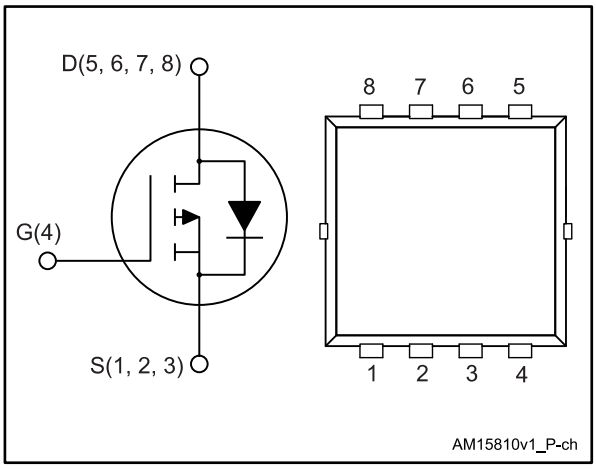


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL35N3LH8	30 V	1.1 mΩ	35 A

- Extremely low on-resistance $R_{DS(on)}$
- Excellent figure of merit (FoM)

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes the 8th generation of STripFET™ technology with an enhanced trench gate structure for very low on-state resistance and gate charge, resulting in best in class conduction and switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STL35N3LH8	35NH8	PowerFLAT™ 3.3 x 3.3	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_{pcb} = 25 °C	35	A
I_D (1)	Drain current (continuous) at T_{pcb} = 100 °C	22	A
I_{DM} (2)	Drain current (pulsed)	140	A
I_D (3)	Drain current (continuous) at Tc = 25 °C	45	A
I_D (3)	Drain current (continuous) at Tc = 100 °C	45	A
I_{DM} (2)(3)	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at T_C = 25 °C	64	W
P_{TOT} (1)	Total dissipation at T_{pcb} = 25 °C	2.9	W
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

Notes:

(1)The value is rated according $R_{thj\text{-}pcb}$.

(2)Pulse width limited by safe operating area.

(3)The value is rated according $R_{thj\text{-}c}$ and limited by package.

Table 3: Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.95	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	42.8	°C/W

Notes:

(1)When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 s.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 30 V			1	µA
		V_{GS} = 0, V_{DS} = 30 V, T_C = 125 °C (1)			10	µA
I_{GSS}	Gate body leakage current	V_{GS} = ± 20 V, V_{DS} = 0			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 17.5 A		0.9	1.1	mΩ
		V_{GS} = 4.5 V, I_D = 17.5 A		1	1.3	

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 24 V, f = 1 MHz, V_{GS} = 0	-	3400	-	pF
C_{oss}	Output capacitance		-	630	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
Q_g	Total gate charge	V_{DD} = 24 V, I_D = 35 A V_{GS} = 4.5 V (see *Figure 3: "Test circuit for gate charge behavior"*)	-	24	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC
R_G	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	-	TBD	-	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 24 V, I_D = 17.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2: "Test circuit for resistive load switching times"*)	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 35 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 35 A, di/dt = 100 A/µs, V_{DD}= 24 V	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.

3 Test circuits

Figure 2: Test circuit for resistive load switching times

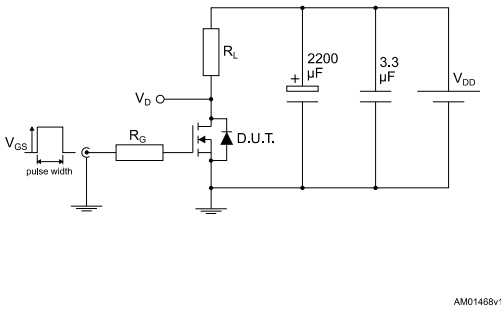


Figure 3: Test circuit for gate charge behavior

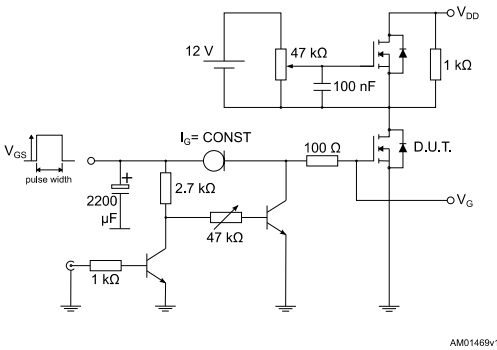


Figure 4: Test circuit for inductive load switching and diode recovery times

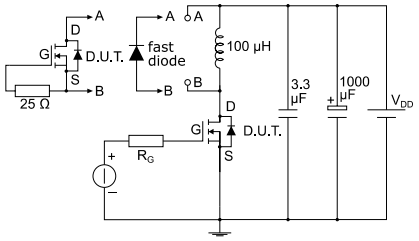


Figure 5: Unclamped inductive load test circuit

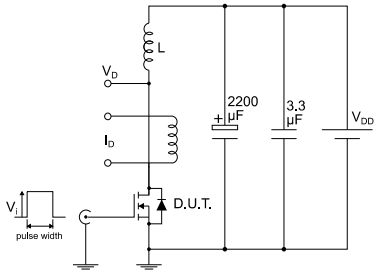


Figure 6: Unclamped inductive waveform

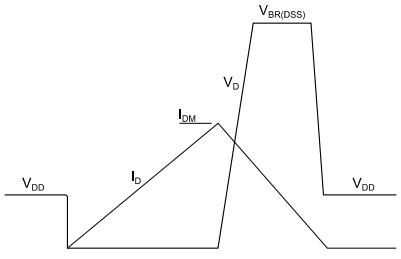
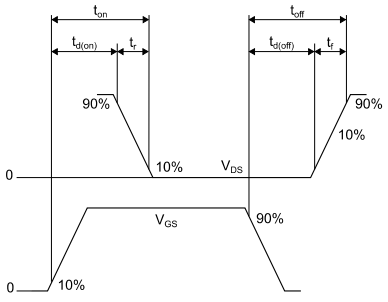


Figure 7: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PoweFLAT™ 3.3x3.3 package information

Figure 8: PowerFLAT™ 3.3x3.3 package outline

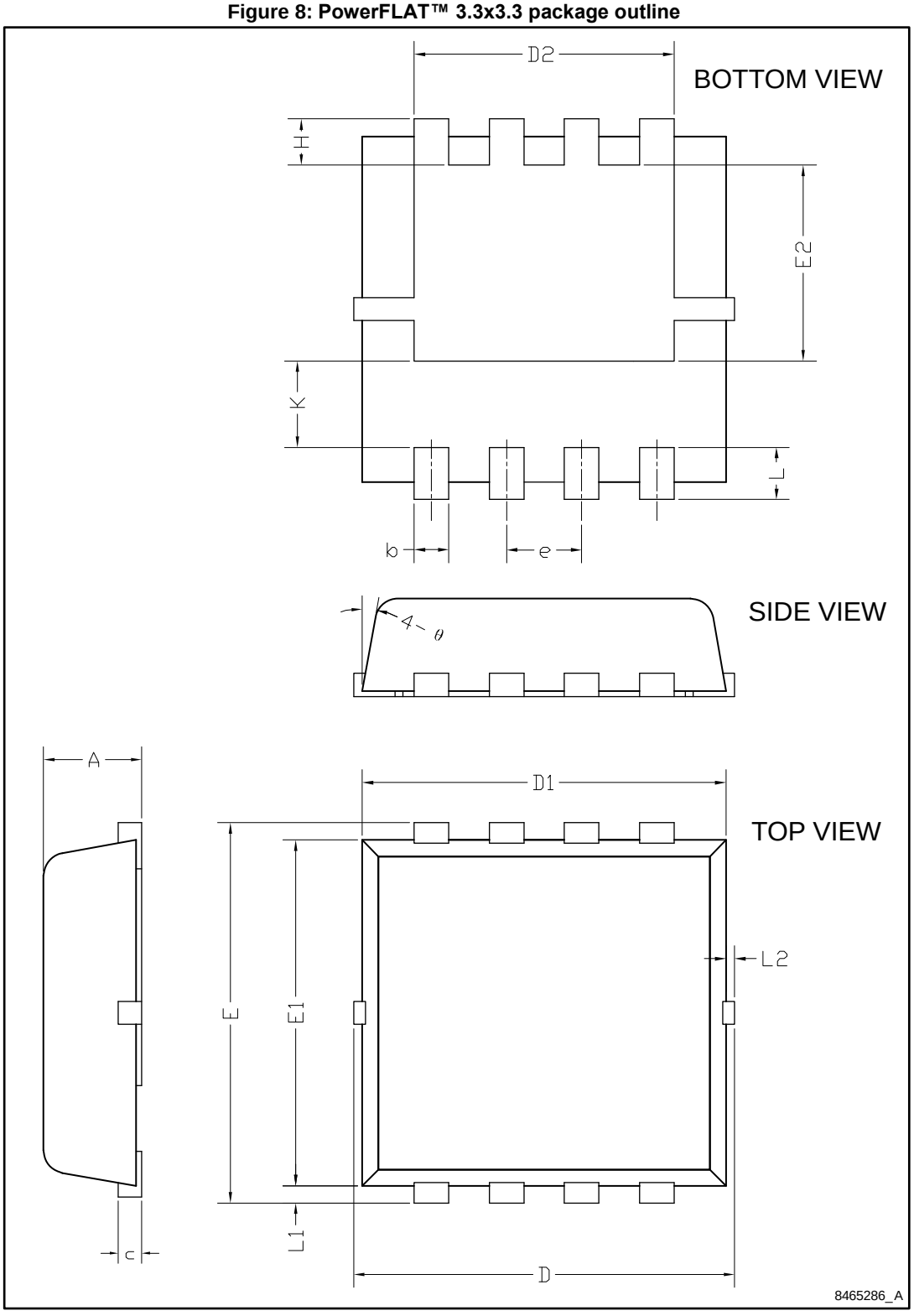
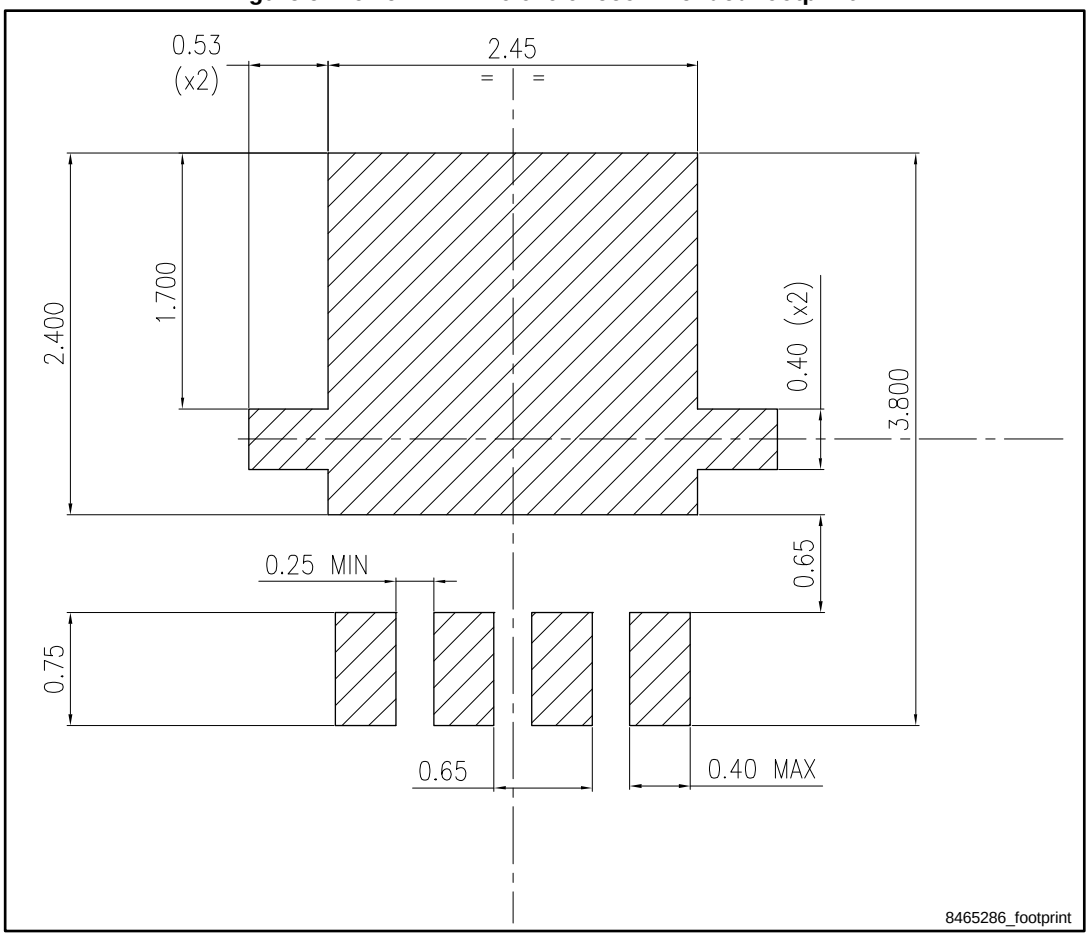


Table 8: PowerFLAT™ 3.3x3.3 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	030	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 9: PowerFLAT™ 3.3x3.3 recommended footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
05-Oct-2016	1	First release.

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