



STL70N2LLH5

N-channel 30 V, 0.0059 Ω , 18 A PowerFLAT™ (5x6)
STripFET™ V Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STL70N2LLH5	30 V	<0.0068 Ω	18 A ⁽¹⁾

1. This value is rated according to R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

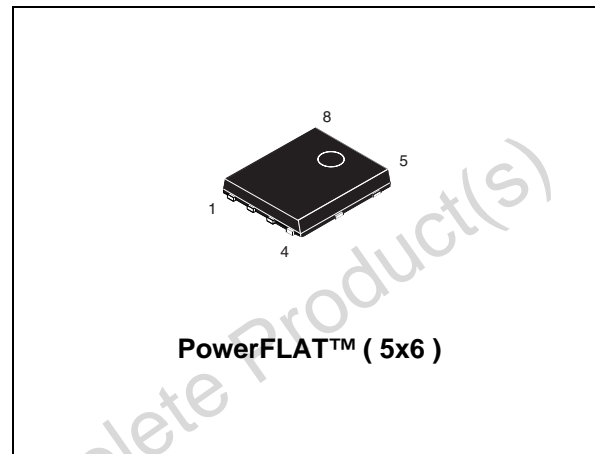


Figure 1. Internal schematic diagram

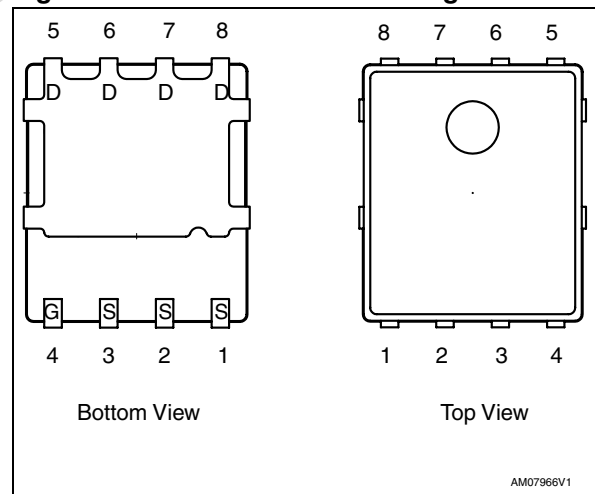


Table 1. Device summary

Order code	Marking	Package	Packaging
STL70N2LLH5	70N2LLH5	PowerFLAT™ (5x6)	Tape and reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 8

4 **Package mechanical data** 9

5 **Revision history** 11

Obsolete Product(s) - Obsolete Product(s)



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	+ 22 / - 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	70	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	43.75	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	18	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	11.25	A
$I_{DM}^{(3)}$	Drain current (pulsed)	72	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	62.5	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ °C}$	4	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. This value is rated according to R_{thj-c}
2. This value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain, steady state)	2	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by $T_J \text{ Max}$)	TBD	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AV}$, $V_{DD} = 21\text{ V}$)	TBD	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125\text{ }^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = +22\text{ V} / -20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 9\text{ A}$		0.0059 0.0075	0.0068 0.0085	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1217 339 46	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15\text{ V}$, $I_D = 18\text{ A}$ $V_{GS} = 4.5\text{ V}$ Figure 3	-	8.3 3.8 3.4	-	nC nC nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 test signal level = 20 mV open drain	-	1.1	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 15\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ Figure 2	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=25\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

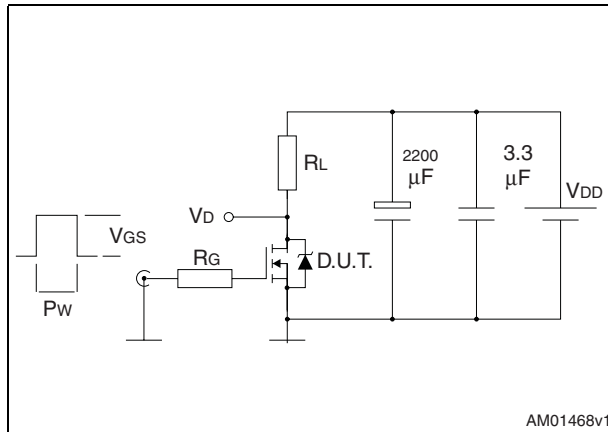


Figure 3. Gate charge test circuit

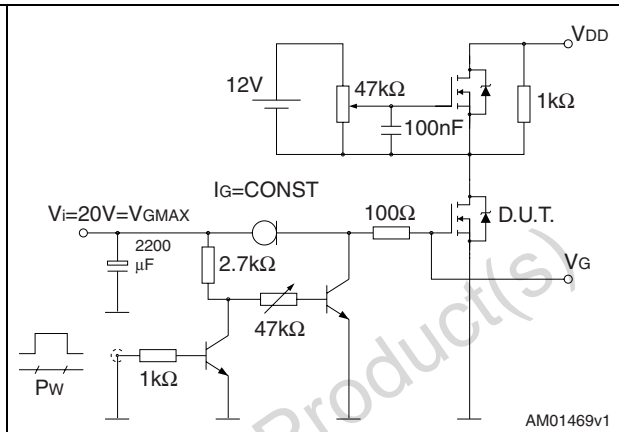


Figure 4. Test circuit for inductive load switching and diode recovery times

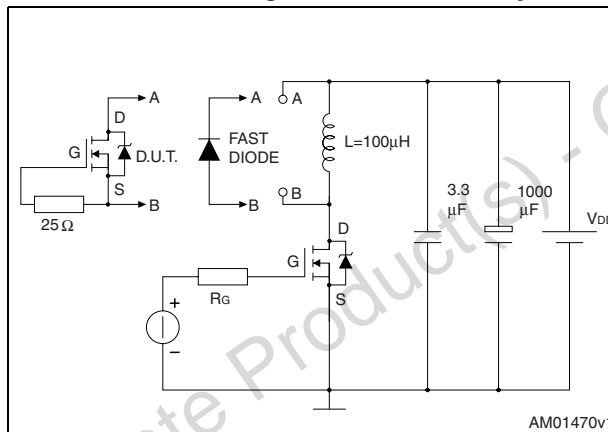


Figure 5. Unclamped inductive load test circuit

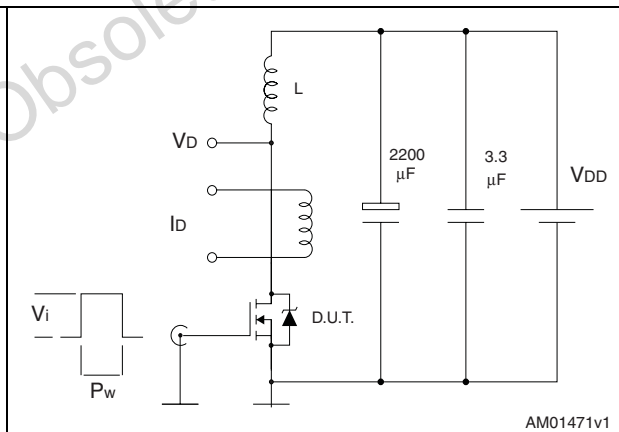


Figure 6. Unclamped inductive waveform

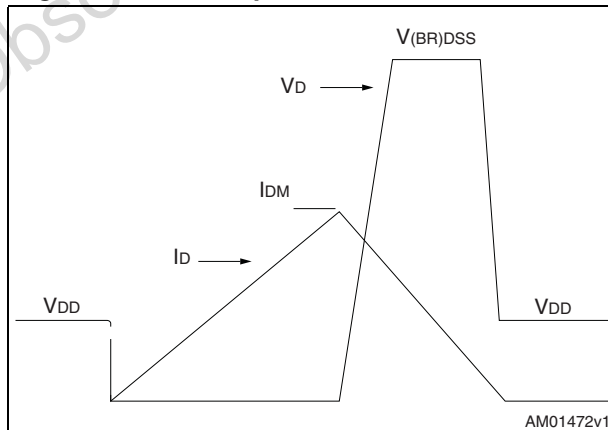
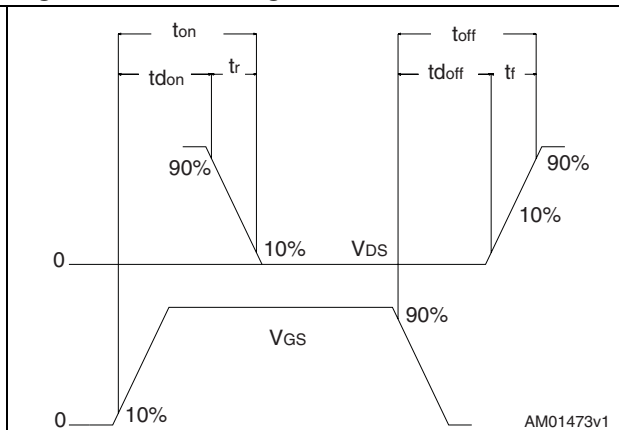


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

Table 9. PowerFLAT 5x6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.50		0.80
K	1.275		1.575

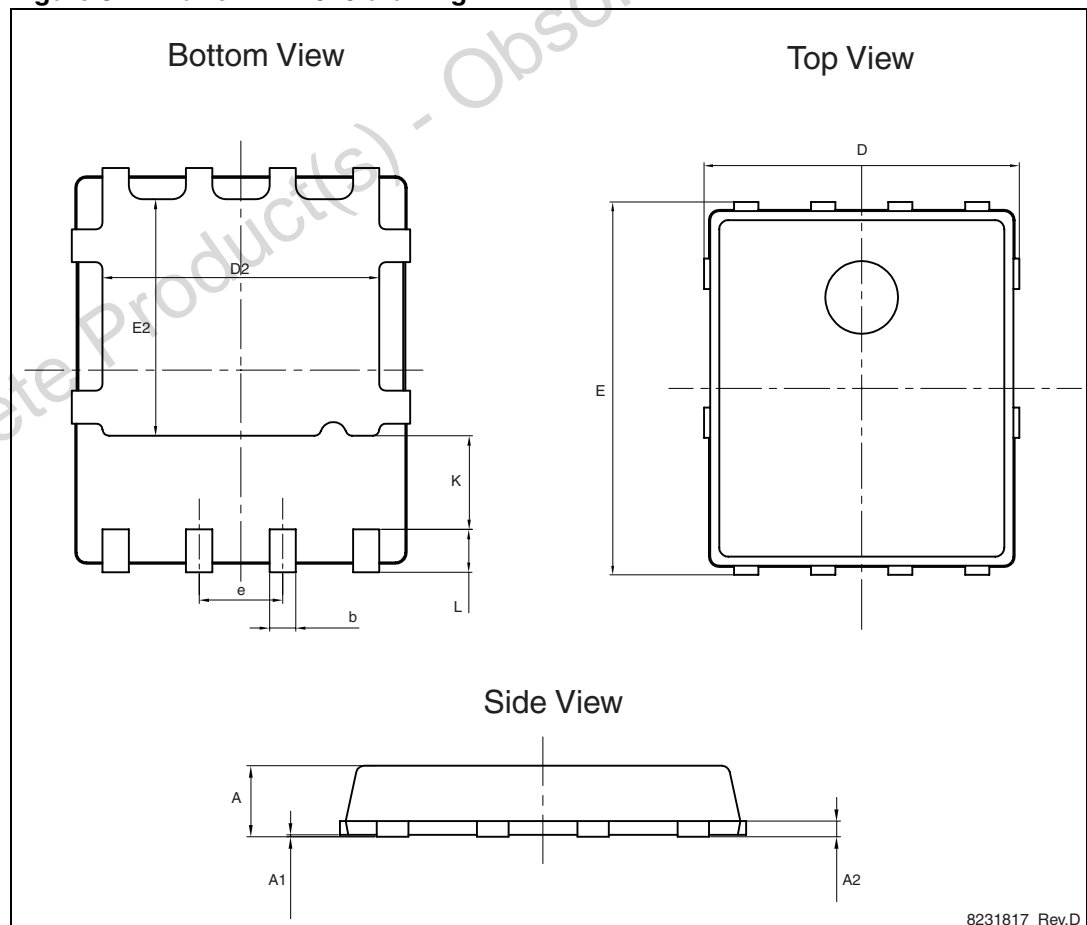
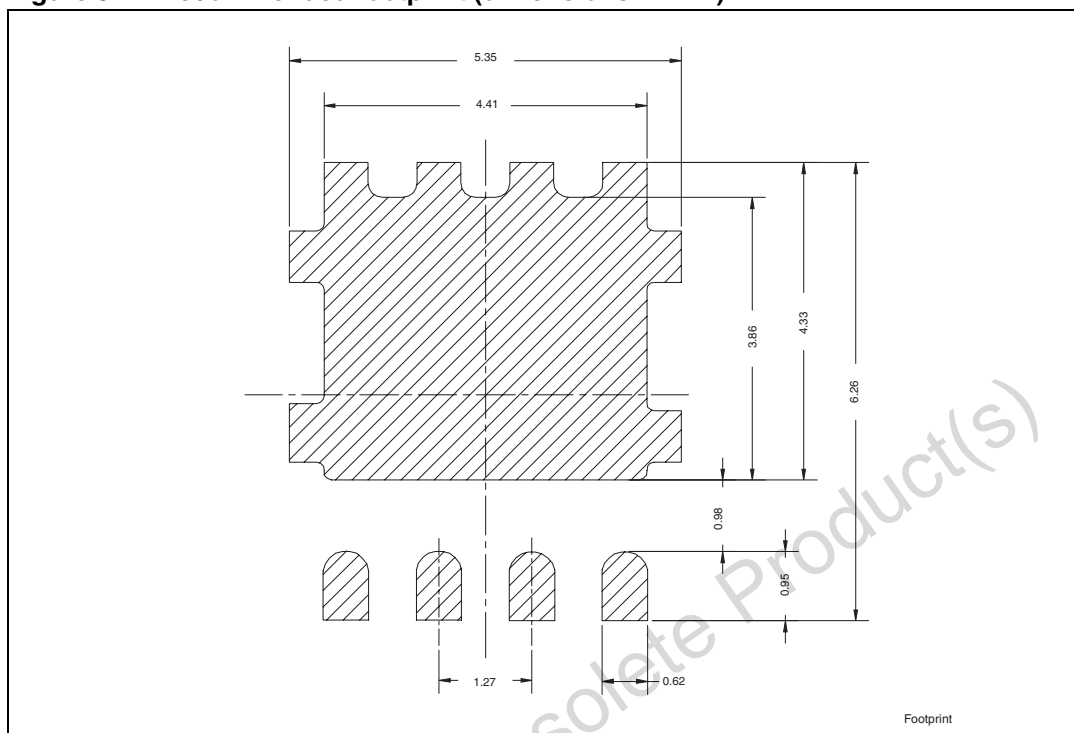
Figure 8. PowerFLAT 5x6 drawing

Figure 9. Recommended footprint (dimensions in mm)

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Jul-2011	1	First release.

Obsolete Product(s) - Obsolete Product(s)

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