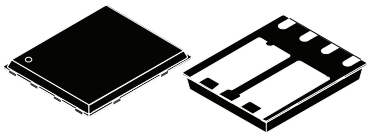
STL8DN4LLF6

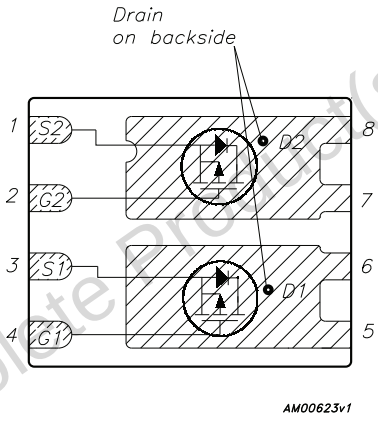
Dual N-channel 40 V, 0.025 Ωtyp., 8 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet − target specification



PowerFLAT™ 5x6 double island

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D
STL8DN4LLF6	40 V	0.03 Ω (V_{GS}=10 V) 0.05 Ω (V_{GS}=4.5 V)	8 A

- Very low on-resistance
- High avalanche ruggedness

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL8DN4LLF6	8DN4LLF6	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	34	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	21	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	8	A
I_D (2)	Drain current (continuous) at T_{pcb} = 100 °C	5.3	A
I_{DM} (2)(3)	Drain current (pulsed)	32	A
P_{TOT} (1)	Total dissipation at T_c = 25 °C	62.5	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4	W
	Derating factor (2)	0.032	°C
T_j	Operating junction temperature	- 55 to 150	°C

1. This value is rated according to $R_{thj\text{-}c}$
2. This value is rated according to $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	32	°C/W

1. When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 20 V			1	µA
		V_{GS} = 0, V_{DS} = 20 V, T_C=125 °C			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A V_{GS} = 4.5 V, I_D = 4 A		0.025 0.04	0.03 0.05	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	300	-	pF
C_{oss}	Output capacitance		-	55	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
Q_g	Total gate charge	V_{DD} = 10 V, I_D = 8 A, V_{GS} = 4.5 V (see *Figure 3*)	-	4	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 10 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 4.5 V	-	TBD	-	ns
t_r	Voltage rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Current fall time		-	TBD	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM} (1)	Source-drain current (pulsed)				32	A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD} = 25 V, T_j=150 °C	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

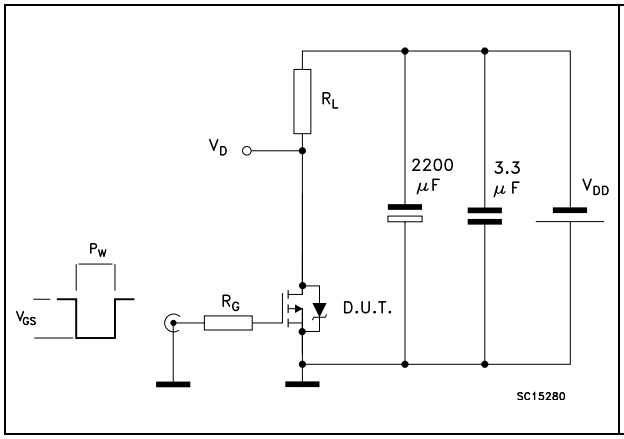


Figure 3. Gate charge test circuit

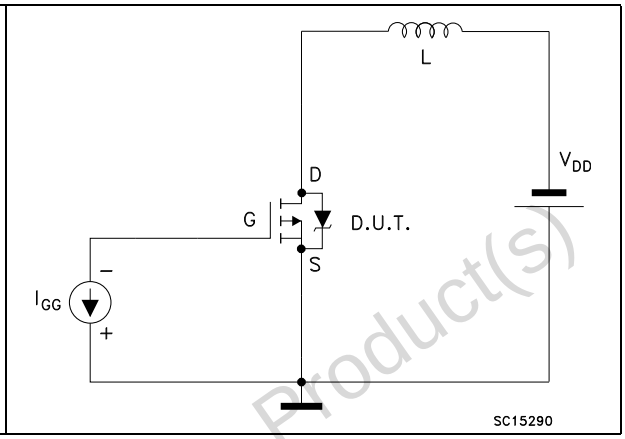
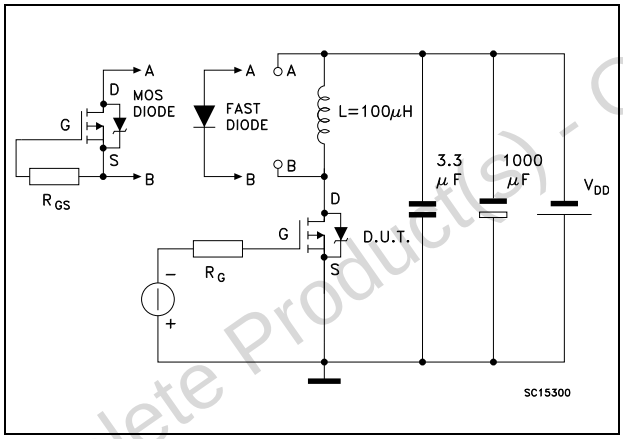


Figure 4. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

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ECOPACK® is an ST trademark.

Table 8. PowerFLAT™ 5x6 - double island mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 5. PowerFLAT™ 5x6 - double island drawing (dimensions are in mm)

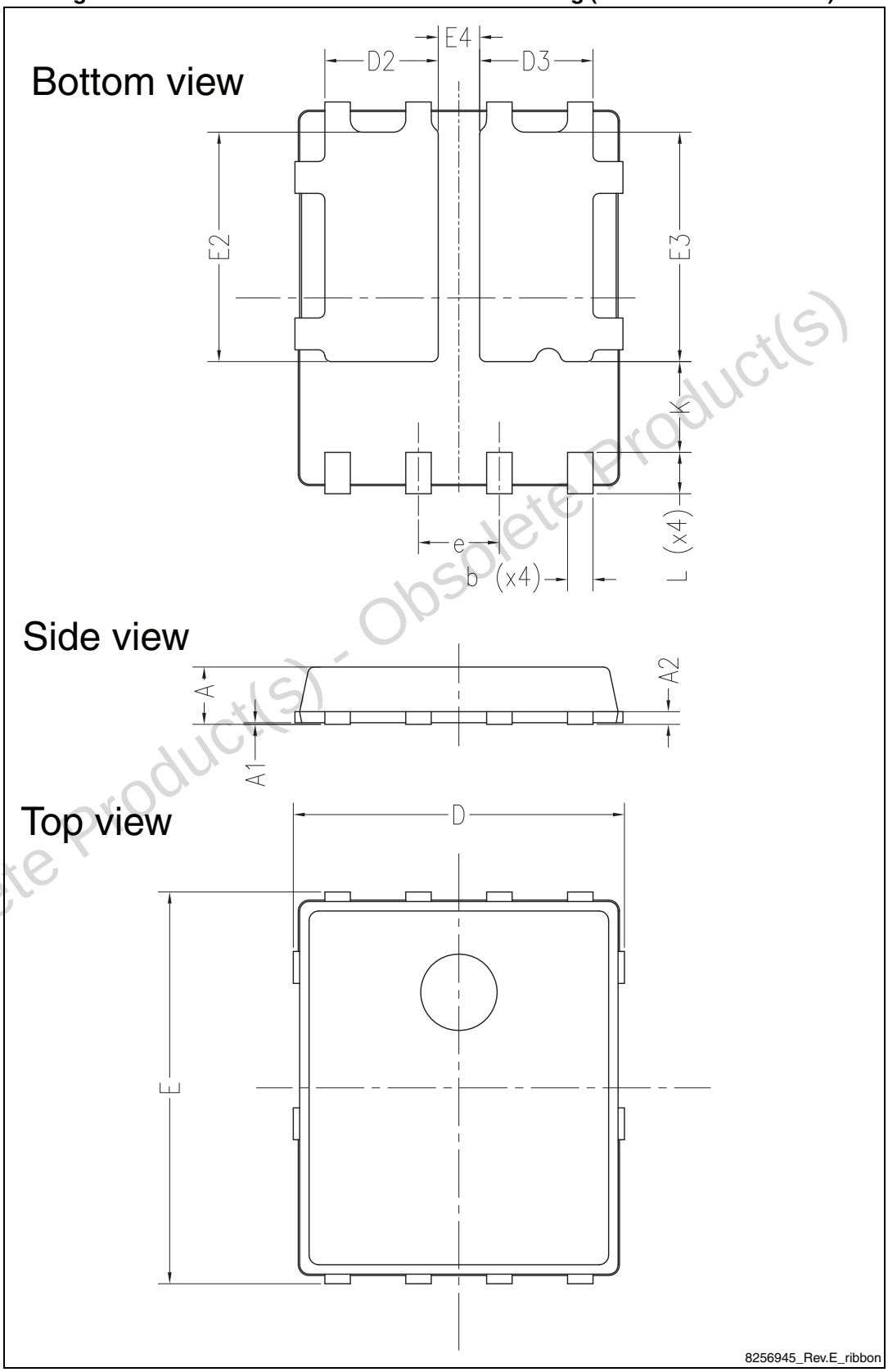
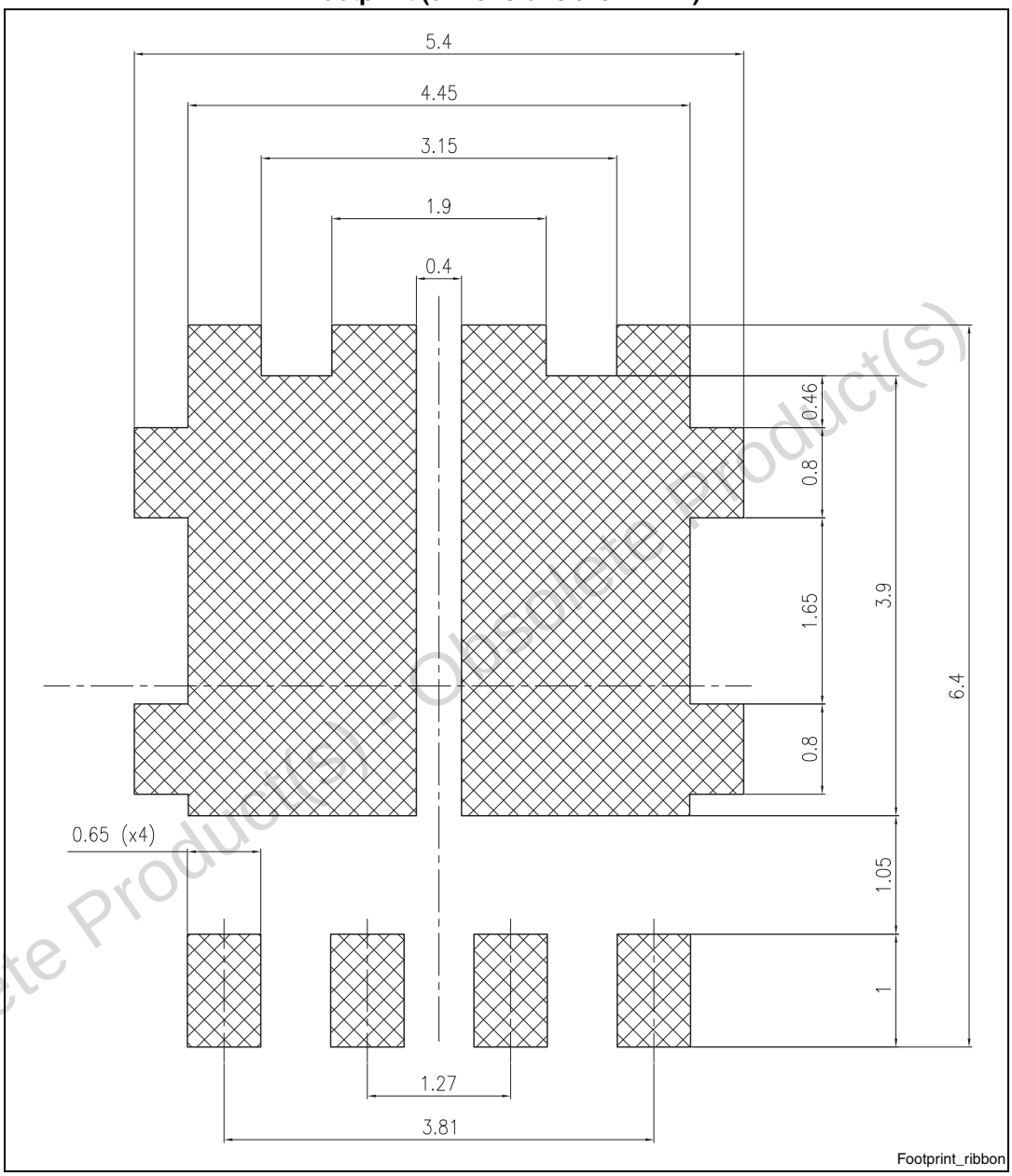


Figure 6. PowerFLAT™ 5x6 - 8 leads dual pad (ribbon) drawing recommended footprint (dimensions are in mm)



5 Packaging mechanical data

Figure 7. PowerFLAT™ 5x6 tape[a]

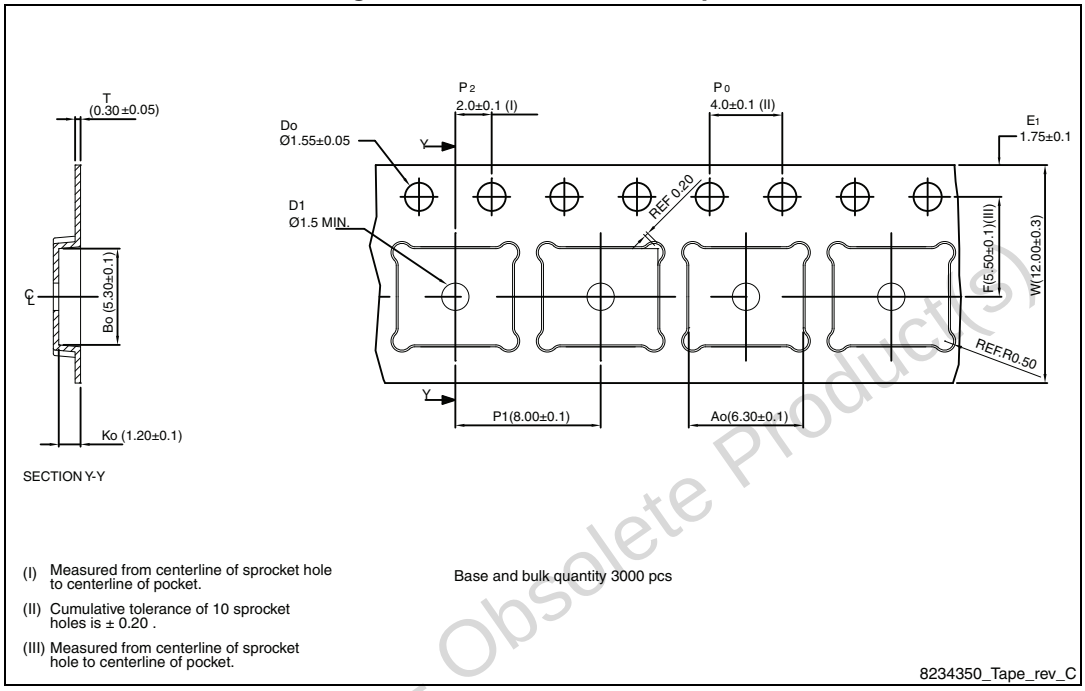
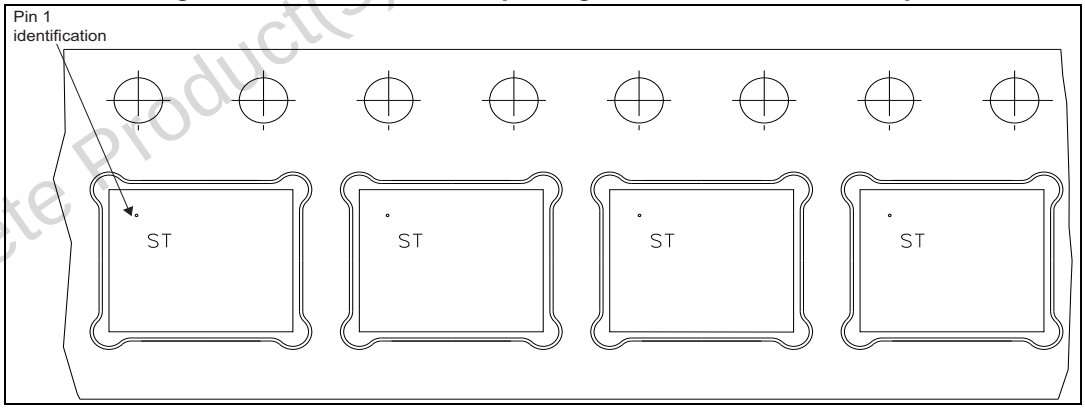
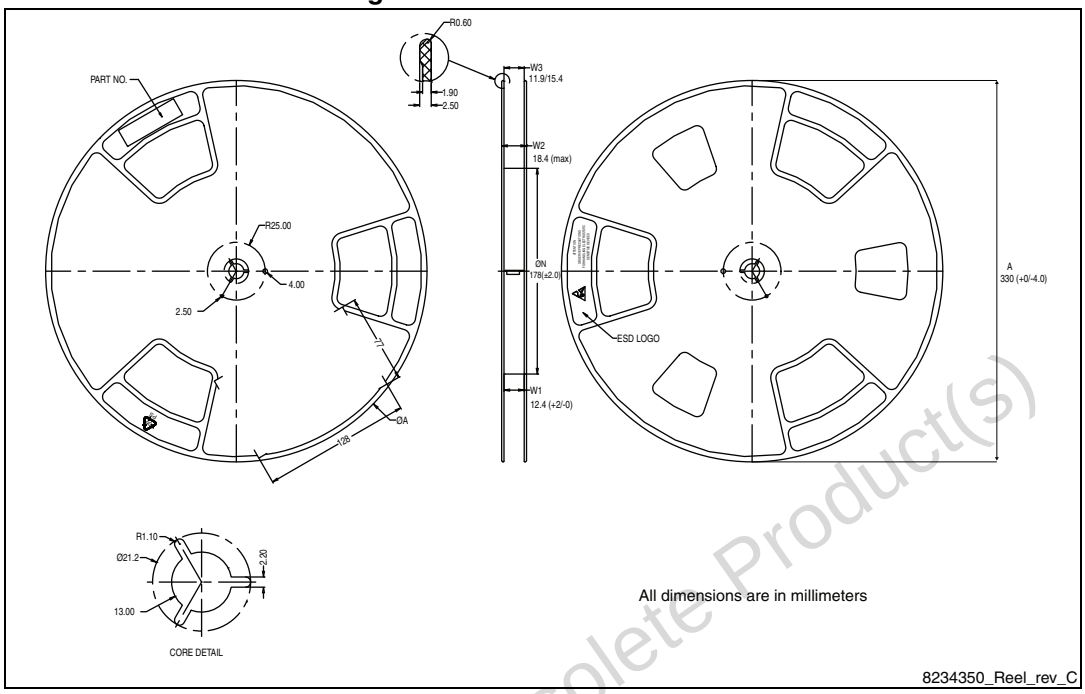


Figure 8. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 9. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Mar-2013	1	First release.

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