STM705, STM706
STM707, STM708, STM813L

5 V supervisor

Datasheet - production data

- 200 ms (typ) \( t_{\text{rec}} \)
- Watchdog timer - 1.6 s (typ)
- Manual reset input (MR)
- Power-fail comparator (PFI/PFO)
- Low supply current - 40 \( \mu \)A (typ)
- Guaranteed RST (RST) assertion down to \( V_{CC} = 1.0 \) V
- Operating temperature:
  - \(-40 \) °C to 85 °C (industrial grade) or
  - \(-40 \) °C to 125 °C (automotive grade for the STM706 only)
- RoHS compliance
  - Lead-free components are compliant with the RoHS directive

Features

- 5 V operating voltage
- Precision \( V_{CC} \) monitor
  - STM705/707/813L
  - \( 4.50 \) V \( \leq V_{RST} \leq 4.75 \) V
  - STM706/708
  - \( 4.25 \) V \( \leq V_{RST} \leq 4.50 \) V
- RST and RST outputs

Table 1. Device summary

<table>
<thead>
<tr>
<th></th>
<th>Watchdog input</th>
<th>Watchdog output(1)</th>
<th>Active-low RST(1)</th>
<th>Active-high RST(1)</th>
<th>Manual reset input</th>
<th>Power-fail comparator</th>
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<tr>
<td>STM705</td>
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<tr>
<td>STM706(2)</td>
<td>✓</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

1. Push-pull output
2. Automotive grade (\(-40 \) °C to 125 °C) option for the STM706 only.

1. Contact local ST sales office for availability.
Contents

1 Description ................................................................. 5

2 Pin descriptions ......................................................... 8
   2.1 MR ................................................................. 8
   2.2 WDI ............................................................... 8
   2.3 WDO ............................................................... 8
   2.4 RST ............................................................... 8
   2.5 RST ............................................................... 8
   2.6 PFI ............................................................... 8
   2.7 PFO ............................................................... 9

3 Operation ............................................................... 11
   3.1 Reset output ....................................................... 11
   3.2 Push-button reset input ......................................... 11
   3.3 Watchdog input (STM705/706/813L) .......................... 11
   3.4 Watchdog output (STM705/706/813L) .......................... 12
   3.5 Power-fail input/output ......................................... 12
   3.6 Ensuring a valid reset output down to VCC = 0 V .............. 12
   3.7 Interfacing to microprocessors with bidirectional reset pins 13

4 Typical operating characteristics .................................. 14

5 Maximum ratings ......................................................... 22

6 DC and AC parameters .................................................. 23

7 Package mechanical data ............................................... 27

8 Part numbering ............................................................. 30

9 Revision history ........................................................... 32
List of tables

Table 1. Device summary ................................................................. 1
Table 2. Signal names ...................................................................... 6
Table 3. Pin description .................................................................... 9
Table 4. Absolute maximum ratings .................................................. 22
Table 5. Operating and AC measurement conditions ......................... 23
Table 6. DC and AC characteristics ................................................... 25
Table 7. SO8 - 8-lead plastic small outline, 150 mils body width, pack. mech. data ........................................ 28
Table 8. TSSOP8 - 8-lead, thin shrink small outline, 3 x 3 mm body size, mechanical data ......................... 29
Table 9. Ordering information scheme .............................................. 30
Table 10. Marking description ......................................................... 31
Table 11. Document revision history ............................................... 32
List of figures

Figure 1. Logic diagram (STM705/706/813L) ................................................................. 5
Figure 2. Logic diagram (STM707/708) ................................................................. 5
Figure 3. STM705/706/813L SO8 connections .......................................................... 6
Figure 4. STM705/706/813L TSSOP8 connections ....................................................... 6
Figure 5. STM707/708 SO8 connections ................................................................. 7
Figure 6. STM707/708 TSSOP8 connections .............................................................. 7
Figure 7. Block diagram (STM705/706/813L) ............................................................ 9
Figure 8. Block diagram (STM707/708) ................................................................. 10
Figure 9. Hardware hookup ....................................................................................... 10
Figure 10. Reset output valid to ground circuit ......................................................... 12
Figure 11. Interfacing to microprocessors with bidirectional reset I/O ....................... 13
Figure 12. Supply current vs. temperature (no load) ............................................... 14
Figure 13. VPFI threshold vs. temperature ............................................................... 14
Figure 14. Reset comparator propagation delay vs. temperature .......................... 15
Figure 15. Power-up trec vs. temperature ............................................................... 15
Figure 16. Normalized reset threshold vs. temperature .......................................... 16
Figure 17. Watchdog time-out period vs. temperature ........................................... 16
Figure 18. PFI to PFO propagation delay vs. temperature ....................................... 17
Figure 19. Output voltage vs. load current (VCC = 5 V; TA = 25 °C) .................... 17
Figure 20. RST output voltage vs. supply voltage ................................................... 18
Figure 21. RST output voltage vs. supply voltage ................................................... 18
Figure 22. RST response time (assertion) .............................................................. 19
Figure 23. RST response time (assertion) .............................................................. 19
Figure 24. Power-fail comparator response time (assertion) .................................. 20
Figure 25. Power-fail comparator response time (de-assertion) .......................... 21
Figure 26. Maximum transient duration vs. reset threshold overdrive .................. 21
Figure 27. AC testing input/output waveforms ...................................................... 23
Figure 28. Power-fail comparator waveform .......................................................... 23
Figure 29. MR timing waveform ........................................................................... 24
Figure 30. Watchdog timing (STM705/706/813L) ................................................. 24
Figure 31. SO8 – 8-lead plastic small outline, 150 mils body width, outline .......... 28
Figure 32. TSSOP8 – 8-lead, thin shrink small outline, 3 x 3 mm body size, outline 29
1 Description

The STM705/706/707/708/813L supervisors are self-contained devices which provide microprocessor supervisory functions. A precision voltage reference and comparator monitors the $V_{CC}$ input for an out-of-tolerance condition. When an invalid $V_{CC}$ condition occurs, the reset output ($RST$) is forced low (or high in the case of $RST$).

These devices also offer a watchdog timer (except for STM707/708) as well as a power-fail comparator to provide the system with an early warning of impending power failure.

These devices are available in a standard 8-pin SOIC package or a space-saving 8-pin TSSOP package.

Figure 1. Logic diagram (STM705/706/813L)

1. For STM705/706 only.
2. For STM813L only.

Figure 2. Logic diagram (STM707/708)
Table 2. Signal names

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>Push-button reset input</td>
</tr>
<tr>
<td>WDI</td>
<td>Watchdog input</td>
</tr>
<tr>
<td>WDO</td>
<td>Watchdog output</td>
</tr>
<tr>
<td>RST</td>
<td>Active-low reset output</td>
</tr>
<tr>
<td>RST(1)</td>
<td>Active-high reset output</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>PFI</td>
<td>Power-fail input</td>
</tr>
<tr>
<td>PFO</td>
<td>Power-fail output</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>NC</td>
<td>No connect</td>
</tr>
</tbody>
</table>

1. For STM813L only.

Figure 3. STM705/706/813L SO8 connections

Figure 4. STM705/706/813L TSSOP8 connections

1. For STM813L, reset output is active-high.
Figure 5. STM707/708 SO8 connections

```
SO8
1  8  RST
2  7  RST
3  6  NC
4  5  PFO
```

Figure 6. STM707/708 TSSOP8 connections

```
TSSOP8
1  8  NC
2  7  PFO
3  6  PFI
4  5  VSS
```
Pin descriptions

2.1 **MR**
A logic low on MR asserts the reset output. Reset remains asserted as long as MR is low and for t_{rec} after MR returns high. This active-low input has an internal pull-up. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.

2.2 **WDI**
If WDI remains high or low for 1.6 s, the internal watchdog timer runs out and reset (or WDO) is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge.

The watchdog function can be disabled by allowing the WDI pin to float.

2.3 **WDO**
It goes low when a transition does not occur on WDI within 1.6 s, and remains low until a transition occurs on WDI (indicating the watchdog interrupt has been serviced). WDO also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output, WDO goes high as soon as V_{CC} exceeds the reset threshold. Output type is push-pull.

Note: For those devices with a WDO output, a watchdog timeout will not trigger reset unless WDO is connected to MR.

2.4 **RST**
Pulses low when triggered, and stays low whenever V_{CC} is below the reset threshold or when MR is a logic low. It remains low for t_{rec} after either V_{CC} rises above the reset threshold, or MR goes from low to high.

2.5 **RST**
Goes high with triggered, and stays high whenever V_{CC} is above the reset threshold or when MR is a logic high. It stays high for t_{rec} after either V_{CC} falls below the reset threshold, or MR goes from high to low.

2.6 **PFI**
When PFI is less than V_{PFI}, PFΩ goes low; otherwise, PFΩ remains high. Connect to ground if unused.
2.7 **PFO**

When PFI is less than \(V_{PFI}\), PFO goes low; otherwise, PFO remains high. Leave open if unused. Output type is push-pull.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MR</td>
<td>Push-button reset input</td>
</tr>
<tr>
<td>6</td>
<td>WDI</td>
<td>Watchdog input</td>
</tr>
<tr>
<td>8</td>
<td>WDO</td>
<td>Watchdog output (push-pull)</td>
</tr>
<tr>
<td>7</td>
<td>RST</td>
<td>Active-low reset output</td>
</tr>
<tr>
<td>7</td>
<td>RST</td>
<td>Active-high reset output</td>
</tr>
<tr>
<td>2</td>
<td>(V_{CC})</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>4</td>
<td>PFI</td>
<td>Power-fail input</td>
</tr>
<tr>
<td>5</td>
<td>PFO</td>
<td>Power-fail output (push-pull)</td>
</tr>
<tr>
<td>3</td>
<td>(V_{SS})</td>
<td>Ground</td>
</tr>
<tr>
<td>—</td>
<td>NC</td>
<td>No connect</td>
</tr>
</tbody>
</table>

1. For STM813L only.

---

STM705, STM706, STM707, STM708, STM813L

**Pin descriptions**

**Table 3. Pin description**

**Figure 7. Block diagram (STM705/706/813L)**

1. For STM813L only.
Figure 8. Block diagram (STM707/708)

Figure 9. Hardware hookup

1. For STM705/706/813L.
3 Operation

3.1 Reset output

The STM705/706/707/708/813L supervisor asserts a reset signal to the MCU whenever V\text{CC} goes below the reset threshold (V\text{RST}), a watchdog time-out occurs (if WDO is tied to MR), or when the push-button reset input (MR) is taken low. RST is guaranteed to be a logic low (logic high for STM707/708/813L) for V\text{CC} < V\text{RST} down to V\text{CC} = 1 V for T\text{A} = 0 °C to 85 °C. During power-up, once V\text{CC} exceeds the reset threshold an internal timer keeps RST low for the reset time-out period, t\text{rec}. After this interval RST returns high. If V\text{CC} drops below the reset threshold, RST goes low. Each time RST is asserted, it stays low for at least the reset time-out period (t\text{rec}). Any time V\text{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V\text{CC} returns above the reset threshold.

3.2 Push-button reset input

A logic low on MR asserts reset. Reset remains asserted while MR is low, and for t\text{rec} (see Figure 29) after it returns high. The MR input has an internal 40 Ω pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from MR to GND to create a manual reset function; external debounce circuitry is not required. If MR is driven from long cables or the device is used in a noisy environment, connect a 0.1 μF capacitor from MR to GND to provide additional noise immunity. MR may float, or be tied to V\text{CC} when not used.

3.3 Watchdog input (STM705/706/813L)

The watchdog timer can be used to detect an out-of-control MCU. If the MCU does not toggle the Watchdog Input (WDI) within t\text{WD} (1.6 s), the reset is asserted. The internal 1.6s timer is cleared by either:

1. a reset pulse, or
2. by toggling WDI (high-to-low or low-to-high), which can detect pulses as short as 50 ns. If WDI is tied high or low, a reset pulse is triggered every 1.8 s (t\text{WD} + t\text{rec}), if WDO is connected to MR.

See Figure 30 for STM705/706/813L.

The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting.

Note: The watchdog function may be disabled by floating WDI or tri-stating the driver connected to WDI. When tri-stated or disconnected, the maximum allowable leakage current is 10 μA and the maximum allowable load capacitance is 200 pF.
3.4 **Watchdog output (STM705/706/813L)**

When $V_{CC}$ drops below the reset threshold, $WDO$ will go low even if the watchdog timer has not yet timed out. However, unlike the reset output, $WDO$ goes high as soon as $V_{CC}$ exceeds the reset threshold. $WDO$ may be used to generate a reset pulse by connecting it to the $MR$ input.

3.5 **Power-fail input/output**

The power-fail input (PFI) is compared to an internal reference voltage (independent from the $V_{RST}$ comparator). If PFI is less than the power-fail threshold ($V_{PFI}$), the power-fail output (PFO) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see Figure 9) to either the unregulated DC input (if it is available) or the regulated output of the $V_{CC}$ regulator. The voltage divider can be set up such that the voltage at PFI falls below $V_{PFI}$ several milliseconds before the regulated $V_{CC}$ input to the STM705/706/707/708/813L or the microprocessor drops below the minimum operating voltage.

If the comparator is unused, PFI should be connected to $VSS$ and PFO left unconnected. PFO may be connected to $MR$ on the STM703/704/818 so that a low voltage on PFI will generate a reset output.

3.6 **Ensuring a valid reset output down to $V_{CC} = 0$ V**

When $V_{CC}$ falls below 1 V, the state of the RST output can no longer be guaranteed, and becomes essentially an open circuit. If a high value pulldown resistor is added to the RST pin, the output will be held low during this condition. A resistor value of approximately 100 k$\Omega$ will be large enough to not load the output under operating conditions, but still sufficient to pull RST to ground during this low voltage condition (see Figure 10).

![Figure 10. Reset output valid to ground circuit](image)
3.7 Interfacing to microprocessors with bidirectional reset pins

Microprocessors with bidirectional reset pins can contend with the STM705-708 reset output. For example, if the reset output is driven high and the micro wants to pull it low, signal contention will result. To prevent this from occurring, connect a 4.7 kΩ resistor between the reset output and the micro's reset I/O as in Figure 11.

Figure 11. Interfacing to microprocessors with bidirectional reset I/O

![Diagram of interfacing to microprocessors with bidirectional reset I/O]

Buffered reset to other system components
4 Typical operating characteristics

Typical values are at $T_A = 25 \, ^\circ C$.

**Figure 12. Supply current vs. temperature (no load)**

**Figure 13. $V_{PI}$ threshold vs. temperature**
Figure 14. Reset comparator propagation delay vs. temperature

![Graph showing the propagation delay vs. temperature for different VCC values.](image)

Temperature (°C)

-40 -20 0 20 40 60 80 100 120

Propagation delay (µs)

10 12 14 16 18 20 22 24 26 28 30

Figure 15. Power-up $t_{\text{rec}}$ vs. temperature

![Graph showing the t_{rec} vs. temperature for different VCC values.](image)

Temperature (°C)

-40 -20 0 20 40 60 80 100 120

$t_{\text{rec}}$ (µs)

210 215 220 225 230 235 240

VCC = 3.0 V

VCC = 4.5 V

VCC = 5.5 V
Figure 16. Normalized reset threshold vs. temperature

![Normalized reset threshold vs. temperature graph](image)

Figure 17. Watchdog time-out period vs. temperature

![Watchdog time-out period vs. temperature graph](image)
Figure 18. PFI to PFO propagation delay vs. temperature

![Graph showing PFI to PFO propagation delay vs. temperature.

Figure 19. Output voltage vs. load current ($V_{CC} = 5$ V; $T_A = 25$ °C)

![Graph showing output voltage vs. load current.](A110496)
Figure 20. RST output voltage vs. supply voltage

Figure 21. RST output voltage vs. supply voltage
Figure 22. $\overline{\text{RST}}$ response time (assertion)

1. $V_{\text{RST}} = 4.603\, \text{V at 25 } ^\circ\text{C.}$
1. \( V_{\text{RST}} = 4.603 \, \text{V} \) at 25 °C.

**Figure 23. RST response time (assertion)**

**Figure 24. Power-fail comparator response time (assertion)**
Figure 25. Power-fail comparator response time (de-assertion)

Figure 26. Maximum transient duration vs. reset threshold overdrive

Reset occurs above the curve.
5 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
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<tbody>
<tr>
<td>T_{STG}</td>
<td>Storage temperature (V_{CC} Off)</td>
<td>–55 to 150</td>
<td>°C</td>
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<tr>
<td>T_{SLD}^{(1)}</td>
<td>Lead solder temperature for 10 seconds</td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>V_{IO}</td>
<td>Input or output voltage</td>
<td>–0.3 to V_{CC} +0.3</td>
<td>V</td>
</tr>
<tr>
<td>V_{CC}</td>
<td>Supply voltage</td>
<td>–0.3 to 7.0</td>
<td>V</td>
</tr>
<tr>
<td>I_{O}</td>
<td>Output current</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>P_{D}</td>
<td>Power dissipation</td>
<td>320</td>
<td>mW</td>
</tr>
</tbody>
</table>

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
6 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in Table 5. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC measurement conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>STM705/706/707/708; STM813L</th>
<th>Unit</th>
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<tbody>
<tr>
<td>$V_{CC}$ supply voltage</td>
<td>1.0 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Ambient operating temperature ($T_A$)</td>
<td>–40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Input rise and fall times</td>
<td>$\leq 5$</td>
<td>ns</td>
</tr>
<tr>
<td>Input pulse voltages</td>
<td>0.2 to 0.8 $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>Input and output timing ref. voltages</td>
<td>0.3 to 0.7 $V_{CC}$</td>
<td>V</td>
</tr>
</tbody>
</table>

Figure 27. AC testing input/output waveforms

Figure 28. Power-fail comparator waveform
1. RST for STM805.

Figure 29. MR timing waveform

Figure 30. Watchdog timing (STM705/706/813L)
### Table 6. DC and AC characteristics

<table>
<thead>
<tr>
<th>Sym</th>
<th>Description</th>
<th>Test condition(1)</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<td>$V_{CC}$</td>
<td>Operating voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>$I_{CC}$</td>
<td>$V_{CC}$ supply current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{LI}$</td>
<td>Input leakage current (MR)</td>
<td>$4.5 , V &lt; V_{CC} &lt; 5.5 , V$</td>
<td>75</td>
<td>125</td>
<td>300</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>Input leakage current (PFI)</td>
<td>$0 , V &lt; V_{IN} &lt; V_{CC}$</td>
<td>−25</td>
<td>2</td>
<td>+25</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>Input leakage current (WDI)</td>
<td>$V_{WDI} = V_{CC}$, time average</td>
<td>120</td>
<td>160</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{WDI} = GND$, time average</td>
<td>−20</td>
<td>−15</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input high voltage (MR)</td>
<td>$4.5 , V &lt; V_{CC} &lt; 5.5 , V$</td>
<td></td>
<td>2.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input high voltage (WDI)</td>
<td>$V_{RST , (max)} &lt; V_{CC} &lt; 5.5 , V$</td>
<td>0.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input low voltage (MR)</td>
<td>$4.5 , V &lt; V_{CC} &lt; 5.5 , V$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input low voltage (WDI)</td>
<td>$V_{RST , (max)} &lt; V_{CC} &lt; 5.5 , V$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output low voltage (PFO, RST, RST, WDO)</td>
<td>$V_{CC} = V_{RST , (max)}$, $I_{SINK} = 3.2 , mA$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output low voltage (RST)</td>
<td>$I_{SINK} = 50 , μA$, $V_{CC} = 1.0 , V$, $T_{A} = 0 , ^{\circ}C$ to 85 $^{\circ}C$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{SINK} = 100 , μA$, $V_{CC} = 1.2 , V$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output high voltage (RST, RST, WDO)</td>
<td>$I_{SOURCE} = 1 , mA$, $V_{CC} = V_{RST , (max)}$</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output high voltage (PFO)</td>
<td>$I_{SOURCE} = 75 , μA$, $V_{CC} = V_{RST , (max)}$</td>
<td>0.8</td>
<td>$V_{CC}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output high voltage (RST)</td>
<td>$I_{SOURCE} = 4 , μA$, $V_{CC} = 1.1 , V$, $T_{A} = 0 , ^{\circ}C$ to 85 $^{\circ}C$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{SOURCE} = 4 , μA$, $V_{CC} = 1.2 , V$</td>
<td>0.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

#### Power-fail comparator

| $V_{PFI}$ | PFI input threshold                                      | PFI falling ($V_{CC} = 5 \, V$) | 1.20  | 1.25 | 1.30  | V    |
| $t_{PFD}$ | PFI to PFO propagation delay                            |                                 | 2     |      |       | μs   |
### Table 6. DC and AC characteristics

<table>
<thead>
<tr>
<th>Sym</th>
<th>Description</th>
<th>Test condition(1)</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Reset thresholds</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{RST}</td>
<td>Reset threshold(3)</td>
<td>STM705/707/813L</td>
<td>4.50</td>
<td>4.65</td>
<td>4.75</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>STM706/708</td>
<td>4.25</td>
<td>4.40</td>
<td>4.50</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Reset threshold hysteresis</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>t_{rec}</td>
<td>RST pulse width</td>
<td>Blank (see Table 9)</td>
<td>140</td>
<td>200</td>
<td>280</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A (see Table 9)</td>
<td>160</td>
<td>200</td>
<td>280</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Push-button reset input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{MLMH} (or t_{MR})</td>
<td>MR pulse width</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{MLRL} (t_{MRD})</td>
<td>MR to RST output delay</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td><strong>Watchdog timer (STM705/706/813L)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{WD}</td>
<td>Watchdog timeout period</td>
<td>4.5 V &lt; V_{CC} &lt; 5.5 V</td>
<td>1.12</td>
<td>1.60</td>
<td>2.24</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td>WDI pulse width</td>
<td>4.5 V &lt; V_{CC} &lt; 5.5 V</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 4.75 V to 5.5 V for STM705/707/813L; V_{CC} = 4.5 V to 5.5 V for STM706/708 (except where noted).
2. V_{CC} (min) = 1.0 V for T_A = 0 °C to +85 °C.
3. For V_{CC} falling.
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.
Figure 31. SO8 – 8-lead plastic small outline, 150 mils body width, outline

1. Drawing is not to scale.

Table 7. SO8 - 8-lead plastic small outline, 150 mils body width, pack. mech. data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>mm</th>
<th>inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Typ</td>
<td>Min</td>
</tr>
<tr>
<td>A</td>
<td>—</td>
<td>1.35</td>
</tr>
<tr>
<td>A1</td>
<td>—</td>
<td>0.10</td>
</tr>
<tr>
<td>B</td>
<td>—</td>
<td>0.33</td>
</tr>
<tr>
<td>C</td>
<td>—</td>
<td>0.19</td>
</tr>
<tr>
<td>D</td>
<td>—</td>
<td>4.80</td>
</tr>
<tr>
<td>ddd</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>E</td>
<td>—</td>
<td>3.80</td>
</tr>
<tr>
<td>e</td>
<td>1.27</td>
<td>—</td>
</tr>
<tr>
<td>H</td>
<td>—</td>
<td>5.80</td>
</tr>
<tr>
<td>h</td>
<td>—</td>
<td>0.25</td>
</tr>
<tr>
<td>L</td>
<td>—</td>
<td>0.40</td>
</tr>
<tr>
<td>α</td>
<td>—</td>
<td>0°</td>
</tr>
<tr>
<td>N</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>
Table 8. TSSOP8 - 8-lead, thin shrink small outline, 3 x 3 mm body size, mechanical data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>mm</th>
<th>inches</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Typ</td>
<td>Min</td>
<td>Max</td>
<td>Typ</td>
</tr>
<tr>
<td>A</td>
<td>—</td>
<td>—</td>
<td>1.10</td>
<td>—</td>
</tr>
<tr>
<td>A1</td>
<td>—</td>
<td>0.05</td>
<td>0.15</td>
<td>—</td>
</tr>
<tr>
<td>A2</td>
<td>0.85</td>
<td>0.75</td>
<td>0.95</td>
<td>0.034</td>
</tr>
<tr>
<td>b</td>
<td>—</td>
<td>0.25</td>
<td>0.40</td>
<td>—</td>
</tr>
<tr>
<td>c</td>
<td>—</td>
<td>0.13</td>
<td>0.23</td>
<td>—</td>
</tr>
<tr>
<td>CP</td>
<td>—</td>
<td>—</td>
<td>0.10</td>
<td>—</td>
</tr>
<tr>
<td>D</td>
<td>3.00</td>
<td>2.90</td>
<td>3.10</td>
<td>0.118</td>
</tr>
<tr>
<td>e</td>
<td>0.65</td>
<td>—</td>
<td>—</td>
<td>0.026</td>
</tr>
<tr>
<td>E</td>
<td>4.90</td>
<td>4.65</td>
<td>5.15</td>
<td>0.193</td>
</tr>
<tr>
<td>E1</td>
<td>3.00</td>
<td>2.90</td>
<td>3.10</td>
<td>0.118</td>
</tr>
<tr>
<td>L</td>
<td>0.55</td>
<td>0.40</td>
<td>0.70</td>
<td>0.022</td>
</tr>
<tr>
<td>L1</td>
<td>0.95</td>
<td>—</td>
<td>—</td>
<td>0.037</td>
</tr>
<tr>
<td>α</td>
<td>—</td>
<td>0°</td>
<td>6°</td>
<td>—</td>
</tr>
<tr>
<td>N</td>
<td>8</td>
<td>8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
8 Part numbering

Table 9. Ordering information scheme

<table>
<thead>
<tr>
<th>Example:</th>
<th>STM705</th>
<th>Y</th>
<th>M</th>
<th>6</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device type and reset threshold voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>STM705/707/813L = VRST = 4.50 V to 4.75 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>STM706/708 = VRST = 4.25 V to 4.50 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Y = automotive grade(^{(1)})((^{(4)}))</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>RST pulse width</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Blank = 140 to 280 ms</td>
</tr>
<tr>
<td>A(^{(2)}) = 160 to 280 ms</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Package</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>M = SO8</td>
</tr>
<tr>
<td>DS(^{(3)}) = TSSOP8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Temperature range</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>6 = –40 to 85 °C</td>
</tr>
<tr>
<td>7 = –40 to 125 °C(^{(4)})</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Shipping method</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>F = ECOPACK(^{(5)}) package, tape and reel</td>
</tr>
</tbody>
</table>

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.
2. Available for STM706/708 in SO8 (M) package only.
3. Contact local ST sales office for availability.
4. Available for the STM706 only.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.
<table>
<thead>
<tr>
<th>Part number</th>
<th>Reset threshold</th>
<th>Package</th>
<th>Topside marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>STM705</td>
<td>4.63 V</td>
<td>SO8</td>
<td>705</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TSSOP8</td>
<td></td>
</tr>
<tr>
<td>STM706</td>
<td>4.38 V</td>
<td>SO8</td>
<td>706&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TSSOP8</td>
<td></td>
</tr>
<tr>
<td>STM707</td>
<td>4.63 V</td>
<td>SO8</td>
<td>707</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TSSOP8</td>
<td></td>
</tr>
<tr>
<td>STM708</td>
<td>4.38 V</td>
<td>SO8</td>
<td>708</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TSSOP8</td>
<td></td>
</tr>
<tr>
<td>STM813L</td>
<td>4.63 V</td>
<td>SO8</td>
<td>813L</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TSSOP8</td>
<td></td>
</tr>
</tbody>
</table>

1. The topside marking for the part number STM706YM7F is “706Y”.
## Revision history

### Table 11. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sep-2003</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>31-Oct-2003</td>
<td>1.1</td>
<td>Update Table 6.</td>
</tr>
<tr>
<td>12-Dec-2003</td>
<td>2</td>
<td>Reformatted; update characteristics (Figure 1, 2, 3, 4, 6, 8, 9, 10, 28; 29, 30, Table 7, 9, 11)</td>
</tr>
<tr>
<td>16-Jan-2004</td>
<td>2.1</td>
<td>Add typical characteristics (Figure 12 to 18, 20 to 26)</td>
</tr>
<tr>
<td>09-Apr-2004</td>
<td>3</td>
<td>Reformatted; update characteristics (Figure 14, 18, 20 to 23, 26; Table 7)</td>
</tr>
<tr>
<td>25-May-2004</td>
<td>4</td>
<td>Update characteristics (Table 4, 7)</td>
</tr>
<tr>
<td>02-Jul-2004</td>
<td>5</td>
<td>Document promoted; corrected waveform (Figure 28)</td>
</tr>
<tr>
<td>21-Sep-2004</td>
<td>6</td>
<td>Clarify root part numbers, pin descriptions (Figure 2, 3, 10; Table 6, 7, 10)</td>
</tr>
<tr>
<td>08-Mar-2005</td>
<td>7</td>
<td>Update typical characteristics (Figure 12 to 26)</td>
</tr>
<tr>
<td>02-Nov-2009</td>
<td>8</td>
<td>Updated Table 1, 3, 4, 6, 9, Section 2.3, Section 2.7, text in Section 7.</td>
</tr>
<tr>
<td>06-Aug-2010</td>
<td>9</td>
<td>Updated Features, Section 4: Typical operating characteristics, Table 9.</td>
</tr>
<tr>
<td>26-Mar-2014</td>
<td>10</td>
<td>Added automotive grade option for the STM706 to Features, Table 1: Device summary, and Table 9: Ordering information scheme</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Removed shipping option in tubes from Table 9: Ordering information scheme</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added footnote 1 to Table 10: Marking description</td>
</tr>
</tbody>
</table>
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