STNRG599

Datasheet

Resonant half bridge controller

Product status link

STNRG599

Product label

SUSTAINABLE TECHNOLOGY

Features

- Phase shift control (PSC) of resonant half-bridge for enhanced dynamic performance and wide input voltage range operation
- Up to 750 kHz maximum frequency with self-adjusting dead-time
- Burst mode operation enables very low open-load input power consumption
- Full protection set: Overcurrent, overpower, DC brown-OUT/IN, hard-switch prevention (HSP) function for anti-capacitive protection and safe startup
- 600 V rail compatible high-side gate driver with integrated bootstrap diode and high dV/dt immunity
- High-voltage startup
- X-capacitor discharge (STNRG599A)
- -300/800 mA high-side and low-side gate drivers with UVLO pull-down
- SO16N package

Application

- SMPS for led TV, desktop, and all-in-one PC
- High-power LED lighting modules
- Consumer and industrial SMPS
- High-end AC-DC adapter, open frame SMPS

Description

The STNRG599 is a double-ended controller designed for series-resonant topologies, supporting both LLC and LCC configurations.

The IC provides two complementary outputs that drive the high-side and low-side MOSFET 180° out of phase. The dead time inserted between the turn-off of one switch and the turn-on of the other is automatically adjusted to fit the transition

times of the half-bridge midpoint, ensuring zero voltage switching across the entire operating range.

Output voltage (or current) regulation is obtained by directly controlling the phase shift between the half-bridge voltage and the resonant tank current. This proprietary control method, called phase shift control (PSC), enhances dynamic behavior and input voltage ripple rejection. Additionally, it makes the control loop with small sensitivity to component tolerance in the LLC / LCC resonant tank.

At light load, STNRG599 enters a controlled burst-mode operation, enabling intermittent converter operation. This reduces the average switching frequency and minimize the open-load input power.

STNRG599 is equipped with a full set of protection features: hard-switch prevention and anti-capacitive protection, 1st and 2nd level overcurrent protection, delayed shutdown and restart function based on pin DELAY (for user-programmable delayed shutdown upon overload with automatic restart). On the whole, OCP1, OCP2, and functions based on pin DELAY provide reliable and robust management of conditions such as short-time overcurrent, continuous overload, and severe output short-circuit.

DC brown-out/in protection is not latched. It is implemented at the input pin LINE, with constant hysteresis between brown-out and brown-in thresholds. The function prevents converter operation outside the selected DC input voltage range.

1 Device and system block diagrams

Figure 1. **Device block diagram**

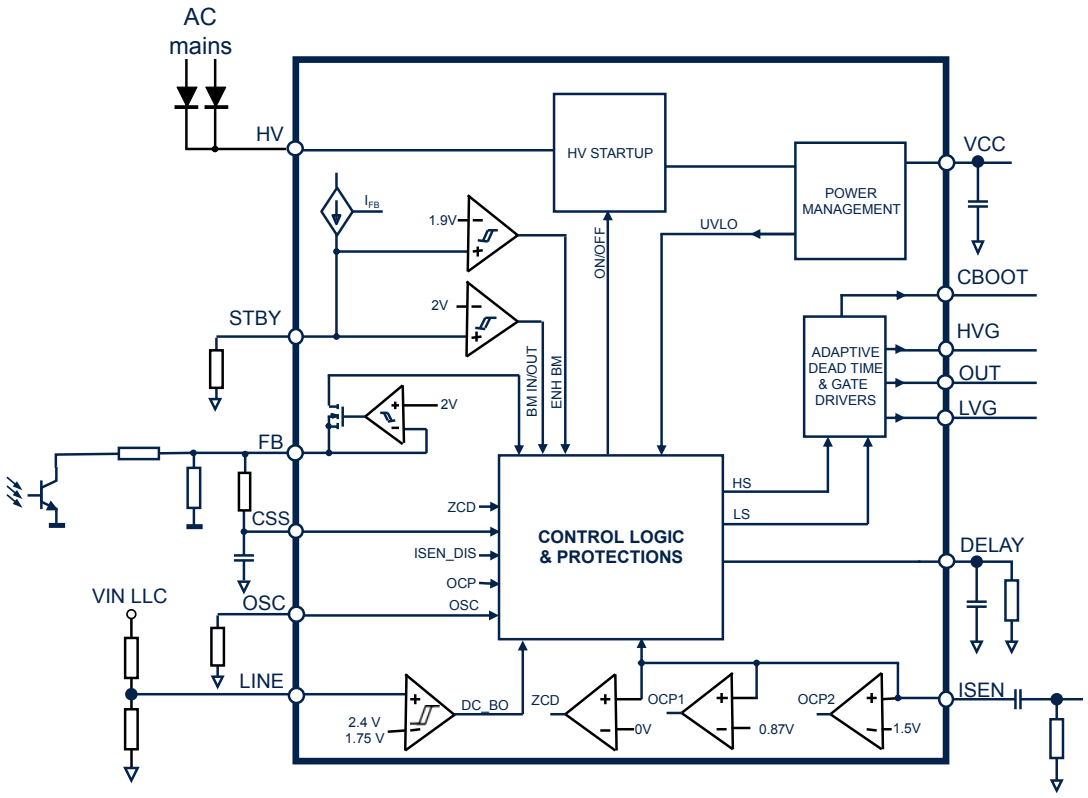
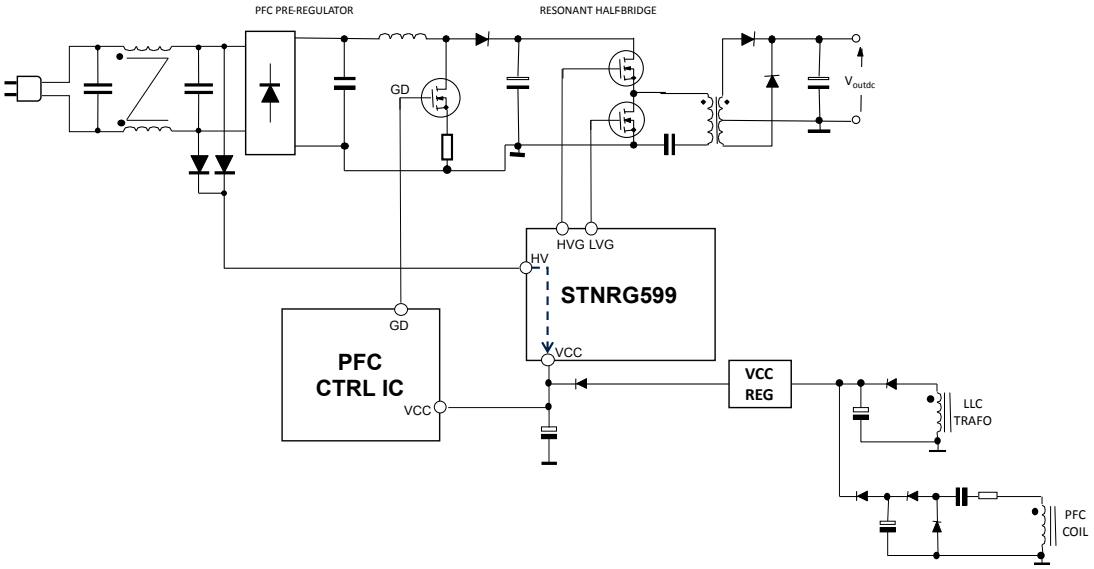


Table 1. **Device information**

Order code	XCAP discharge function	Package marking
STNRG599A	Enabled	STNRG599A
STNRG599B	Disabled	STNRG599B

Figure 2. Typical system diagram



2 Device pinout and pin description

Figure 3. **Device pinout (top view)**

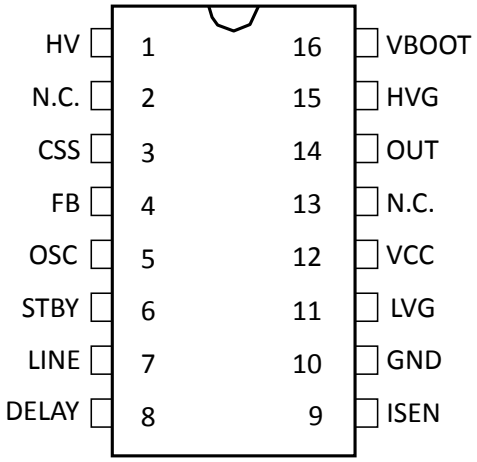


Table 2. **Pin description**

N.	Name	Function
1	HV	High-voltage start-up generator and AC voltage sensing input for X-capacitor discharge. The pin can withstand 800 V and must be connected to the AC side of the input rectifier bridge, via a pair of diodes (1N400x type) with common cathode, to sense the AC input voltage. If the pin voltage is higher than 30 V (max), then an internal circuit charges the external capacitor connected between the pin VCC and ground. The first charging period is done at low current (1 mA, typ) to guarantee IC safety, in case the pin VCC is shorted to ground. When VCC > 1.2 V (typ), the charging current increases to about 9 mA, and VCC is brought to VCCon (16.5 V, typ), at which point the control IC operation can start. After VCCon has been triggered, the HVSU generator is kept on for about 80 ms, then it is turned off. In relation to fault management, each time a fault is released, if no other valid faults are present, the HVSU generator is turned on to charge VCC to VCCon. The purpose of the HVSU turn-on at fault release is twofold: one, it guarantees the necessary condition (VCC ≥ VCCon) for restarting the switching activity; two, it ensures that the restart of the switching activity, happening when VCC is close to VCCoff, cannot turn off the IC. X-capacitor discharge function (STNRG599A): when mains voltage disconnection is detected by the dedicated internal circuitry, the HVSU generator is activated to discharge the X-capacitors of the EMI filter to a safe level. In this way, the converter can meet safety regulations without using the traditional discharge resistor in parallel to the X-capacitor that is between the phase conductor and the neutral conductor, thus enabling low-power consumption in open load according to efficiency standards. X-capacitor discharge function is disabled in the STNRG599B.
2	N.C.	High-voltage spacer not internally connected. Purpose: to isolate high-voltage section and foster compliance with safety regulations (creepage distance) on the PCB.
3	CSS	Half-bridge soft-start. The soft-start function is implemented by connecting a capacitor, C_{SS}, from the pin CSS to ground, and a resistor, R_{SS}, from the pin CSS to the pin FB. R_{SS} and C_{SS} set both the initial phase and the time constant of the soft start procedure. An internal switch (120 Ω, typ) fully discharges C_{SS} each time the IC is turned off (that is, when VCC < VCCoff, ISEN > 1.5 V, LINE < 1.75 V, LINE > 3.1 V, DELAY > 1 V). In this way, a complete soft start occurs when the IC turns on again.

N.	Name	Function
		For the sake of precision, after a fault, the restart of the switching activity is allowed only after C_{SS} has been discharged to less than 100 mV (necessary condition for the restart of the switching activity). The internal switch is also shortly activated (5 us, typ) when ISEN > 0.87 V (OCP1 event). In this way, the operating phase is temporarily increased and the power transfer is limited. CSS > 1 V: STBY enabled. CSS > 300 mV: OCP1 and OCP2 enabled. The enable of STBY, OCP1, and OCP2 by CSS is reset by any fault (= event stops switching, apart from burst mode operation). In detail, the reset conditions are: • DELAY = 1.75 V • VCC = VCCon after that VCC = VCCoff (while VCC is toggling and DELAY = GND) • LINE = 2.4 V after that LINE = 1.75 V (in case DELAY = GND and VCC > VCCon)
4	FB	Feedback pin and min/max phase shift setup. The pin, which provides an accurate 2 V voltage reference, is connected to the collector of the optocoupler that sustains the feedback loop. The current sunk by the optocoupler, i.e. sourced by the pin, is mirrored inside the IC to build the feedback signal. A resistor, R_{PHMIN}, between pin FB and ground defines the minimum feedback current mirrored into the IC and, therefore, the minimum phase shift the control loop can set. In this way, the maximum power that can be transferred is set. A resistor, R_{PHMAX}, in series between pin FB and the collector of the optocoupler, is necessary to limit the current sourced by the pin itself. The typical maximum sourced current is 500 uA, so the typical value of the resistor is 4 kΩ. This resistor also defines the maximum phase shift the control loop can set (the maximum phase shift defined by R_{PHMAX} is usually overwritten by the burst mode threshold that is programmed at pin STBY). Max C = 100 pF.
5	OSC	Internal oscillator. The current source for the internal oscillator is programmed by the resistor, R_{OSC}, connected between the pin and ground. A capacitor in parallel may be required for filtering purposes. Max C = 100 pF. Max sourced current = 500 uA.
6	STBY	Burst mode operation. A resistor, R_{STBY}, between pin STBY and ground, defines the feedback current and the corresponding phase shift at which burst mode operation starts. When V_{STBY} goes above 2 V, the switching activity is stopped. The voltage hysteresis on pin STBY is 125 mV: the switching activity is restarted when V_{STBY} goes below 1.875 V. Enhanced burst mode: as the voltage on pin STBY rises across 1.9 V, the feedback current mirrored into the IC is reduced by 30% to reduce the phase shift between the half-bridge voltage and the resonant tank current, during the switching packet, thus increasing the energy transferred by each switching cycle. The 30% reduction of the feedback current mirrored into the IC is removed when V_{STBY} goes above 2.0 V, that is, the threshold at which the switching activity is stopped. Burst mode operation is disabled as long as V_{CSS} < 1 V. STBY is enabled when V_{CSS} goes above 1 V (reset by DELAY = 1.75 V). Internal replica of V_{STBY} is bottom clamped. The external effect is that, when VCC reaches 6 V during turn-on, V_{STBY} rises to about 1.5 V · $R_{STBY}/(R_{STBY}+R_{INT})$ with R_{INT} = 102 kΩ (typ).
7	LINE	Line sensing input: DC brown-out/in + OVP protection + Feedback failure disconnection

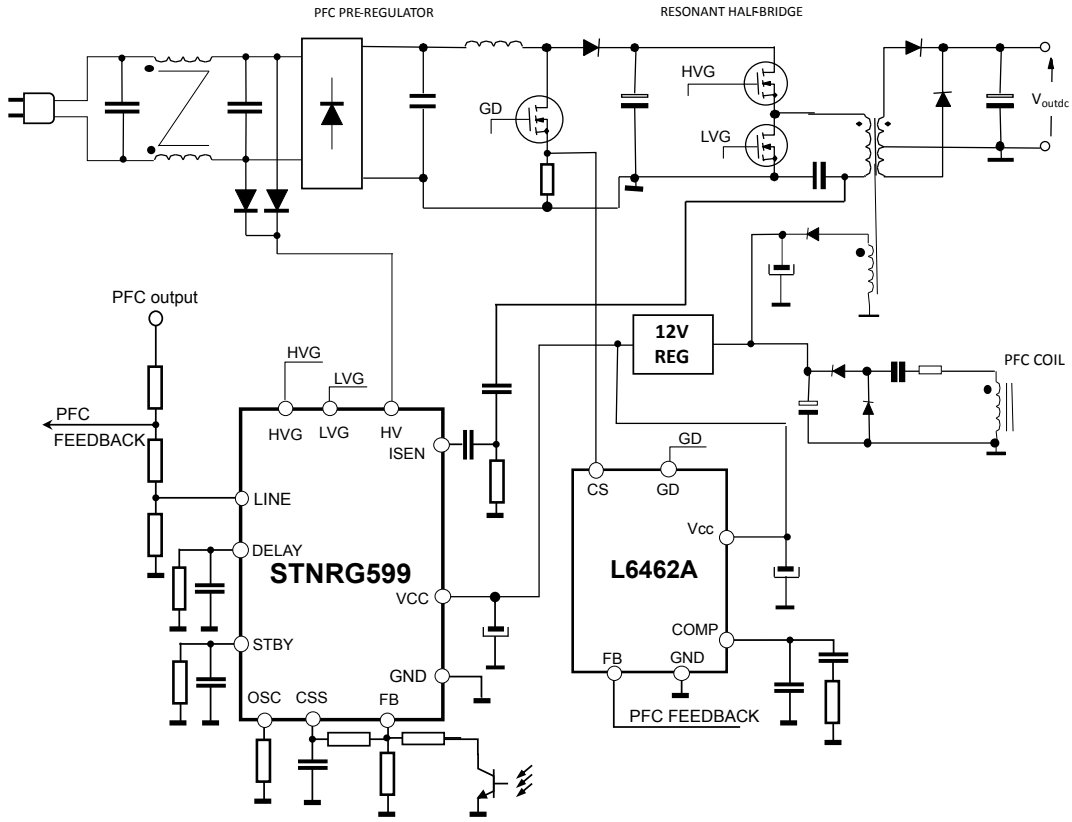
N.	Name	Function
		The pin monitors the input voltage of the half-bridge by means of an external resistive divider. The IC is enabled when V_{LINE} > 2.4 V (typ) and disabled when V_{LINE} < 1.75 V (typ). The soft-start capacitor C_{SS} is completely discharged when V_{LINE} < 1.75 V, so that the whole soft-start process can take place when V_{LINE} > 2.4 V. A small RC filter (R up to 100 Ω, C up to 10 nF) from pin LINE to ground might be needed to filter noise. If the pin is pulled to 3.1 V (typ, 200 mV hysteresis), then the turn-off procedure based on pin DELAY is activated: the switching activity is immediately stopped, the soft-start capacitor C_{SS} is completely discharged, and the internal 250 uA current source is kept on until V_{DELAY} = 1.75 V. As the voltage on the pin exceeds 1.75 V, the internal 250 uA current source is turned off. The voltage on the pin then decays because of R_{DELAY} and, also in this case, the IC is restarted, following the complete soft-start process, when V_{DELAY} falls below 0.24 V. In both cases: • when the fault is triggered (LINE falling below 1.75 V or LINE rising above 3.1 V), the switching activity is stopped after the running LVG / HVG pulse pair is completed by the control loop • when the fault is released (LINE rising above 2.4 V or LINE falling below 2.9 V), the HVSU can be turned on to bring VCC to VCCon. At this point, the switching activity can restart (provided there is no other active fault). The pin is internally clamped to 3.4 V, typ, to manage feedback failure disconnection of the low-side resistor of the external divider on the input voltage.
8	DELAY	Delayed shutdown and restart upon overload. A capacitor, C_{DELAY}, and a resistor, R_{DELAY}, are connected from this pin to ground to set: • the maximum duration of an overcurrent condition before the IC stops switching and • the delay after which the IC restarts switching. Each time V_{ISEN} > 0.87 V, which is an OCP1 event, C_{DELAY} is charged by an internal 250 µA current source for 5 us (typ.) and then it is slowly discharged by R_{DELAY}. When the voltage on the pin reaches 1 V, • the soft-start capacitor C_{SS} is completely discharged (internal switch, 120 Ω, typ) and • the internal 250 µA current source is kept on until V_{DELAY} = 1.75 V. As the voltage on the pin exceeds 1.75 V, the IC stops switching (after the running LVG / HVG has elapsed) and the internal 250 uA current source is turned off. The voltage on the pin then decays because of R_{DELAY}. When V_{DELAY} reaches 0.24 V, the IC is restarted following the complete soft-start process. In this way, under short-circuit conditions, the converter works intermittently with very low input average power. The switching activity is inhibited when V_{DELAY} is falling from 1.75 V to 0.24 V. If the function is not used, then DELAY can be connected to ground. In this case (DELAY = GND), the DELAY procedure cannot take place when the switching activity is stopped by an OCP2 event (ISEN = 1.5 V) and/or an OVP event (LINE = 3.1 V). Two events can set the HVSU generator: • VCC = VCCoff (occurring when VCC is sustained by the switching activity of the converter, because such switching activity has been stopped by the fault event), • LINE toggling below 1.75 V and above 2.4 V (to be done at application level, to solve the latch that occurs in case VCC cannot reach VCCoff). When DELAY = GND, the internal 250 uA current source that is activated by OCP2 or OVP is turned off at VCC = VCCon, after the activation of the HVSU generator when VCC has reached VCCoff.

N.	Name	Function
		If DELAY = GND and VCC cannot reach VCCoff, then any fault entailing DELAY would latch the converter. The latch can be solved by sensing the fault release at application level and setting a low / high transition to the pin LINE.
9	ISEN	Voltage sensing input of resonant tank current. The resonant tank current can be sensed through a series resistor (lossy sensing) or through a capacitive shunt (lossless sensing). The signal is used to implement the phase-shift control methodology and some protection features. It must sense the resonant current tank: it cannot be shorted to ground or left open. It must be AC coupled by means of a ceramic capacitor around 10 nF. If the voltage at the input terminal of the AC coupling capacitor exceeds 0.87 V (corresponding to OCP1 fault), then two actions take place: • the soft-start capacitor C_{SS} is discharged by the internal switch (120 Ω) at pin CSS for 5 us (typ), and then it is recharged by R_{SS}. • the capacitor C_{DELAY} is charged by an internal 250 µA current source for 5 us (typ.), and then it is slowly discharged by R_{DELAY}. The C_{SS} discharge temporarily increases the current mirrored into the pin FB, so that the phase shift slightly increases, thus limiting the transferred power. Under output short-circuit conditions, the resulting operation of the converter is a nearly constant peak primary current. This condition is allowed for a maximum time set by the delayed shutdown function (see description of pin DELAY). Second-level overcurrent protection, OCP2, is also implemented: if the current keeps building up despite OCP1 protection, or if a large current spike is observed, a comparator referenced to 1.5 V can be triggered (voltage at the input of the AC coupling capacitor). In this case, the following actions take place: • switching is immediately stopped, and a restart procedure based on pin DELAY is activated (HVG pulse reset by OCP2, not by control loop) • the soft-start capacitor C_{SS} is completely discharged, and the internal 250 uA current source is kept on until V_{DELAY} = 1.75 V. As the voltage on the pin exceeds 1.75 V, the internal 250 uA current source is turned off. The voltage on the pin then decays because of R_{DELAY} and, the IC is restarted, following the complete soft-start process, when V_{DELAY} falls below 0.24 V. The switching activity is also conditioned by CSS: it is not allowed when CSS < 0.1 V. OCP1 and OCP2 are disabled when voltage at pin CSS is less than 300 mV. An OCP1 fault is not latched (event not stored in a flip-flop) within the IC: each time the voltage at the input of the AC coupling capacitor at pin ISEN reaches 0.87 V, an internal pulse lasting 5 us is generated to perform the actions described above (C_{SS} discharge and C_{DELAY} charge, for 5 us). An OCP2 fault is latched (event stored in a flip-flop) within the IC: when the voltage at the input of the AC coupling capacitor at pin ISEN reaches 1.5 V, an internal flip-flop is set; such flip-flop is usually reset by DELAY = 1.75 V. In case DELAY = GND, the flip-flip is reset when VCC = VCCon, after the HVSU has been turned on at VCC = VCCoff. If DELAY = GND and VCC cannot reach VCCoff, then the reset must be forced at application level with a low / high transition at pin LINE. VCC = VCCon after VCC = VCCoff and LINE toggling low /high are mechanisms to turn off the internal 250 uA current source (DELAY = GND and/or VCC > VCCoff). The signal at pin is also used to implement the Hard Switch Prevention (HSP) / Anti-Capacitive Protection (ACP) function.
10	GND	IC ground. The pin collects both the return currents of the low side gate driver (pin LVG) and of all the IC biasing circuitry. External biasing components that are referenced to ground must be directly connected to pin GND and the PCB trace(s) must be kept separated from any PCB traces carrying pulsed return currents.
11	LVG	Output of the low side gate driver.

N.	Name	Function
		The driver is capable of 0.3 A source and 0.8 A sink peak current (minimum values, including temperature variation) to drive the low side MOSFET of the half-bridge leg. The pin is actively pulled to ground during UVLO. There is no timeout on the pulse length. The LVG pulse is reset by the control loop.
12	VCC	IC supply voltage. The pin feeds both the signal and biasing part of the IC and the low side gate driver (pin LVG). A bypass ceramic capacitor (100 nF, typ.), from the pin to ground is recommended, while an electrolytic capacitor is necessary to collect the charge from the HVSU generator and to sustain IC operation. At VCC = VCCon (and during normal operation), the switching activity is conditioned by the state of the pins LINE, DELAY, ISEN, CSS according to the following (see corresponding pin description for details): • LINE < 1.75 V or > 3.10 V: no switch • DELAY falling from 1.75 V to 0.24 V: no switch • ISEN > 1.5 V (& CSS > 300 mV): no switch • CSS < 0.1 V: necessary condition for switching During a fault condition, in which VCC is charged / discharged between VCCon and VCCoff, when VCCoff is triggered, CSS is discharged. At VCC = VCCoff, the HVSU generator is turned on. At VCC = VCCon, the internal state is reset. The pins LINE, DELAY, ISEN, CSS are internally polled before the pin VCC reaches VCCon.
13	N.C.	High-voltage spacer not internally connected. Purpose: to isolate high-voltage section and foster compliance with safety regulations (creepage distance) on the PCB.
14	OUT	Floating ground of the high side gate driver. The pin collects the return current of the high side gate driver. Careful layout of the PCB trace is necessary to avoid large negative spikes that can damage the IC, considering that the pin is subject to the full voltage swing of the half-bridge leg.
15	HVG	Output of the high side gate driver. The driver is capable of a 0.3 A source and a 0.8 A sink peak current (minimum values, including temperature variation) to drive the high side MOSFET of the half-bridge leg. An internal resistor connected to pin OUT guarantees that the pin is not floating during UVLO. There is no timeout on the pulse length. The HVG pulse is reset by the control loop or by OCP2.
16	VBOOT	Floating supply voltage of the high side gate driver. The external bootstrap capacitor connected between this pin and pin OUT must be fed by an external bootstrap diode.

3 Typical application schematic

Figure 4. **Typical application schematic**



Note: At both pins LINE and ISEN, an RC filter can be added to suppress high frequency noise usually generated by the switching activity of the power stages. For pin ISEN, RC filter must be placed between the current sensing resistor and the AC coupling capacitor (that is, it must not be directly connected to the pin itself), and its time constant not exceed about 200 nsec, to avoid impacting the control loop. There are no special requirements for the time constant of the RC filter at pin LINE.

4 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	AMR	Unit
V_{HV}	1	Voltage range	-1 to 800	V
V_{VBOOT}	16	Floating supply voltage (referred to GND)	-1 to 620	V
V_{HVG}	15	High side gate driver	V_{OUT}-0.3 to V_{VBOOT} +0.3	V
V_{OUT}	14	Floating ground voltage (referred to GND)	-3 to 600	V
dV_{OUT}/dt	14	Floating ground max. slew rate	50	V/ns
V_{VCC}	11	IC Supply voltage	-0.3 to 20	V
V_{LVG}	12	Low side gate driver	-0.3 to Vcc	V
V_{ISEN}	9	Current sense voltage	-3 to 5.5	V
V_{LINE}	7	Voltage range	-0.3 to 3.6	V
I_{FB}	4	Maximum source current	2	mA
Other pins	3, 4, 5, 6, 8	Analog inputs & outputs voltage range	-0.3 to 3.6	V
ESD HBM	14-15	According to ANSI/ESDA/JEDEC JS-001-2014	±900	V
	1, 3 to 12, 16		±2000	

Stressing the device above the AMR may cause permanent damage of the device.
Device operation at the AMR may affect the device reliability.

5 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Max. thermal resistance, junction-to-ambient (SO16)	120	°C/W
P_{tot}	Power dissipation @Tamb = 50°C (SO16)	0.83	W
T_j	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

6 Electrical characteristics

(T_j = -40 to +125 °C, V_{HV} > 25 V, V_{VCC} = V_{VBOOT} = 15 V, C_{HVG} = C_{LVG} = 1 nF; unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IC SUPPLY VOLTAGE						
V_{VCC}	Operating range	After turn-on	10		19	V
V_{VCCOn}	Turn-on threshold	Voltage rising(1)	15.5	16.5	17.5	V
V_{VCCOff}	Turn-off threshold	Voltage falling(1)	9	9.5	10	V
SUPPLY CURRENT						
I_{op}	Operating supply current	LVG and HVG unloaded		1.5		mA
I_{FAULT}	Residual consumption	V_{DELAY} > 1.75 V or V_{LINE} < 1.75 V		800		µA
I_q	Quiescent current (excluding I_{OSC}, I_{FB})	Idle during burst mode T_j = 27 °C		1		mA
HIGH VOLTAGE START-UP CURRENT GENERATOR						
V_{HV_BD}	Breakdown voltage	I_{HV} < 100 µA	800			V
V_{VCC_SO}	V_{VCC} switch overvoltage: V_{VCC} at which I_{HV_ON} changes from 1 mA to 10 mA			1.1		V
I_{HV_ON}	Current sunk by pin HV to charge pin VCC	V_{HV} >= 30 V V_{VCC} < V_{VCC_SO}	0.4	1	1.7	mA
		V_{HV} >= 30 V 16.5 V < V_{VCC} < 17.5 V	5	9.3	14	mA
I_{HV_OFF}	Off-state leakage current	V_{HV} = 400 V		20	40	µA
T_{TOUT}	Generator shutdown timeout	After V_{VCC} > V_{VCC_ON}	60	80	100	ms
X-CAPACITORS DISCHARGE (STNRG599A)						
V_{HVmin}	Peak residual voltage (application parameter: V_{HVmax} after 1 s from mains disconnection)	$I_{HV,\ DIS}$ > 4.2 mA			40	V
$I_{HV,\ DIS}$	Discharge current	*V_{HV} = 45 V*	4.2			mA
T_{DET}	Detection time (no XCAP if V_{HV} missing for less than T_{DET})		48	64		ms
LINE - HB INPUT VOLTAGE SENSING						
V_{LINE_E}	Enable voltage	Voltage rising(2)	2.33	2.4	2.47	V
V_{LINE_D}	Disable voltage	Voltage falling(2)	1.7	1.75	1.8	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{LINE_PROT}	Protection threshold	Voltage rising(2)	3.01	3.1	3.19	V
$V_{LINE\_PROT\_DIS}$	Disable of protection threshold	Voltage falling(2)	2.81	2.9	2.99	V
V_{LINE_CLAMP}	Protection clamp	Voltage rising(2)	3.2	3.4	3.6	V
I_{LINE_CLAMP}	Clamp current			0.5		mA
ADAPTIVE DEAD-TIME						
T_{D_max}	Maximum dead-time, HB rising		700			ns
	Max variation between DT on rising and DT on falling	DT on falling copied from measured DT on rising. DT on falling > DT on rising			10	%
T_{D_min}	Minimum dead-time, HB rising	Assuming gate fall time + MOSFET off time + HB transition time ≈ 170 ns		270	300	ns
	Max variation between DT on rising and DT on falling	DT on falling copied from measured DT on rising. DT on falling > DT on rising			20	%
T_{D_out}	Watch dog on dead-time	No HSP / ACP		1.2		us
FEEDBACK INPUT (pin FB)						
V_{REF}	Voltage reference(3)		1.93	2	2.07	V
		I_{REF} = -500 uA	1.93	2	2.07	
I_{FBmax}			500			uA
STBY FUNCTION						
K_{STBY}	Mirroring ratio I_{STBY}/I_{FB}	I_{FB} > 50 uA		0.5		
V_{STBY_2V0}(4)	Stop switching threshold $V_{CSS} > V_{CSS\_BME}$	Voltage rising(5)	1.93	2.00	2.07	V
$V_{STBY\_2V0\_LH}$(4)	Local hysteresis of burst mode comparator		10	25	45	mV
V_{STBY_1V9}(4)	Enhanced burst mode comparator	Voltage rising(5)	1.83	1.90	1.97	V
$V_{STBY\_1V9\_LH}$(4)	Local hysteresis of burst mode comparator		10	25	40	mV
$\%I_{FB\_RED}$	% I_{FB} reduction	By design (not tested)		30		%
V_{CSS_BME}	V_{CSS} above which BM is enabled	Voltage rising	09	1	1.1	V
COSC MANAGEMENT AT TURN OFF						
T_{VTIME_RESET}	Time V_{TIME} kept zero after turn-off of LVG/HVG			50		ns
PIN OSC						

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{REF_OSC}	Reference voltage[3]		1.85	2.00	2.15	V
CSS - SOFT START						
I_{LEAK}	Open state current	V_{CSS} = 2 V			1	µA
R_{D_CSS}	Soft-start internal discharge resistor			120		Ω
T_{DISCH}	C_{SS} discharge duration	$V_{ISEN} > V_{ISEN\_OCP1}$		5		µs
ISEN – ZERO CURRENT COMPARATOR						
V_{ISENth_PS}	Zero-current threshold for phase shift control loop	AC value. Internal DC value ≈ 1.65 V	-2	0	2	mV
Note: specified voltage values are referred to the input of the series capacitance at pin ISEN, not to the pin.						
ISEN – PROTECTION COMPARATORS						
I_{SEN}	Input impedance			100		kΩ
V_{ISEN_OCP1}	OCP1 threshold	Voltage rising[6]	0.820	0.870	0.920	V
V_{ISEN_OCP2}	OCP2 threshold	Voltage rising[6]	1.4	1.5	1.6	V
$V_{CSS\_EN\_OCP}$	OCP1,2 enable			300		mV
V_{pos}	Zero current for ACP/HSP		20	40	60	mV
V_{neg}	Zero current for ACP/HSP		-60	-40	-20	mV
Note: specified voltage values are referred to the input of the series capacitance at pin ISEN, not to the pin						
DELAY – DELAYED SHUT DOWN FUNCTION						
I_{LEAK}	Open-state current	V_{DELAY} = 1.8 V			-0.5	µA
I_{CHARGE}	Charge current	V_{DELAY} = 1 V, V_{ISEN} = 0.85 V	180	250	320	µA
V_{TH1}	Threshold at which DELAY procedure is no more reversible	Voltage rising [7]	0.95	1.0	1.05	V
V_{TH2}	Threshold at which switching activity is stopped	Voltage rising[7]	1.65	1.75	1.85	V
V_{TH3}	Restart threshold	Voltage falling[7]	0.14	0.24	0.34	V
LOW-SIDE GATE DRIVER (voltages referred to GND)						
V_{LVGL}	Output low voltage	I_{sink} = 100 mA		0.7	1.5	V
V_{LVGH}	Output high voltage	I_{source} = 10 mA V_{VCC} = 15 V	14.0	14.9		V
t_f	Voltage fall time	From 13.5 V to 1.5 V		25	50	ns
t_r	Voltage rise time	From 1.5 V to 13.5 V	30	43	75	ns
	UVLO saturation[8]	V_{VCC} = 0.5 V, I_{sink} = 1 mA		1	1.5	V
HIGH-SIDE GATE DRIVER (voltages referred to OUT)						
V_{HVGL}	Output low voltage	I_{sink} = 100 mA V_{VBOOT}- V_{OUT} = 15 V		0.7	1.5	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{HVGH}	Output high voltage	I_{source} = 10 mA V_{VBOOT}- V_{OUT} = 15 V	14.0	14.9		V
t_f	Voltage fall time	From 13.5 V to 1.5 V		25	50	ns
t_r	Voltage rise time	From 1.5 V to 13.5 V	30	43	75	ns
R_{PD_HO}	HVG-OUT pull-down		8	25	35	kΩ

1. *Values tracking each other*
2. *Values tracking each other*
3. *Matched voltage references*
4. $V_{STBY\_STOP} = V_{STBY\_2V0}$

   $V_{STBY\_REST} = V_{STBY\_1V9} – V_{STBY\_1V9\_LH}$

   $V_{STBY\_EBM\_ON} = V_{STBY\_1V9}$

   $V_{STBY\_EBM\_OFF} = V_{STBY\_2V0}$
5. *Values tracking each other*
6. *Values tracking each other*
7. *Values tracking each other*
8. *In case of $V_{VCC} < V_{VCCOn}$, if external current is forced into pin LVG, then an internal clamp is activated to avoid external MOSFET turn-on (pin LVG can rise above V_{GSth} because of the external injection). V_{VCC} = 0 → 0.3 V, the UVLO saturation is bypassed by internal parasitic diode and V_{LVG} = 0.6 V typ. V_{VCC} : 0.3 V → 1.1 V, the UVLO saturation is active. V_{VCC} > 1.1 V, the internal LS MOSFET is turned on and pin LVG is kept to ground. Test of UVLO saturation must be done with V_{VCC} around 0.5 V.*

7 Description of operation

7.1 Application information

The STNRG599 is an advanced double-ended controller specific for the resonant half-bridge topology. In these converters, the MOSFETs of the half-bridge leg are alternately switched on and off (180° out-of-phase) to generate a high-voltage square wave that is applied to a resonant tank circuit. This is commonly referred to as operation at “50% duty cycle”, although the real duty cycle, i.e. the ratio of the on-time of either switch to the switching period, is less than 50% because of the dead time between complementary gate drive pulses. Dead time is inserted between the turning off of one MOSFET and the turning on of the other MOSFET. During such dead time, both MOSFETs are off. Dead time is necessary for the correct operation of the resonant tank converter: it enables soft switching of the MOSFETs and, therefore, high-frequency operation with high efficiency and low EMI emissions. In brief, during dead time, the half-bridge node voltage moves between from the high level to ground and vice versa, pushed by the switched current (that is, the resonant tank current flowing at the time the MOSFET is turned off). It successively discharges and charges the equivalent capacitance of the half-ridge node. When the half-bridge node voltage has reached the ground or the high level, the corresponding MOSFET (low side or high side) can be turned on. The transition time of the half-bridge node depends on the switched current that, in turn, depends on the output load. A useful feature offered by STNRG599 is the adaptive dead time function: the controller can set a dead time value, within a certain range, according to the half-bridge node transition time. The benefits and operation of the adaptive dead time function are described in the dedicated section. In brief, it allows optimization of the resonant tank design so that soft switching can be achieved with a lower level of magnetizing current in the transformer; in this way, the converter efficiency can be optimized over a broad load range.

Normal operation of the resonant tank converter is such that the frequency (of the 50% duty cycle square wave feeding the resonant tank) increases when the load is reduced. This operating mode is called continuous switching. In general, at some light load, the switching losses become relevant and dominant, so it is no longer possible to regulate the output load in continuous switching operation while keeping good efficiency and being compliant with energy-saving regulations.

Output regulation at light load with limited switching frequency increase is allowed by burst mode operation: rather than continuously switching, the converter starts operating in a controlled intermittent way in which packets of a limited number of switching cycles are spaced by idle periods characterized by both MOSFETs in the off state. Details of the burst mode function of STNR599, in relationship with phase shift control methodology, are given in the dedicated section.

7.2 Phase shift control (PSC) methodology

The controlled variable in the phase shift control methodology is the phase between the half-bridge edge (rising or falling) and the zero crossing (ascending or descending) of the resonant tank current. The phase is defined as the ratio between the time from the half-bridge edge to the resonant current zero crossing and the time the half bridge stays high or low. In other words, the phase is the displacement angle between the input voltage and the input current of the resonant tank. Since the power transferred across the resonant tank in a switching cycle (disregarding the losses) is proportional to the input voltage by the input current and by the cosine of the displacement angle (i.e., the phase), controlling the latter make it possible to control the output power. The phase approaches zero at full load, while it approaches 0.5 at light load (0.5 corresponds to π / 2 rad, given that T_{SW} corresponds to 2·π rad).

Inside STNRG599, the phase shift, Φ_{SH}, is measured as the ratio between the time from one MOSFET turn-off to the corresponding zero crossing of the sensed resonant current, and the time from the MOSFET turn-off to the complementary MOSFET turn-off. Figure 5 shows the phase shift between the half-bridge voltage and the resonant tank current, while Figure 6 shows the way the phase shift is measured inside STNRG599. The control law resulting from the implementation of the phase shift control methodology is:

$$\Phi_{SH} = \frac{T_z}{T_{sw}/2} = 0.25 \cdot \frac{I_{FB}}{I_{OSC}} \quad (1)$$

where I_{FB} is the current sourced by pin FB and I_{OSC} is the current sourced by pin OSC. The former usually consists of the feedback current by the optocoupler, the soft-start current, and an offset current defining the minimum phase shift. The latter is simply given by 2 V / R_{OSC}, since pin OSC is a reference voltage source. The control law states that the phase shift is programmed by the current source by pin FB with respect to the current programmed by R_{OSC} at pin OSC.

Figure 5. Phase shift between the half-bridge voltage and the resonant tank current

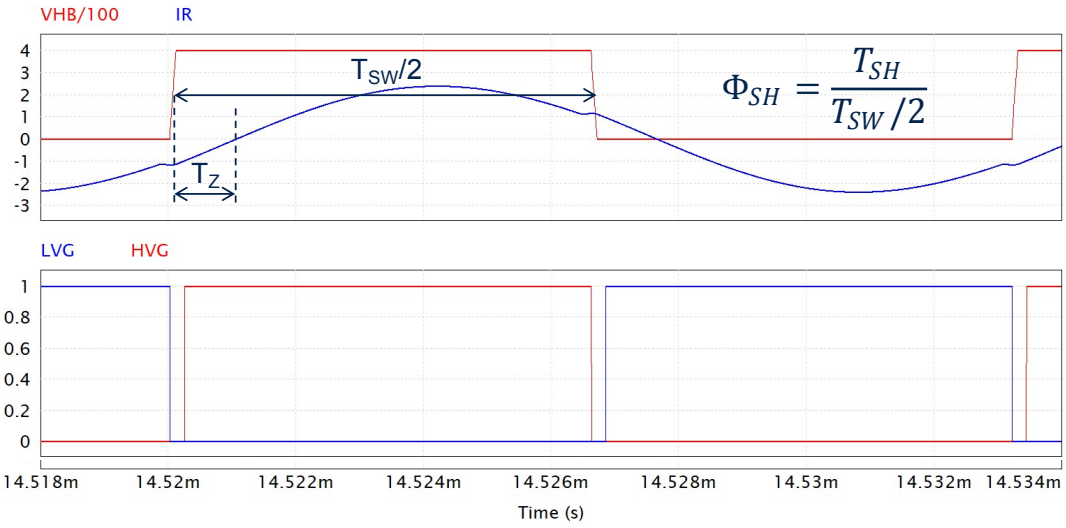
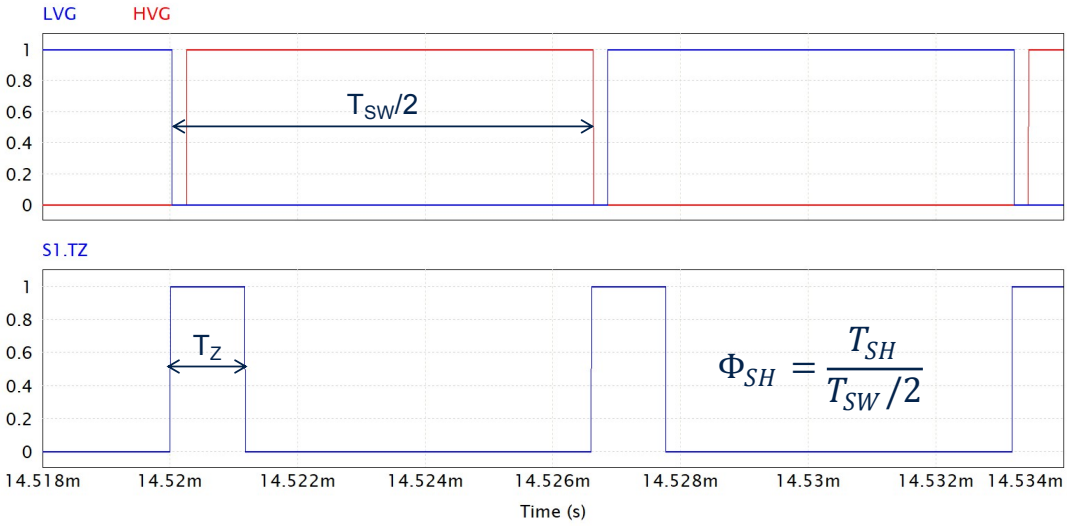


Figure 6. Phase shift internally measured by STNRG599



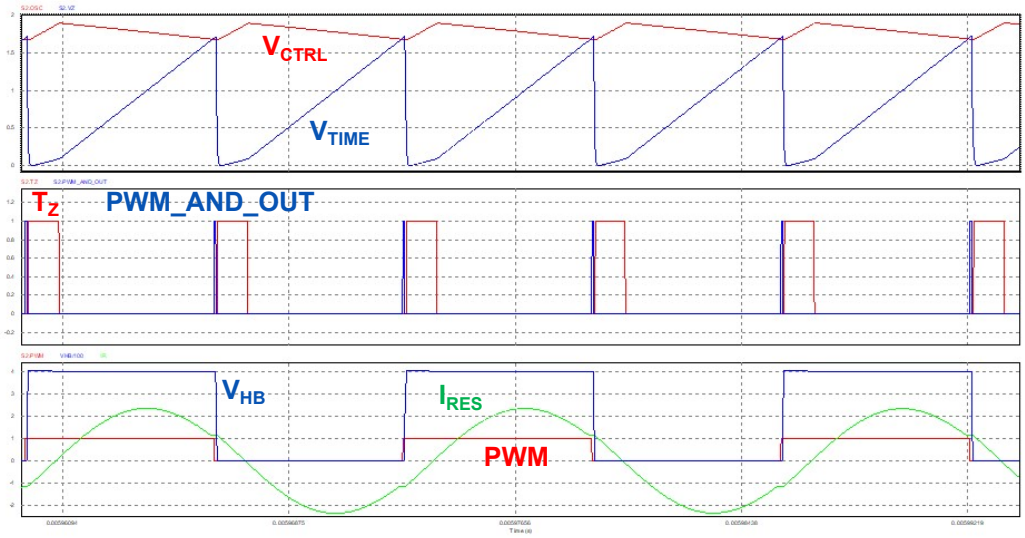
The purpose of Figure 7 and Figure 8 is to describe what happens inside STNRG599, despite the fact that relevant signals are internal and cannot be observed.

In both figures, the top quadrant shows the double-slope sawtooth internal signal, V_{TIME}, whose peak is the reference signal, and the offset triangular internal signal, V_{CTRL}, whose mean value represents the transferred power. In the second quadrant, the impulsive PWM signal, with pulses generated at each event "V_{CTRL} (descending) = V_{TIME} (ascending)", is shown together with the logical signal T_Z, which represents the phase of resonant tank input voltage and current. The bottom quadrant shows the latched PWM signal that ultimately generates the half-bridge square waveform (scaled version shown for convenience) and the corresponding resonant tank current.

From the comparison of Figure 7 and Figure 8, the following aspects can be highlighted:

- the level of the control signal V_{CTRL} is proportional to the output load
- the phase shift (width of logical signal T_Z) increases when load is reduced
- when load is reduced, the resulting switching frequency is increased (as expected).

Figure 7. Phase shift control - Typical signals at nominal input voltage, 400 V / 21 A (100%) (for a 77 kHz resonant tank designed for 250 W / 12 V)

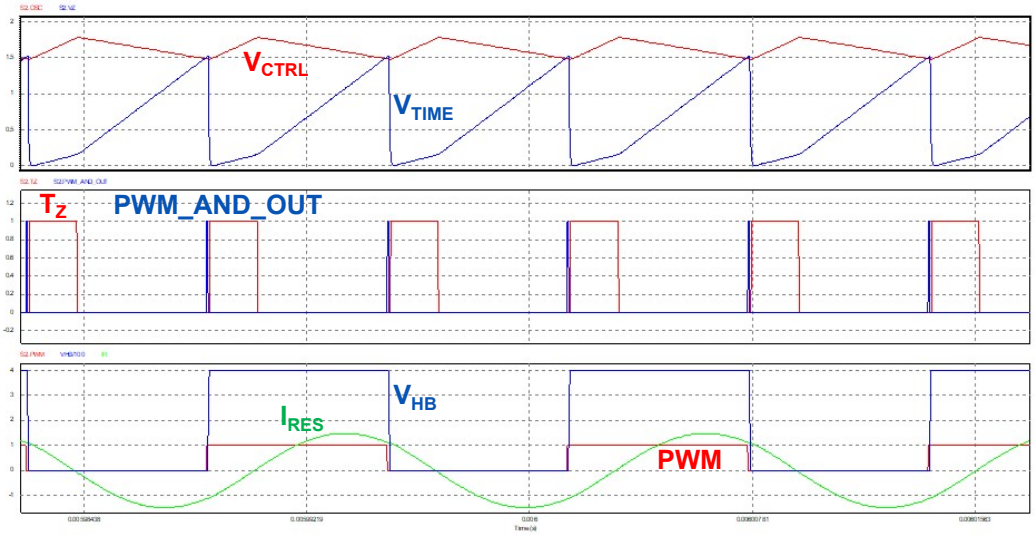


V_{CTRL}: control signal, V_{TIME}: reference signal

T_Z: phase signal, PWM_AND_OUT: PWM pulse train

PWM: driving signal, V_{HB}/100: scaled HB voltage, I_{RES}: resonant tank current

Figure 8. Phase shift control - Typical signals at nominal input voltage, 400 V / 10.5 A (50%) (for a 77 kHz resonant tank designed for 250 W / 12 V)



V_{CTRL}: control signal, V_{TIME}: reference signal

T_Z: phase signal, PWM_AND_OUT: PWM pulse train

PWM: driving signal, V_{HB}/100: scaled HB voltage, I_{RES}: resonant tank current

7.3 Burst mode operation

Burst mode operation is used to avoid the unbounded switching frequency increase that would otherwise be required to regulate the output at light load. At a certain point, continuous switching operation is stopped, and output load regulation is based on the balance between the idle periods and the switching packets.

The PSC methodology allows setting the entry level of burst mode operation in terms of the phase (between the input voltage and the input current of the resonant tank) at which burst mode operation must start. Since the phase is proportional to the transferred power, the burst mode entry level is directly linked to the output load.

The burst mode function is implemented in the following way. Pin STBY sources, onto an external resistor R_{STBY} connected between the pin and ground, a replica of the feedback current that the optocoupler sinks from pin FB. During continuous switching operation, the voltage at pin STBY is less than 2 V and increases when the output load is reduced, according to the feedback mechanism. For instance, in output voltage regulation, an output load reduction causes an output voltage to rise. This results in a lower error amplifier output voltage, i.e. a larger current pulled by the optocoupler. The larger current is sourced by pin STBY onto R_{STBY}, so that the pin voltage increases.

When the increasing voltage at pin STBY reaches 2 V, the burst mode comparator toggles and sets a flip-flop whose output is used to stop the switching activity. Consequently, the output voltage decreases, pushing down the voltage at pin STBY as well. When it reaches 1.9 V – 25 mV, the flip-flop is reset and the switching activity can restart. The flip-flop reset, and thus the restart of the switching activity, is driven by a second comparator, whose main function is to improve a limitation of the simple on / off burst mode method described above.

In fact, from the viewpoint of the phase shift between the half-bridge voltage and the resonant tank current (the control variable of STNRG599), burst mode operation starts when the phase shift has reached the value programmed by R_{STBY}. If the desired burst mode threshold corresponds to a very small fraction of the full load, then the phase shift would be close to 90°, corresponding to a very small energy amount transferred in the single switching cycle. The following mechanism is implemented to increase the energy involved in a switching cycle during burst mode operation and so to foster better efficiency of the system at light loads.

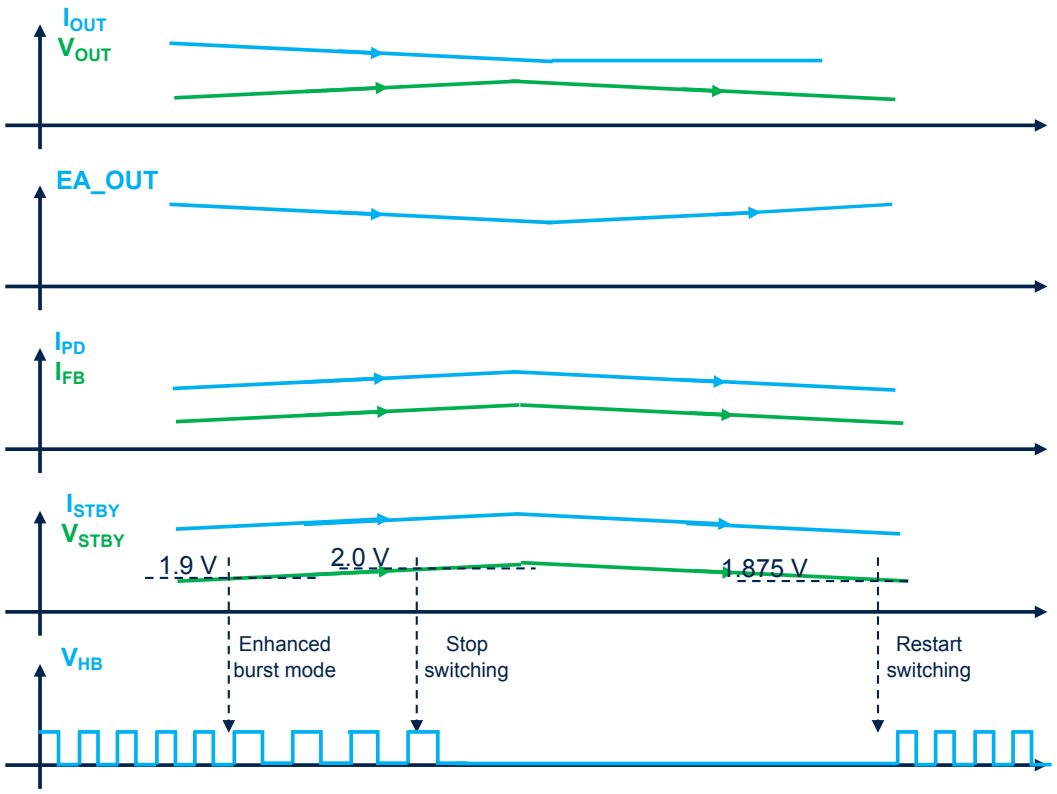
When the increasing voltage at pin STBY reaches 1.9 V, the enhanced burst mode comparator toggles and activates a 30% reduction on the feedback current, mirrored into STNRG599 through pin FB, which defines the phase shift. In this way, a phase shift reduction is forced in the final part of the switching activity before it is stopped by the burst mode comparator referenced at 2 V that also disables the 30% reduction on the feedback current.

The following Figure 9 qualitatively shows the main signals involved in burst mode operation. The output voltage increase, induced by the output current reduction, causes the reduction of the error amplifier output, EA_{OUT}, which in turn, corresponds to an increase of the photodiode current, I_{PD}, and the feedback current, I_{FB}. Note that the feedback current is smaller than the photodiode current because the CTR of the optocoupler is smaller than 1 at the typical forward current of the photodiode. The feedback current is mirrored and sourced at pin STBY, so I_{STBY} and V_{STBY} increase. At V_{STBY} = 1.9 V, the programmed phase shift is increased by 30%, corresponding to a switching frequency reduction. When V_{STBY} reaches 2.0 V, the switching activity is stopped as soon as the ongoing HVG pulse has elapsed. The effect of stopping the switching activity is that the output voltage starts decreasing and, correspondingly, the error amplifier output also decreases. Therefore, at pin STBY, the sourced current, and the pin voltage decrease. When V_{STBY} reached 1.875 V (= 1.9 V – 25 mV), the switching activity restarts.

Note that burst mode function is disabled as long as the voltage at pin CSS (soft-start pin) is less than 1 V. This means that if STBY > 2 V & CSS < 1 V, the switching activity is not stopped.

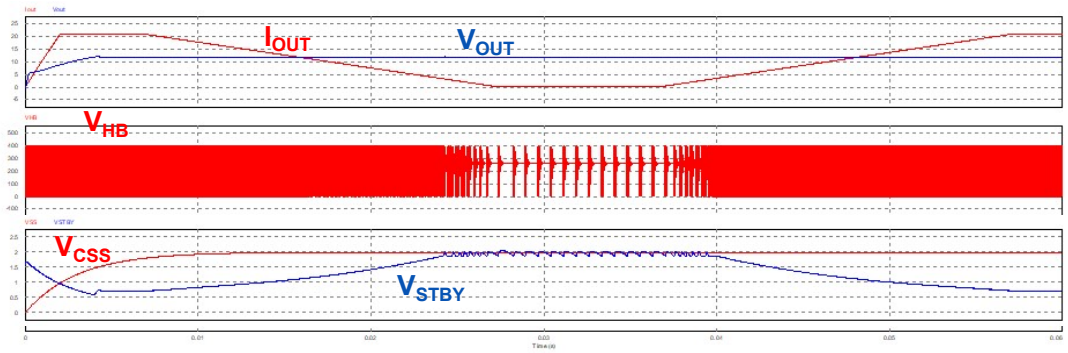
During burst mode operation, the stop and restart events are accurately controlled to minimize the effect on the DC voltage across the resonant capacitor: the last pulse before switching is stopped is a complete high-side pulse (HVG), while the first pulse at restart is a half low-side pulse (LVG). If the burst mode function is not used, pin STBY must be connected to ground.

Figure 9. **Main signals during burst mode operation**



An example of burst mode operation is shown in the following Figure 10 and Figure 11, illustrating the behavior of a PSC controlled converter when the load is changed from full load to nearly open load and then back to full load. The converter is designed at 77 kHz to deliver 250 W over 12 V at 400 V nominal input voltage; burst mode operation is set at about 10% of full load. The constant current output load, starting from full load (21 A), goes down to light load (0.5 A ≈ 2.5% of full load) in 20 ms, remains at light load for 10 ms, and eventually returns to the full load in 20 ms.

Figure 10. **Phase shift control – Burst mode operation / Long time base**

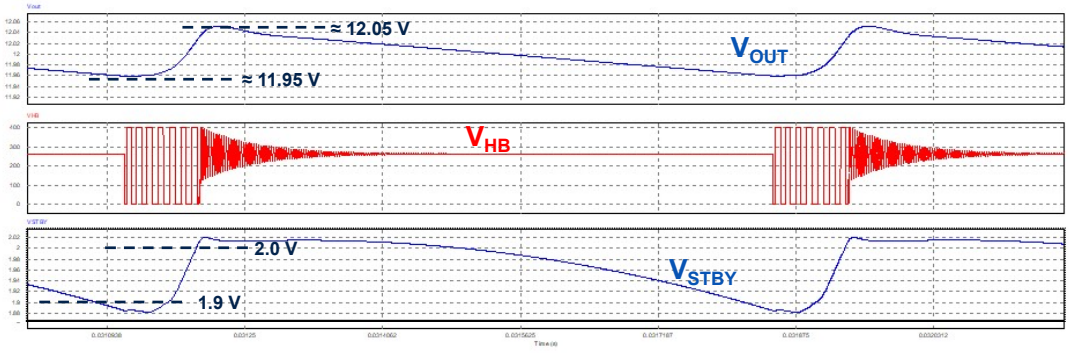


I_{OUT}: output current, V_{OUT}: output voltage

V_{HB}: half bridge voltage

V_{CSS}: soft start capacitor voltage, V_{STBY}: burst mode input signal

Figure 11. **Phase shift control – Burst mode operation / Short time base**



V_{OUT}: output voltage

V_{HB}: half bridge voltage

V_{STBY}: burst mode input signal

7.4 Current sensing and protection features

7.4.1 Current sensing

Pin ISEN is used for sensing the voltage corresponding to the instantaneous value of the resonant tank current, to perform the following tasks:

1. Implementation of phase shift control.
2. Overcurrent protection (OCP)
3. Capacitive mode detection (ACP) and hard-switch prevention (HSP)

It is important to highlight that pin ISEN must be externally AC coupled (i.e., a series capacitor is required) and that the electrical characteristics referring to pin ISEN are given at the series capacitor terminal opposite to pin ISEN. In other words, for instance, VISEN_OCP1/2 threshold values are those measured with the oscilloscope probe at the input side of the series capacitor, for which OCP1 and OCP2 events are observed. The oscilloscope probe must not be connected directly to pin ISEN, but rather to the input side of the series capacitor.

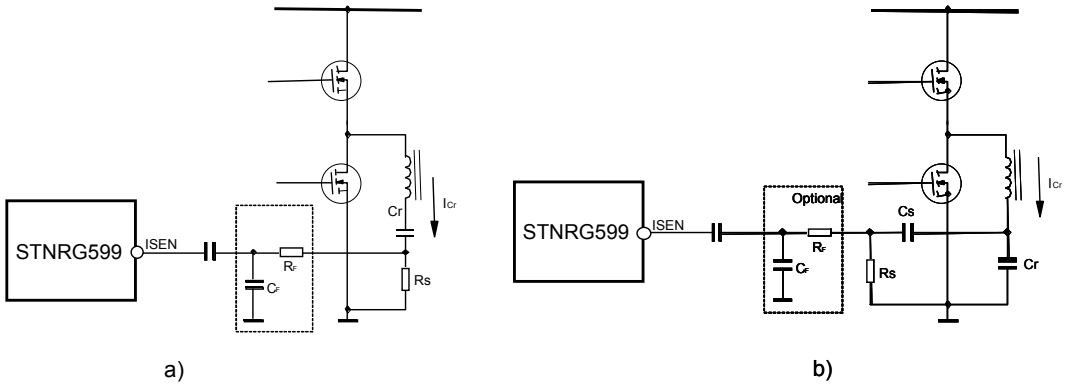
For the implementation of the phase shift control, pin ISEN feeds a precise zero crossing detector whose output is logically combined with the internal PWM driving signal to generate the logical signal TZ, whose width corresponds to the phase shift. See previous dedicated Section 7.2 for details.

In relationship to overcurrent protection, the signal at pin ISEN is compared with the OCP1 and OCP2 thresholds (0.87 V and 1.50 V, typ) to start the internal processes described inTable 2, in Section Section 7.4.2 and Section 7.4.3, and finally summarized in the table in Section 10.

The signal at pin ISEN is also used for capacitive mode detection and hard-switch prevention; these protection mechanisms are described in Section 7.5.

Figure 12 shows the typical ways the instantaneous resonant tank current can be sensed and converted into a voltage signal: lossy sensing by means of a series resistor, and lossless sensing by means of a capacitive shunt. In both cases, a smoothing RC filter is usually required to reduce the high-frequency noise at the sensing pin. Its time constant should not exceed 100/200 ns, to limit the impact on the overall control loop and on protection mechanisms, especially hard-switch prevention. The higher the switching frequency, the smaller the time constant must be. In general, a larger time constant increases the chance of hard switching when the converter operates near the capacitive region, because the delay introduced by the filter may approach the time lag between the half-bridge node voltage and the resonant current zero crossing.

Figure 12. Resonant tank current sensing. a) Lossy sensing with series resistor, b) Lossless with capacitive shunt



The value of the current sense resistor (R_S) depends on the current sensing circuit that is implemented, but the general rule is that the first-level overcurrent protection (OCP1) threshold must not be triggered during normal operation by the converter. This means that the signal at pin ISEN must remain below the minimum OCP1 threshold value of 0.82 V. In other words, the maximum peak of the resonant tank current, occuring at maximum output current and minimum input voltage, must not generate a voltage at pin ISEN that exceeds 0.82 V.

In the circuit shown in Figure 12a), the current sensing resistor R_S is in series with the resonant tank. Its value is determined by the equation:

$$Rs = \frac{0.82}{I_{Crpkx}} \tag{2}$$

where I_{Crpkx} is the maximum expected peak current flowing through the resonant capacitor and the primary winding of the transformer. The power dissipation in R_S can be approximately calculated with the following equation:

$$P_{Rs} \approx 0.4 \cdot I_{Crpkx} \tag{3}$$

In the circuit shown in Figure 12b), C_r and C_S form a capacitive current divider, where C_S is a small fraction of C_r. In this case, the corresponding current sense resistor R_S is given by:

$$Rs = \frac{0.82}{I_{Crpkx}} \cdot \left(1 + \frac{C_r}{Cs}\right) \tag{4}$$

In this way, the power dissipation associated with R_S is reduced by a factor of $(1+C_r/C_S)$.

7.4.2 Overcurrent protection, OCP1 and OCP2

In a resonant tank converter, the most efficient way to reduce an excessive current level is to increase the phase shift or the switching frequency, so that the transferred power is decreased.

To implement the overcurrent protection features, pin ISEN is internally connected to the positive input of two comparators, respectively referenced to V_{ISENx} (0.87 / 0.82 V, typ./min.) and to 1.5 V (typ). The former is for 1st level protection (OCP1) and sustains the delayed shutdown function, while the latter is for 2nd level protection (OCP2) and provides immediate turn-off. Note that pin ISEN can also withstand negative voltages, but OCP1 and OCP2 are triggered only on positive voltages.

OCP1 – If the voltage at pin ISEN exceeds 0.87 V (typ.), the OCP1 comparator is triggered and the internal switch at pin CSS is turned on for 5 us to discharge the soft-start capacitor C_{SS}. The effect is an instantaneous increase of the phase shift / switching frequency and the corresponding reduction of the transferred power. Under output short-circuit condition, this mechanism results in a resonant tank current whose peak periodically oscillates below the maximum value set by the sensing resistor, R_S. An OCP1 event also starts the delayed shutdown process (details are described in the dedicated section).

OCP2 – If the voltage at pin ISEN exceeds 1.5 V (typ.), the OCP2 comparator is triggered and the switching activity is stopped immediately (HVG pulse reset by OCP2). The soft-start capacitor C_{SS} is fully discharged by the activation of the internal switch connected to pin CSS, so that the full soft-start procedure can take place when the IC restarts. Furthermore, the internal current source at pin DELAY is turned on till V_{DELAY} = 1.75 V. Assuming that R_{DELAY} // C_{DELAY} are connected from pin DELAY to ground, the capacitor is then discharged by the resistor, and the IC restarts when V_{DELAY} = 0.24 V. Detail of the delayed shutdown process are given in the dedicated section.

OCP1 and OCP2 are disabled when CSS < 300 mV.

Refer to the description of pin ISEN for further details on OCP1 and OCP2.

7.4.3 Delayed shutdown and restart upon overload

The 1st level OCP is effective in limiting the energy flow from primary to secondary in case of output short-circuit or output overload. However, under such conditions, the secondary side current flowing in the windings and rectifiers might be so high as to endanger the safety of the converter if it is allowed to flow continuously. To prevent damage, it is customary to force the converter to work intermittently: in this way, the average output current is reduced to values such that the thermal stress on the transformer and rectifiers can be handled.

In STNRG599, the programmable and controlled intermittent operation of the converter under overload or short-circuit is supported by pin DELAY, at which the delayed shutdown and restart function is implemented.

The user can set the maximum time, T_{SH}, the converter is allowed to operate under overload or short-circuit. If the stress condition lasts less than T_{SH}, no action is taken, thereby providing the system with the desired immunity to short-lasting events. Otherwise, when T_{SH} is exceeded, an overload protection procedure is activated: the IC is turned off and, in case of continuous overload or short-circuit, the converter operates intermittently with a user-defined duty cycle. The delayed shutdown and restart upon overload function is described hereinafter.

A capacitor and a resistor must be connected in parallel from pin DELAY to ground. When an OCP1 event is triggered, that is V_{ISEN} > 0.87 V, not only is the soft-start capacitor C_{SS} discharged for 5 us, but the delay capacitor C_{DELAY} is charged by an internal 250 uA current source for 5 us. Because of the presence of the delay resistor R_{DELAY}, as soon as the current source is turned off, C_{DELAY} is slightly discharged and the voltage at pin DELAY, V_{DELAY}, decreases slightly. This discharge is negligible because the time constant of the delayed shutdown and restart mechanism must be relatively long.

During an overload or a short-circuit, OCP1 events are periodically triggered, causing $C_{SS}$to discharge and C_{DELAY} to charge. The average current charging C_{DELAY} depends on the soft-start network (R_{SS} and C_{SS}), the transfer function of the resonant tank, and the overload or short-circuit impedance. As already mentioned, the discharge through R_{DELAY} can be neglected. This operation goes on until V_{DELAY} reaches 1 V, unless the overload or short-circuit is removed.

T_{SH} is the time V_{DELAY} takes to reach 1 V. There is no simple relationship between T_{SH} and C_{DELAY}, because many factors affect the average charging current. It is more practical to experimentally determine the value of C_{DELAY} that provides the desired T_{SH}. As a rough indication, T_{SH} is on the order of 100 ms when C_{DELAY} = 1 uF and a dead short circuit is applied (dead short means that the load impedance is very small).

If V_{DELAY} does not reach 1 V (i.e., T_{SH} has not elapsed because the overload condition has been removed), then C_{DELAY}, no longer charged by the internal 250 uA current source, is discharged by R_{DELAY}. Note that if another overload condition occurs before the complete discharge of C_{DELAY}, the corresponding equivalent T_{SH} is smaller, since the charging process of C_{DELAY} starts from V_{DELAY} > 0 V.

If the overload condition is such that V_{DELAY} reaches 1 V, then two actions occur: 1) C_{SS} is fully discharged (by the internal switch) to maximize the operating phase, and therefore the switching frequency, and to ensure a complete soft-start at the next restart. 2) C_{DELAY} is continuously charged (by the internal current source) until V_{DELAY} reaches 1.75 V. The time from V_{DELAY} = 1 V to V_{DELAY} = 1.75 V is defined as T_{MP}, estimated by:

$$T_{MP} = \frac{1.75 - 1.0}{0.25} \cdot C_{DELAY} = 3 \cdot C_{DELAY} \quad (5)$$

where T_{MP} is in milliseconds and C_{DELAY} is in uF. During T_{MP}, the phase shift is close to the one programmed by the soft-start function. This means the switching frequency remains near the maximum allowed value, thereby minimizing the energy in the resonant tank.

When V_{DELAY} reaches 1.75 V, the switching activity is stopped (after the ongoing LVG / HVG cycle has elapsed), and the internal current source is turned off. At this point, C_{DELAY} is slowly discharged by R_{DELAY}. STNRG599 resumes operation when V_{DELAY} falls below 0.24 V. The time V_{DELAY} takes to decay from 1.75 V to 0.24 V is defined as T_{STOP}, estimated by the following formula:

$$T_{STOP} = R_{DELAY} \cdot C_{DELAY} \cdot ln\frac{1.75}{0.24} \approx 2 \cdot R_{DELAY} \cdot C_{DELAY} \quad (6)$$

where T_{STOP} is in milliseconds when R_{DELAY} and C_{DELAY} are expressed in kΩ and uF, respectively.

The operation of delayed shutdown and restart upon overload mechanism is shown in the timing diagram of Figure 13.

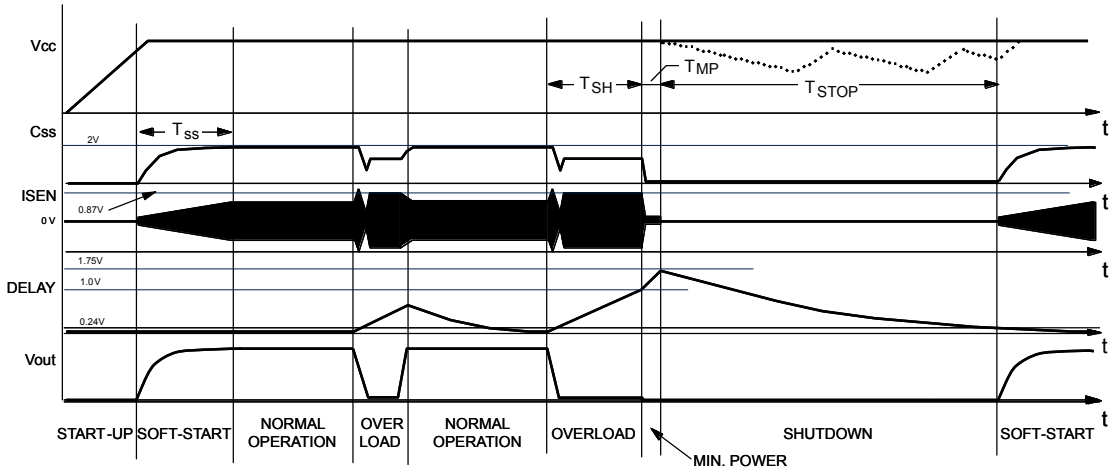
During normal operation, a first overload is applied but it lasts less than T_{SH}, i.e., V_{DELAY} does not reach 1 V. In this case, power transfer is limited because C_{SS} is discharged and the actual phase shift is more than the one the control loop would force; consequently, the output voltage is less than the regulated value. When the overload Is removed, C_{SS} restored to its steady-state value (2 V) and normal regulation takes place; at the same time, C_{DELAY}discharges through R_{DELAY}.

A second overload condition is then applied, this time lasting longer than T_{SH}. The power transfer is limited as in the first case, but now V_{DELAY} reaches 1 V. At this point, on one side, C_{SS} is fully discharged, further limiting power transfer and reducing the output voltage. On the other side, C_{DELAY} is charged by the internal current source until V_{DELAY} reaches 1.75 V. At this threshold, the switching activity is stopped (after the ongoing LVG / HVG cycle has elapsed), and the internal current source is turned off, allowing C_{DELAY} to discharge through R_{DELAY}.

When T_{STOP} has elapsed, that is V_{DELAY} has reached 0.24 V, the switching activity restarts following the full soft-start procedure. If the overload has been removed, the converter recovers to normal operation.

Note: if, during the T_{STOP}phase, VCC falls below VCCoff, the HVSU generator is activated. STNRG599 retains memory of the event and does not restart immediately after VCC has exceeded VCCon, if V_{DELAY} is still higher than 0.24 V.

Figure 13. Delayed shutdown and restart upon overload



The delayed shutdown and restart upon overload function can be disabled by connecting pin DELAY to ground. In this case, repeated OCP1 events do not result in a fault, since pin DELAY cannot reach 1 V and then 1.75 V.

Connecting pin DELAY to ground also affects OCP2 and OVP faults. When these faults are triggered, switching activity is stopped, but the restart procedure based on pin DELAY cannot take place.

7.5 Hard-switching prevention (HSP) and anti-capacitive protection (ACP)

A resonant tank converter works in capacitive mode, in which the voltage lags the current, when its switching frequency drops below a critical value that depends on the loading conditions and the input-to-output voltage ratio of the tank. Operation in capacitive mode is fostered by overload or short circuit, especially in case of low input voltage (voltage feeding the half-bridge leg less than the minimum specified for that resonant tank or marginal design of the latter).

It is possible to design a resonant tank converter that never works in capacitive mode, even under an abnormal operating condition. However, this requires design constraints that can be unacceptable in some cases (for instance, a transformer magnetizing current too large to have a converter compliant with light load or open load efficiency targets). The STNRG599 implements a hard-switching prevention (HSP) function and an anti-capacitive protection (ACP) function to avoid the severe drawbacks of operation in the capacitive region. At the same time, they still make it possible for the resonant tank converter design to guarantee operation in the inductive region (in the specified operating range, neglecting abnormal operating conditions). HSP function and ACP function are described hereinafter.

Hard-switching prevention, HSP.

After the conduction time, for correct turn-off, the resonant tank current must be positive when the half-bridge is HIGH (i.e., the HVG driver must be turned off) and negative when the half-bridge is LOW (i.e., the LVG driver must be turned off). To provide a certain margin on hard-switching (in other words, to prevent it) in relationship to the HSP function, the resonant tank current is defined as positive when V_{ISEN} > +40 mV and negative when V_{ISEN} < –40 mV. The hard-switching prevention method is the following:

- At the time the natural turn-off should take place, if the half-bridge is HIGH and V_{ISEN} < +40 mV, or the half-bridge is LOW and V_{ISEN} > –40 mV, then the active driver is not turned off, that is, the conduction time is made longer (and the half-bridge cannot toggle). A timer implementing 5 us timeout starts.
- While the conduction time is made longer, if the resonant tank current becomes the correct polarity with respect to the half-bridge state (V_{ISEN} > +40 mV when the half-bridge is HIGH, V_{ISEN} < – 40 mV when the half-bridge is LOW), then the active driver is turned off (and the timer is reset). Otherwise, if the 5 us timeout elapses, the active driver is turned off, without checking the polarity of the resonant tank current.

Anti-Capacitive Protection, ACP.

After the dead time, for correct turn-on, the resonant tank current must be negative when the half-bridge should go HIGH (that is when the HVG driver must be turned on) and positive when the half-bridge should go LOW (that is when the LVG driver must be turned on). To avoid capacitive mode, a certain margin must be considered, so, also for the ACP function, the resonant tank current is defined as positive when V_{ISEN} > +40 mV and negative when V_{ISEN} < –40 mV. The anti-capacitive protection method is the following:

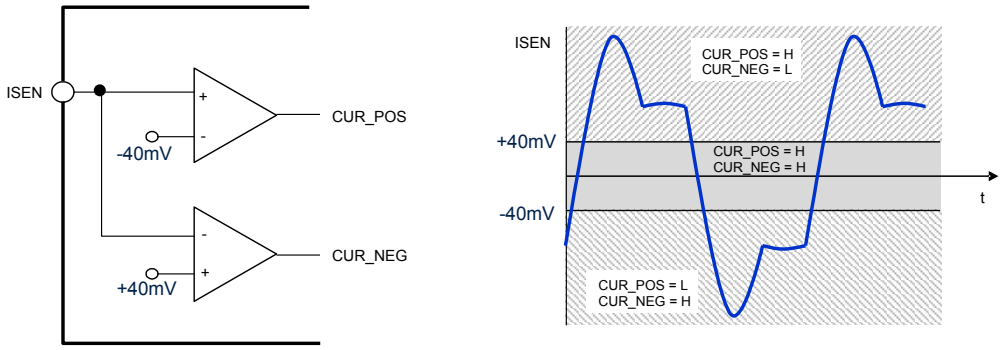
- At the end of the dead time, the driver is not turned on (i.e., the dead time is made longer) in case V_{ISEN} > –40 mV and the HVG driver must be turned on (i.e., the half-bridge must go HIGH) and in case V_{ISEN} < +40 mV and the LVG driver must be turned on (i.e., the half-bridge must go LOW). A timer implementing 20 us timeout starts.
- While the dead time is made longer, if the resonant tank current becomes the correct polarity with respect to the half-bridge transition that should take place (V_{ISEN} < –40 mV when the half-bridge should go HIGH and the HVG driver should be turned on, V_{ISEN} > +40 mV when the half-bridge should go LOW and the LVG driver should be turned on), then the driver is turned on (and the timer is reset). Otherwise, if the 20 us timeout elapses, the driver is turned on, without checking the polarity of the resonant tank current.

In case one of the two protection mechanisms takes place, at the end of the extended conduction time or dead time, the internal signals CTRL and TIME are set to 1 V and 0 V, respectively. The internal signals CTRL and TIME are both released at the first ZCD event.

To better understand HSP and ACP, it is worth remembering that a resonant tank converter must operate with the resonant tank current lagging behind the half-bridge voltage applied to the resonant tank; in other words, in normal operation, the resonant tank behaves like an inductive reactance. In this way, the voltage applied to the resonant tank and the resonant current have the same polarity when the half-bridge node toggles, which is a necessary condition for soft switching to occur. If the phase relationship should reverse, (i.e., the resonant tank current should lead the applied voltage like in a circuit having capacitive reactance), then hard switching would occur, with several adverse effects that may range from degradation of the electrical performance of the converter to catastrophic failure of the MOSFETs of the half-bridge leg.

HSP and ACP are based on a dedicated window comparator at the pin ISEN and on internal logic circuitry. The following Figure 14 helps the understanding of HSP and ACP mechanisms.

Figure 14. **Hard switch protection and anti capacitive protection**



7.6 Soft start function

In the STNRG599, the soft-start is sweeping the phase shift from a larger value to a smaller value until the control loop takes over, with the consequence that the operating frequency will sweep from an initially high value down to the point at which the control loop takes over. The soft-start procedure helps keep the initial resonant tank current at low levels, and avoid excessive inrush current to the output.

In the STNRG599, the soft-start function is implemented by connecting a series RC branch from the pin FB to the ground: the resistor to pin FB, the capacitor to the ground. Then, the node between the soft-start resistor (R_{SS}) and the soft-start capacitor (C_{SS}) is connected at pin CSS. See previous Figure 1 and/or Figure 4. At turn-on, the pin FB offers a 2 V reference level, so C_{SS}, which is initially discharged, is charged by R_{SS} to 2 V.

The soft-start current flowing during the charging process is mirrored inside the STNRG599, in the same way as for the feedback current pulled by the optocoupler and the offset current that defines the minimum phase shift. Hence, during the soft-start, this extra current flows across the pin FB and, according to the phase shift control law (eq. 1 in Section 7.2), it forces the converter to operate at higher phase shift than what that would be defined by the feedback. The extra current decreases while the soft-start capacitor is charged and vanishes when the pin CSS has reached 2 V. Consequently, the extra phase shift decreases and vanishes, as well.

Each time a fault occurs (DELAY from repeated OCP1 events, single OCP2 or OVP event, DCBO), the restart of the switching activity is conditioned by the discharge of the soft-start capacitor until at least 100 mV, so that the almost complete soft-start procedure can take place.

Note that the soft-start current could set a phase shift higher than the one programmed by R_{STBY} at pin STBY to enter burst-mode operation. To avoid burst-mode operation being activated during the soft-start, burst-mode is disabled till CSS < 1 V. Consequently, a certain relationship must be kept among R_{STBY} and R_{SS}, as explained in the Section 9.

7.7 Safe start procedure

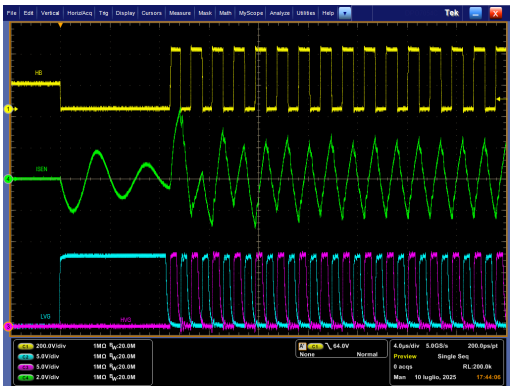
Despite the soft-start, it is possible to observe hard-switching events, during the very first cycles of the half-bridge node, in case no countermeasure is taken to avoid them.

For instance, it is customary to start the switching activity of the half-bridge by turning on the low-side MOSFET for a preset time, to pre-charge the bootstrap capacitor of the high-side driver, so that the high-side MOSFET can be properly driven from the very first cycle. The pre-charge time is typically constant, that is, it is written in the controller. An example is shown in the following Figure 15 in the left-hand picture. A constant pre-charge time obviously cannot guarantee that the resonant capacitor voltage is zero at the first turn-on of the high-side MOSFET. If the resonant capacitor voltage is not zero, then the very first turn-on of the high-side MOSFET could occur with non-zero drain-to-source voltage and positive resonant tank current, that is when the body diode of the low-side MOSFET is conducting. Inverse recovery of the low-side MOSFET body diode cannot be avoided, and further hard-switching events could occur. The number of hard-switching events is limited but potentially hazardous, as they could destroy both MOSFETs of the half-bridge leg, in case the resulting dv/dt across the low-side MOSFET exceeds its rating.

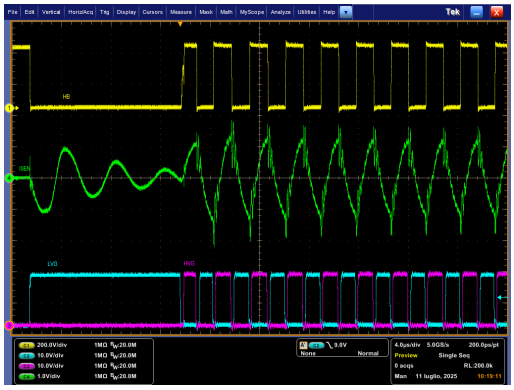
In STNRG599, the described behavior is prevented by HSP which extends the pre-charge pulse on the low side MOSFET until the resonant tank current is negative, as shown in the following Figure 15 in the right-hand picture. However, also in this case, when the MOSFET is turned on the very first time, its drain-to-source voltage is non-zero; therefore, in a stricter sense, a hard-switching event occurs.

However, in this case, the body diode of the other MOSFET is not reverse-recovered, and the hard-switching event is of negligible concern. In fact, the related capacitive power loss is thermally insignificant and, with a proper gate drive circuit, spurious turn-on of the other MOSFET through C_{GD} injection can be easily prevented.

Figure 15. Start-up behavior: L6599A on the left, STNRG599 on the right



LVG, HVG = 5 V/div



LVG, HVG = 10 V/div

The flux imbalance in the transformer in the first cycles is another possible cause of hard-switching events. To understand their origin, it is worth remembering that the half-bridge is driven at 50% duty cycle, so that under steady-state conditions the voltage across the resonant capacitor has a DC component equal to $V_{in}/2$. Consequently, the transformer's primary winding is symmetrically driven by a $\pm V_{in}/2$ square wave. However, at start-up, the voltage across the resonant capacitor is often different from $V_{in}/2$, so it takes some time for its DC component to reach that steady-state value. During this transient, in which operation is at 50% duty cycle, the transformer is not driven symmetrically, then there is a significant V · s imbalance in two consecutive half cycles. If this imbalance is large, then there is a significant difference in the up and down slopes of the tank current: so, the duration of the two half-cycles being the same, the current may not reverse in a switching half-cycle. Once again, one MOSFET can be turned on while the body diode of the other MOSFET is conducting and this may happen for a few cycles. However, also in this case, HSP prevents these events by extending the conduction time of the low side MOSFET till the tank current becomes negative.

Overall, the HSP function along with the usual soft-start function defines a new start-up procedure free of hard-switching cycles, which can be referred to as the safe-start procedure.

7.8 Adaptive dead time

For the correct operation of a resonant tank converter, a dead time, T_D, must be inserted after one switch is turned off, that is before the turn-on of the complementary one; during T_D, both switches are in the off state, hence the half-bridge (HB) node is a high-impedance node.

The dead time is essential to achieve soft-switching. Its value must be larger than the time T_T needed for the rail-to-rail swing of the HB node. T_T depends on the total parasitic capacitance of the HB node that must be completely charged or discharged, depending on the direction of the HB node, and on the value of the resonant tank current during the transition.

With good approximation, the resonant tank current during T_T can be considered constant and equal to the so called switched current (I_S), which is the value of the resonant tank current when the transition begins, i.e., when the switch is turned off. If C_{HB} denotes the total parasitic capacitance of the node HB (C_{HB} includes the C_{OSS} of the MOSFETs, the parasitic capacitance of the primary winding of the transformer and other stray capacitances), then the condition for soft-switching that should be met under all the operating conditions is:

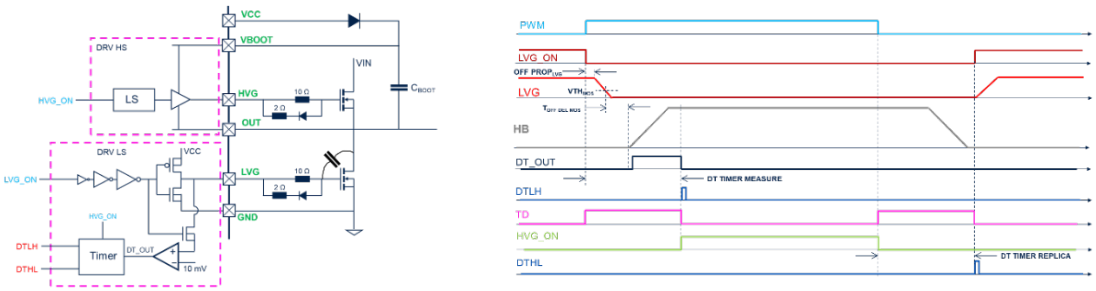
$$T_T = \frac{C_{HB}}{I_S} \cdot V_{in} \leq T_D \quad (7)$$

The previous formula suggests that T_D should be large enough to always exceed T_T, especially with maximum input voltage and minimum output load, that is the operating corner at which I_S is minimum and T_T is maximum.

However, a dead time that is too long may lead to losing soft-switching too: in fact, the resonant tank current must not change polarity within the dead time, which could lead to turning on the MOSFET with a non-zero drain-to-source voltage or, even worse, with the body diode (of the other MOSFET) in conduction. This event might occur at the maximum output load and minimum input voltage, especially when the tank circuit is designed for low magnetizing current to optimize the light load efficiency. Additionally, a dead time that is too long might increase the conduction losses in the body diodes and significantly limit the operating frequency of the resonant tank converter.

A good approach is to adjust T_D so that it tracks T_T, keeping T_D just longer than T_T under all operating conditions. This is the goal of the adaptive dead time (ADT) function implemented in the STNRG599. The block diagram and the key waveforms of the adaptive dead time generator are shown in the following Figure 16.

Figure 16. Adaptive dead time generator, block diagram and key waveforms



The HB node, i.e., the midpoint of the half-bridge leg, is connected to the pin OUT. The rising edge transition of the HB is sensed through the Cgd capacitance of the low-side MOSFET of the half -bridge (or through an external small capacitor). As far as the signal on the low-side MOSFET of the internal driver is above 10 mV, the comparator output, DT_OUT, is high and keeps running the internal timer that is started by the turn-off command of the low-side MOSFET of the half-bridge. When the half-bridge transition has elapsed, the comparator output goes low and the internal timer is reset: the half bridge high-side MOSFET is turned on and the measured dead time (from the half-bridge low-side MOSFET turn-off to the detected end of the rising edge of the half-bridge) is stored for the following falling edge transition of the half-bridge.

Overall, the ADT generator is active on the rising edge of the HB node: The dead time value found for this transition is then applied onto the following opposite transition, that is the falling edge of the HB node. The “copied” dead time is typically 30 ns longer than the measured dead time.

The ADT generator gives a minimum dead time of 300 ns (max.) and a maximum dead time of 700 ns (min.), depending on the slope of the HB. If, for some reason, the end of the HB transition was not detected, then the dead time would last indefinitely. To avoid this stall condition, a timeout of about 1.2 ms, on the dead time generation, is applied: unless ACP mechanism is active (dead time made longer to let the resonant tank current become the right polarity before turning on the MOSFET), the turn-on of one MOSFET is forced after about 1 ms from the time at which the other MOSFET has been turned off.

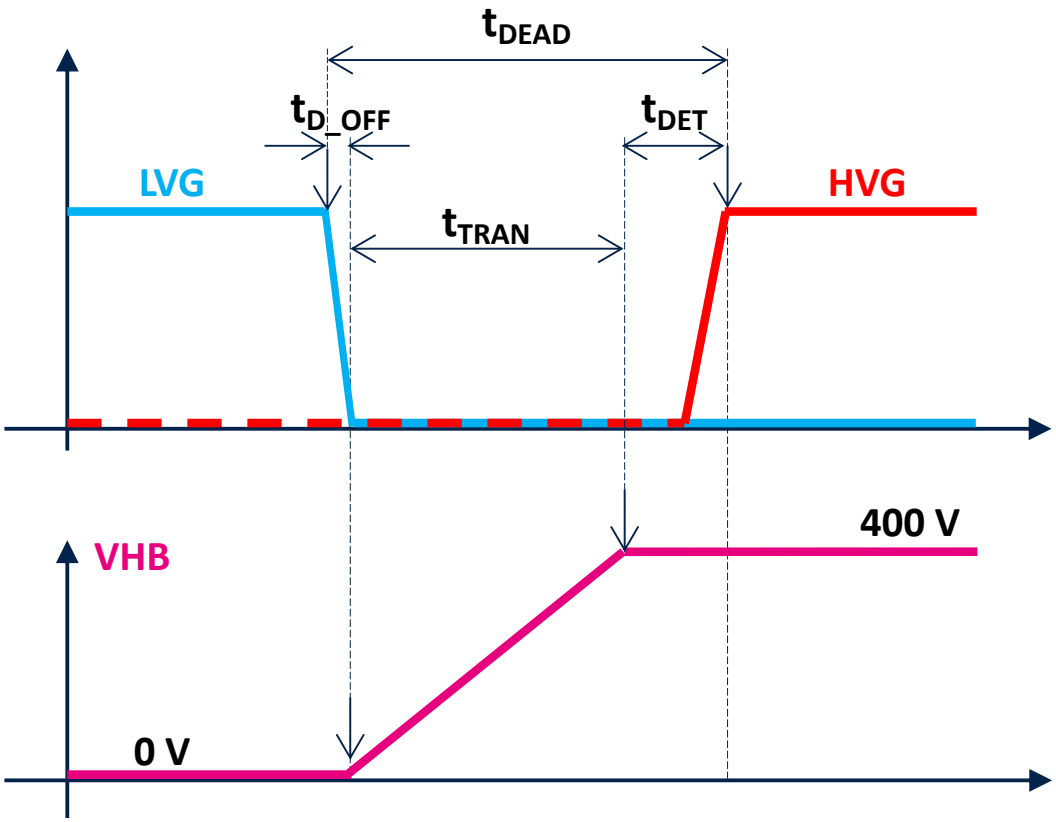
The observable dead time during the operation of the resonant converter can be better explained with the aid of the picture in the following Figure 17. Clearly, the comments that follow apply to the high-to-low transition as well.

There are three contributors to t_{DEAD}:

- The turn off delay of the MOSFET, t_{D_OFF}, that depends on the input characteristics of the specific MOSFET and the speed its gate is driven.
- The transition time, t_{TRAN}, taken by the node HB, to swing rail-to-rail, from 0V to 400 V when rising (and vice versa when falling).
- The detection time, t_{DET}, elapsing from the end of the node HB transition to the gate drive signal, of the other MOSFET, going high; t_{DET} includes the detection time itself as well as the propagation delay from the logic circuitry to the driver output.

It is important to highlight that the value of t_{DEAD_MIN} specified in the electrical characteristics is essentially t_{DET}: Therefore, in practice, the minimum observable t_{DEAD} will always be longer. t_{DEAD_MAX}, instead, is counted starting from the negative-going edge of the gate drive signal.

Figure 17. **Detailed dead time definition**



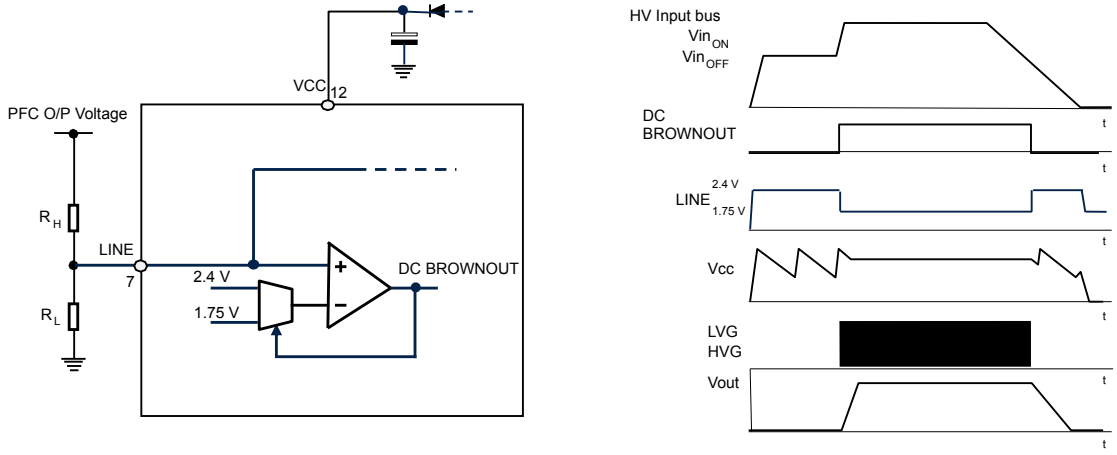
Finally, it is worth stating that the ADT function does not significantly increase efficiency by itself. It is a degree of freedom that can be exploited for this purpose when designing the resonant tank. Essentially, it allows for the use of a higher magnetizing inductance in the transformer, which minimizes the magnetizing current and thus the conduction losses associated with it. Additionally, this may reduce the switched current to the minimum required to achieve soft-switching, thus reducing the turn-off switching losses in the MOSFETs. Efficiency at medium and light load will maximally benefit from this optimization.

7.9 Line sensing (DC brown out/in), overvoltage protection (OVP) and feedback failure disconnection (FFD)

At pin LINE, three functionalities are implemented: the DC brown out/in, which is the typical one, the overvoltage protection, which is to stop switching when the pin is pulled to 3.1V ,typ, and the feedback failure disconnection, which is supported by the internal clamp at 3.2V, min.

The line sensing function implements the DC brown-out/in of the converter: STNRG599 operation is disabled when the input voltage of the half-bridge leg is below a certain value and enabled when it is above that value to which a hysteresis is added. The sensed voltage is usually the output voltage of the PFC stage performing the AC-DC conversion before the DC-DC conversion done by the resonant tank converter. The block diagram and the timing diagram of the line sensing function are shown in the following Figure 18.

Figure 18. **Line sensing function, block diagram and timing diagram**



The line sensing function is accomplished by a comparator whose positive input is the pin LINE, its negative input is referenced to two thresholds that are toggled to implement the DC brown-out/in hysteresis. STNRG599 operation is enabled when V_{LINE} > 2.4 V (typ) and disabled when V_{LINE} < 1.75 V (typ). When V_{LINE} goes below the disable threshold, the soft-start capacitor is completely discharged and the power consumption of the IC is reduced. Furthermore, if VCC goes below VCCoff, the HVSU generator is enabled to keep VCC charging and discharging between VCCon and VCCoff, until the converter is not enabled by V_{LINE} going above the enable threshold.

The desired DC brown-in and brown-out threshold can be set by properly choosing the resistors of the external divider that senses the input voltage of the converter. Hysteresis is not programmable, but constant.

The pin LINE is prone to pick up noise because it is a high-impedance input that is externally connected to the high-value resistances of the sensing divider (for instance, if the resistor R_H is 10 MΩ, then the resistor R_L is about 2 V / (400 V / 10 MΩ) = 50 kΩ and it is the equivalent external resistance). This sensitivity might alter the measured brown-out voltage during operation or cause unwanted disable of the IC during ESD/EFT test. Therefore, it is recommended to bypass the pin LINE to ground with a small time constant RC filter (R up to 100 Ω, C up to 10 nF), to prevent such malfunctioning.

At pin LINE, an OVP comparator (3.1 V, typ with 200 mV hysteresis) and an internal clamper (3.2 V, min) are available.

If the pin is pulled to 3.1 V, typ, the turn-off procedure based on pin DELAY is activated. The switching activity is immediately stopped, the soft-start capacitor(C_{SS}) is completely discharged and the internal 250 uA current source is kept on until V_{DELAY} = 1.75 V. As the voltage on the pin exceeds 1.75 V, the internal 250 uA current source is turned off. The voltage on the pin decays because of R_{DELAY} and, also in this case, the IC is restarted, following the complete soft-start process, when V_{DELAY} falls below 0.24 V.

In both cases (LINE < 1.75 V or LINE > 3.1 V), the switching activity is stopped once the running LVG / HVG cycle is completed (driving pulse is not reset by fault, but by the control loop signal after the fault is triggered).

In case the pin DELAY is connected to ground, the turn-off procedure based on it cannot take place. VCC = VCCoff is the only event that can enable the HVSU generator to bring VCC to VCCon, guaranteeing the necessary condition for the restart of the switching activity. If VCC cannot reach VCCoff, then the OVP fault would latch the converter. The only way to solve this condition would be sensing the fault release at application level to set a low / high transition to the pin LINE.

The internal clamper to 3.2 V, min, manages the feedback failure disconnection of the low-side resistor of the external divider on the input voltage, so avoiding the uncontrolled rise of the pin LINE because of the high-side resistor of the external divider.

7.10 High-voltage startup and x-capacitor discharge function

STNRG599 embeds a high-voltage startup (HVSU) generator which allows the turn-on of STNRG599 itself and of a PFC control IC. The pin HV must be connected to the AC side of the input rectifier bridge, via a pair of diodes with common cathode, to sense the AC input voltage.

If the pin HV voltage is higher than 30 V (typ), then the HVSU generator starts charging the external capacitor, C_{VCC}, connected between the pin VCC and the pin GND. The first charging period is done at low current (about 1.2 mA) to be safe in case the pin VCC is shorted to ground. Then, when VCC rises above about 1.2 V, the charging current is increased to about 9 mA and VCC is brought to VCCon (16.5 V, typ), at which the control IC operation can start; the HVSU generator is turned off after about 80 ms from VCCon to relax the hold-up requirement on C_{VCC}.

The switching activity will effectively start only in the case that no fault is detected at VCCon (2.4 V < V_{LINE} < 3.1 V or V_{DELAY} not falling from 1.75 V to 0.24 V). The STNRG599 will be sustained by the on-board supply based on the auxiliary winding of the resonant transformer.

Conversely, if a fault is detected (V_{LINE} < 1.75 V & > 3.1 V or V_{DELAY} falling from 1.75 V to 0.24 V), then the switching activity will not start and VCC will be discharged, down to VCCoff, by intrinsic consumption, and re-charged, up to VCCon, by the HVSU generator.

In general, at any fault in which the switching activity is stopped, the consumption of the STNRG599 is reduced and VCC is again discharged and re-charged between VCCoff and VCCon. This mechanism assumes that the power supply of the STNRG599 is fed by on-board circuitry sustained by an auxiliary winding of the resonant tank transformer. After a fault, the HVSU generator is activated once the fault condition is no longer valid and the necessary condition for switching is verified.

The HVSU generator is also activated by the X-capacitor discharge function which detects the disconnection of the mains voltage. In this case, to meet safety regulations, the X capacitors of the EMI filter must be discharged to a safe voltage. The X-capacitor discharge function allows for building of a converter meeting such safety requirements, avoiding the usage of the traditional discharge resistor between the phase and the neutral of the AC line, thus enabling low power consumption in open load, according to efficiency standards. X-capacitor discharge function is enabled in the STNRG599A and disabled in the STNRG599B.

8 Bootstrap section

The floating drive of the high-side MOSFET is referenced to the pin OUT, connected to the half-bridge node, and supplied through pin VBOOT by means of a bootstrap circuit. The STNR599 does not integrate a bootstrap diode, therefore, an external high-voltage fast recovery diode (D_{BOOT}) must be connected from pin VCC to pin VBOOT to charge the boot capacitor C_{BOOT}, which is connected between pin VBOOT and pin OUT. This capacitor performs a function similar to that of C_{VCC}, connected between pin VCC and pin GND.

At startup, or at the beginning of a switching packet during burst-mode operation, the low-side MOSFET is always turned on first to charge CBOOT, ensuring it is ready to supply the floating drive of the high-side MOSFET.

9 STNRG599 setup

The control variable in the STNRG599 is the phase shift between the half-bridge voltage and the resonant tank current. The steady state control law is given by the equation in Section 7.2, reported here for convenience

Eq.8

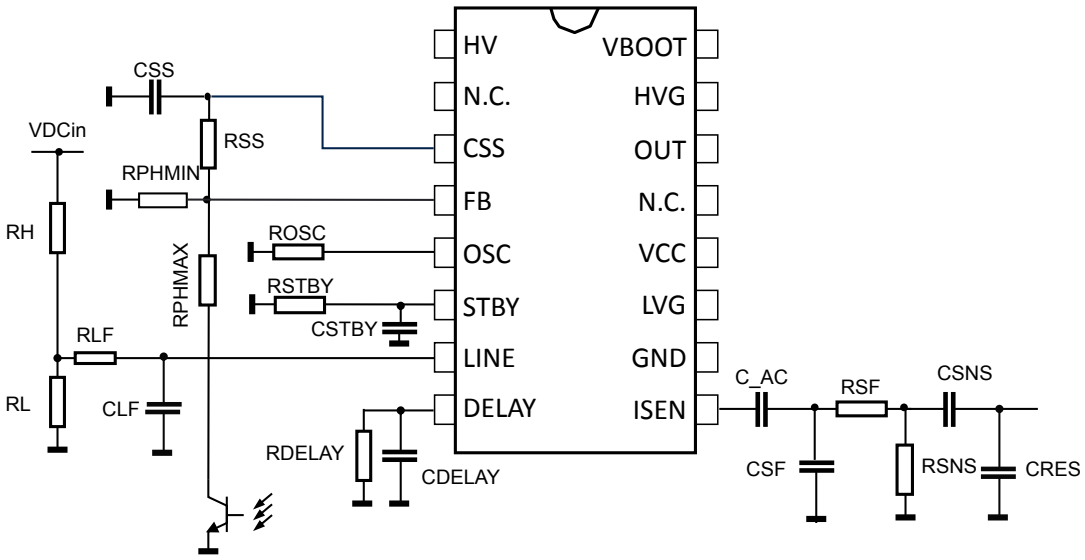
$$\Phi_{SH} = \frac{T_z}{T_{sw}/2} = 0.25 \cdot \frac{I_{FB}}{I_{OSC}} \quad (8)$$

where

- I_{FB} = feedback current = current sourced out from the pin FB
- I_{OSC} = 2V / R_{OSC} = current sourced out from the pin OSC
- Φ_{SH} = phase shift = T_Z / (T_{SW}/2)
  - T_Z = Time from HB edge to ISEN zero-crossing
  - T_{SW}/2 = Half the switching period

Figure 19 shows the basic schematic for the setup of the STNRG599.

Figure 19. STNRG599 setup, basic schematic



The setup of the STNRG599 can be done according to the following procedure. The first step is to calculate R_{OSC} (resistor from pin OSC to ground) that calibrates internal signals of the STNRG599 with respect to the operating frequency of the application. R_{OSC} can be found by the following Eq. (9), where f_{sw_min} is at minimum input voltage and maximum output current.

Eq. 9

$$R_{osc}[k\Omega] \sim \frac{4 \cdot 10^3}{f_{sw\,min}[kHz]} \quad (9)$$

Then, R_{PHMIN} and R_{PHMAX} (resistor from pin FB to ground and resistor between pin FB and the optocoupler, respectively) are found by the following equations 10 and 11. The former sets the minimum phase shift that can be programmed by the STNRG599, the latter limits the current sourced by the pin FB. Typical minimum phase shift is 0.05 – 0.15.

Eq.10

$$R_{PHMIN} \approx \frac{R_{OSC}}{4 \cdot \Phi_{SH\_min}} \quad (10)$$

Eq.11

$$R_{PHMAX} \approx \frac{2V}{500_{\mu A}} \approx 4 - 5\left[k\Omega\right] \quad (11)$$

The equation for the soft-start resistor is

Eq.12

$$R_{SS} = \frac{R_{OSC}}{4 \cdot \Phi_{SH\_SS}} \quad (12)$$

in which Φ_{SH_SS} is the phase shift programmed at time zero. To limit the resonant current peak in the switching cycles, Φ_{SH_SS} must be set close to 0.5 (or even more, considering internal delays). Therefore, R_{SS} is typically near $R_{OSC}/2$.

The soft-start capacitor is linked to the soft-start resistor by the time constant of the soft start procedure. This time constant, T_{SS}, is in the range from a few milliseconds to a few tens of milliseconds. The relationship between C_{SS} and R_{SS} is

Eq.13

$$C_{SS} = \frac{T_{SS}}{R_{SS}} \quad (13)$$

Burst-mode threshold is set by the resistor from the pin STBY to ground, which defines the phase shift at which burst-mode operation must start. Phase shift at burst-mode is defined by the following equation that links LLC tank parameters, the output voltage and the output current at which burst-mode operation must start.

Eq.14

$$\Phi_{SH\_BM} = \frac{1}{\pi} \cdot tan^{-1}\left(\frac{n_t^2 \cdot \sqrt{L_r \cdot C_r}}{L_m + L_r} \cdot \frac{V_{out}}{I_{out\_BM}}\right) \quad (14)$$

The result of the previous equation is used in the following equation to calculate R_{STBY} from R_{OSC}:

Eq.15

$$R_{STBY} \approx \frac{0.5}{0.15 + \Phi_{SH\_BM}} \cdot R_{osc} \quad (15)$$

These equations are rather precise when the operation is near resonance, but their results must be fine-tuned when operation is above resonance. Furthermore, a few hundred picoFarad capacitor in parallel with R_{STBY} is recommended to prevent noise pickup.

The delayed shutdown function, based on R_{DELAY} // C_{DELAY} at pin DELAY, can be designed according to the following equations in which the parameters are defined in Section 7.4.3.

Eq.16

$$C_{DELAY} = \frac{T_{MP}}{3} \quad (16)$$

Eq.17

$$R_{DELAY} = \frac{T_{STOP}}{2 \cdot C_{DELAY}} \quad (17)$$

DC brown-out/in thresholds are defined by the divider from the half-bridge input voltage to the pin LINE, according to the following equations:

Eq.18

$$R_H \approx 10 - 12\ [M\Omega] \quad (18)$$

Eq.19

$$R_L = \frac{2.4 \cdot R_H}{VDC_{Brown-in} - 2.4} \quad (19)$$

Since the hysteresis between the brown-in threshold and the brown-out threshold is constant, the above relationships also define the brown-out voltage:

Eq.20

$$VDC_{Brown-out} = \frac{1.75 \cdot [R_H + R_L]}{R_L} \cong 0.73 \cdot VDC_{Brown-in} \quad (20)$$

To prevent noise pick-up, an RC filter close to pin is recommended, with the resistor around 100 Ω and the capacitor between 1 nF and 10 nF.

Finally, a current sensing network can be designed according to the following equation, where I_{CRES_pk} is the maximum resonant current peak and C_{SNS} is typically 1/100 of C_{RES}.

Eq.21

$$R_{SNS} = \frac{0.82}{I_{CRES\_pk}} \cdot \left(1 + \frac{C_{RES}}{C_{SNS}}\right) \quad (21)$$

The AC coupling capacitor to the pin ISEN is typically 10 nF. An RC filter between the sensing resistor and the AC coupling capacitor is recommended to filter high-frequency noise. Its time constant should not exceed 200 ns, to avoid impacting the control loop and the protection mechanisms.

10 Summary of protection mechanisms and faults management

- A fault is an event whose direct effect is to stop switching.
- STNRG599 is characterized by the following faults:
  - VCC falling to VCCoff (9.5 V, typ)
  - LINE falling to DCBO threshold (1.75 V, typ)
  - DELAY rising to STOP threshold (1.75 V, typ)
  - Single OCP2 event (ISEN = 1.5 V → Stop switching and DELAY procedure activated)
  - Single OVP event (LINE = 3.1 V → Stop switching and DELAY procedure activated)
- DELAY fault is triggered by three mechanisms:
  - repeated OCP1 events (ISEN = 0.87 V)
  - single OCP2 event (ISEN = 1.5 V)
  - single OVP event (LINE = 3.1 V)
- XCAP is not a fault because it does not directly stop switching
- OCP1 is not a fault because it does not directly stop switching
- When DELAY is not used (DELAY = GND) and/or VCC cannot reach VCCoff (because of a fault), some mechanisms are different from typical ones (DELAY programmed).
- Stop switching vs LVG / HVG pulses – detail/remark:
  - Burst mode: LVG / HVG completed
  - All faults but OCP2: LVG / HVG completed
  - OCP2: not active on LVG, HVG interrupted

Protection	Fault	Condition	Action
XCAP	No	AC mains removal (no rectified voltage for more than 64 ms, typ)	• Cx discharged below 40 V within 1 s from AC mains removal. • No other action required.
OCP1	No	ISEN = 0.87 V (rising)	• C_{SS} discharged for 5 us by internal switch, 120 Ω, typ. • C_{DELAY} charged for 5 us by 250 uA current source. • Disabled for C_{SS} < 300 mV.
VCCoff	Yes	VCC = VCCoff (falling)	• Stop switching. • C_{SS} discharged (no restart allowed till V_{CSS} < 100 mV). • HVSU turned on till VCC = VCCon (rising). • HVSU kept on for 80 ms from VCC = VCCon.
DCBO	Yes	LINE < 1.75 V	• Stop switching (LVG / HVG running cycle completed) • C_{SS} discharged (no restart allowed till V_{CSS} < 100 mV). • Fault released when LINE > 2.4 V (& < 3.1 V). • At fault release (if no other faults & if V_{CSS} < 100 mV): HVSU turned on until VCC = VCCon (rising) and HVSU kept on for 80 ms from VCC = VCCon. • While VCC > VCCon, in case of no fault, restart switching. • Otherwise (any valid fault), no switching and HVSU off.

Protection	Fault	Condition	Action
DCBO	Yes	DELAY = GND	• Note: In case DELAY = GND and VCC were kept above VCCon, any fault but DCBO (i.e., OCP2 and OVP) would result in a system latch. Such a condition can be removed if an external circuitry is built to sense the fault condition and to drive LINE low/high when the fault condition is no longer valid. Low/High transition on pin LINE = pin LINE pulled down below 1.75 V and then pulled up above 2.4 V (and below 3.1 V).
DELAY by repeated OCP1	Yes	DELAY = 1 V (rising)	• C_{SS} discharged (no restart allowed till V_{CSS} < 100 mV). • Turn on internal 250 uA: C_{DELAY} from 1 V to 1.75 V (irreversible process).
		DELAY = 1.75 V (rising)	• Stop switching (LVG / HVG running cycle completed). • Turn off internal 250 uA: HVSU kept on for 80 ms from VCC = VCCon.
		DELAY = 0.24 V (falling)	• Fault released when DELAY < 0.24 V. • At fault release (if no other faults & if V_{CSS} < 100 mV): HVSU turned on until VCC = VCCon (rising) and HVSU kept on for 80 ms from VCC = VCCon.
		@ VCCon	• While VCC > VCCon, in case of no fault, restart switching. • Otherwise (any valid fault), no switching and HVSU off.
		DELAY = GND	• Note: DELAY can be connected to ground. In this case, the stop switching by DELAY, which is caused by repeated OCP1 events, cannot take place. No special care required.
DELAY by OCP2	Yes	ISEN = 1.5 V (rising)	• Stop switching at trigger (not active on LVG, HVG pulse interrupted. • C_{SS} discharged (no restart allowed till V_{CSS} < 100 mV). • Turn on internal 250 uA: C_{DELAY} to 1.75 V (irreversible process).
		DELAY = 1.75 V (rising)	• Turn off internal 250 uA: C_{DELAY} discharge into R_{DELAY} and reset of OCP2 fault.
		DELAY = 0.24 V (falling)	• Fault released when DELAY < 0.24 V & ISEN < 1.5 V. • At fault release (if no other faults & if V_{CSS} < 100 mV): HVSU turned on till VCC = VCCon (rising) and HVSU kept on for 80 ms from VCC = VCCon.
		@ VCCon	• While VCC > VCCon, in case of no fault, restart switching. • Otherwise (any valid fault), no switching and HVSU off.
		DELAY = GND	• Note: if DELAY = GND, then the procedure based on DELAY = 1.75 V cannot take place. The internal 250 uA is turned off by an alternative mechanism, that is when VCC = VCCon after the HVSU turns on. The OCP2 fault is reset by VCC = VCCon after HVSU generator restart at VCC = VCCoff.

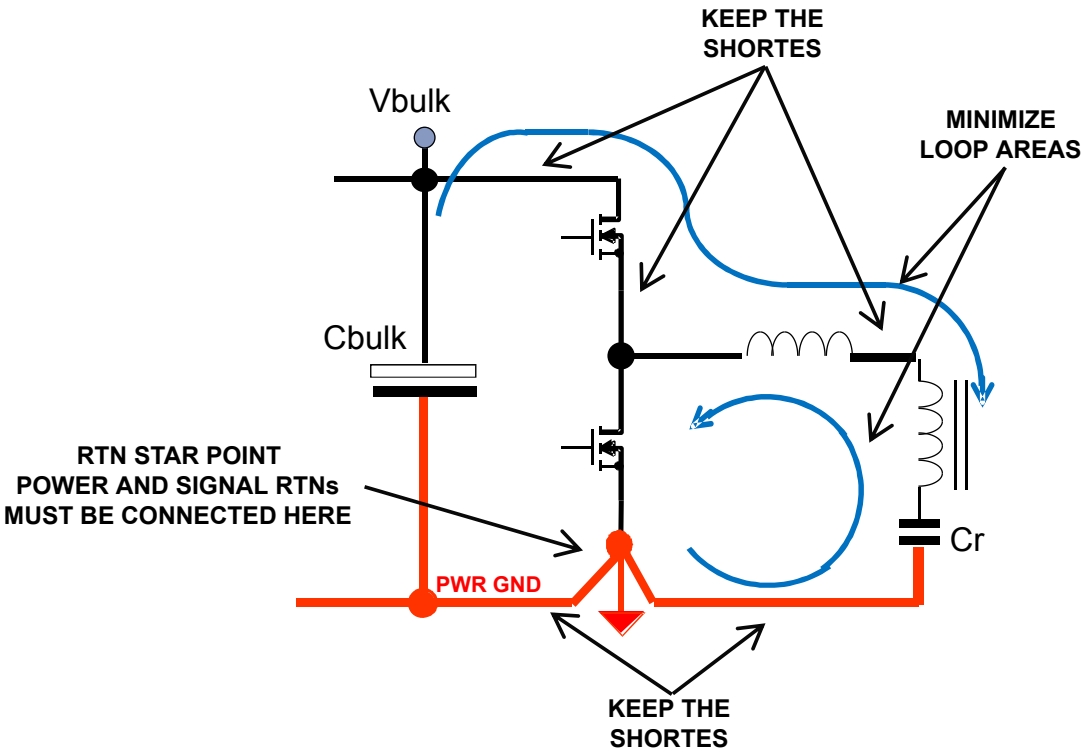
Protection	Fault	Condition	Action
DELAY by OCP2	Yes	DELAY = GND & VCC cannot reach VCCoff	• Note: in case DELAY = GND and VCC were kept above VCCon, any fault but DCBO (i.e., OCP2 and OVP) would result in a system latch. Such a condition can be removed if an external circuitry is built to sense the fault condition and to drive LINE low/high when the fault condition is no longer valid. Low/High transition on pin LINE = pin LINE pulled down below 1.75 V and then pulled up above 2.4 V (and below 3.1 V).
DELAY by OVP	Yes	LINE = 3.1 V (rising)	• Stop switching (LVG / HVG running cycle completed). • C_{SS} discharged (no restart allowed till V_{CSS} < 100 mV). • Turn on internal 250 uA: C_{DELAY} to 1.75 V (irreversible process).
		DELAY = 1.75 V (rising)	• Turn off internal 250 uA: C_{DELAY} discharge into R_{DELAY} and reset of OCP2 fault
		DELAY = 0.24 V (falling)	• Fault released when DELAY < 0.24 V & LINE < 2.9 V. • At fault release (if no other faults & if V_{CSS} < 100 mV): HVSU turned on until VCC = VCCon (rising) and HVSU kept on for 80 ms from VCC = VCCon.
		@ VCCon	• While VCC > VCCon, in case of no fault, restart switching. • Otherwise (any valid fault), no switching and HVSU off.
		DELAY = GND	• Note: if DELAY = GND, then the procedure based on DELAY = 1.75 V cannot take place. The internal 250 uA is turned off by an alternative mechanism, that is when VCC = VCCon after the HVSU turn on. The OCP2 fault is reset by VCC = VCCon after HVSU generator restart at VCC = VCCoff.
		DELAY = GND & VCC cannot reach VCCoff	• Note: in case DELAY = GND and VCC were kept above VCCon, any fault but DCBO (i.e., OCP2 and OVP) would result in a system latch. Such a condition can be removed if an external circuitry is built to sense the fault condition and to drive LINE low/high when the fault condition is no longer valid. Low/High transition on pin LINE = pin LINE pulled down below 1.75 V and then pulled up above 2.4 V (and below 3.1 V).
		$t_{OVP} > t_{DELAY}$	• Note: OVP condition longer than DELAY discharge (= when DELAY = 0.24 V, falling, the OVP condition is still valid). At DELAY = 0.24 V, the OVP condition set the internal 250 uA, bringing DELAY to 1.75 V and restarting a DELAY cycle.

11 Layout hints

The layout of any converter is a very important step in the design process. Although it may look time consuming, a good layout fosters easier and faster functional debug, as well as increased reliability and robustness of the application. Furthermore, the correct layout also allows for the design of smaller EMI filters. The STNRG599 does not have any special requirements in terms of layout, apart from applying general common sense rules, especially regarding ground connections and connections of high-voltage / current signals, which are schematically summarized in the following.

1. Keep power and signal RTNs separated. Connect the return pins of components carrying high current, such as the resonant capacitor and the source of the low-side switch, as close as possible. This point is the RTN star point. In case the front end is a PFC stage, the RTN star point must be connected to the negative terminal of the bulk capacitor at the PFC output. If there is no PFC stage, then the RTN star point must be connected to the negative terminal of the bulk capacitor after the rectifier bridge. When the LLC stage and the PFC stage are far away from each other, it is good practice to split the bulk capacitor, one close to the PFC output, the other close to the LLC input. In this way, differential mode noise from both stages is minimized. The heat sink of the half-bridge leg, if any, must be connected to the primary ground, near the source of the low-side switch.
2. Minimize the length of the tracks relevant to the half-bridge leg and the transformer, and minimize the loop areas as shown in the following Figure 20. The width of the tracks must be rather wide to minimize their parasitic inductance.

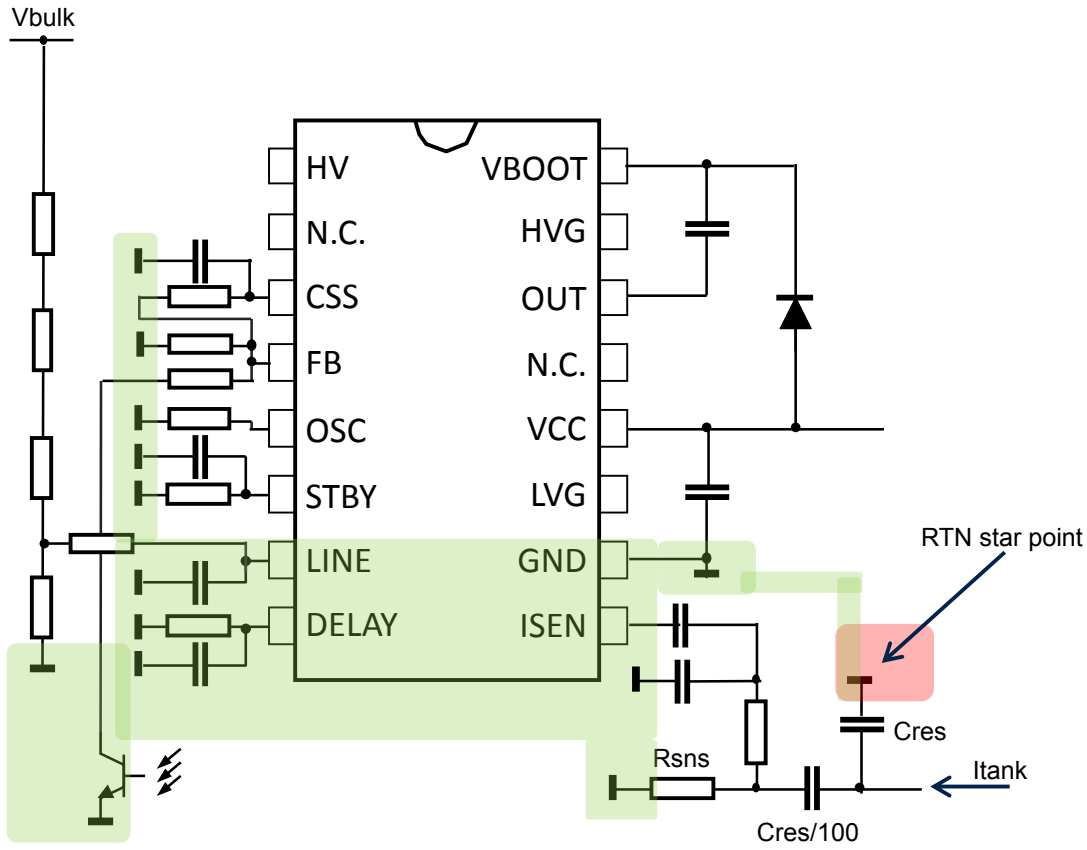
Figure 20. LLC stage power connections



3. Place signal components and relevant RC filters as close as possible to the corresponding pins of the STNRG599. Take special care for pin ISEN. Obviously, components and tracks related to pins from #3 to #9 must be kept away from tracks carrying power signals, especially the switching ones like the half-bridge node.
4. The power supply capacitor and the bootstrap capacitor must be of the ceramic type, placed close to corresponding pins, which are VCC / GND and VBOOT / OUT respectively. A proper bootstrap diode must be connected from pin VCC to pin VBOOT, again as close as possible to the pins themselves. See the following Figure 21 for reference.

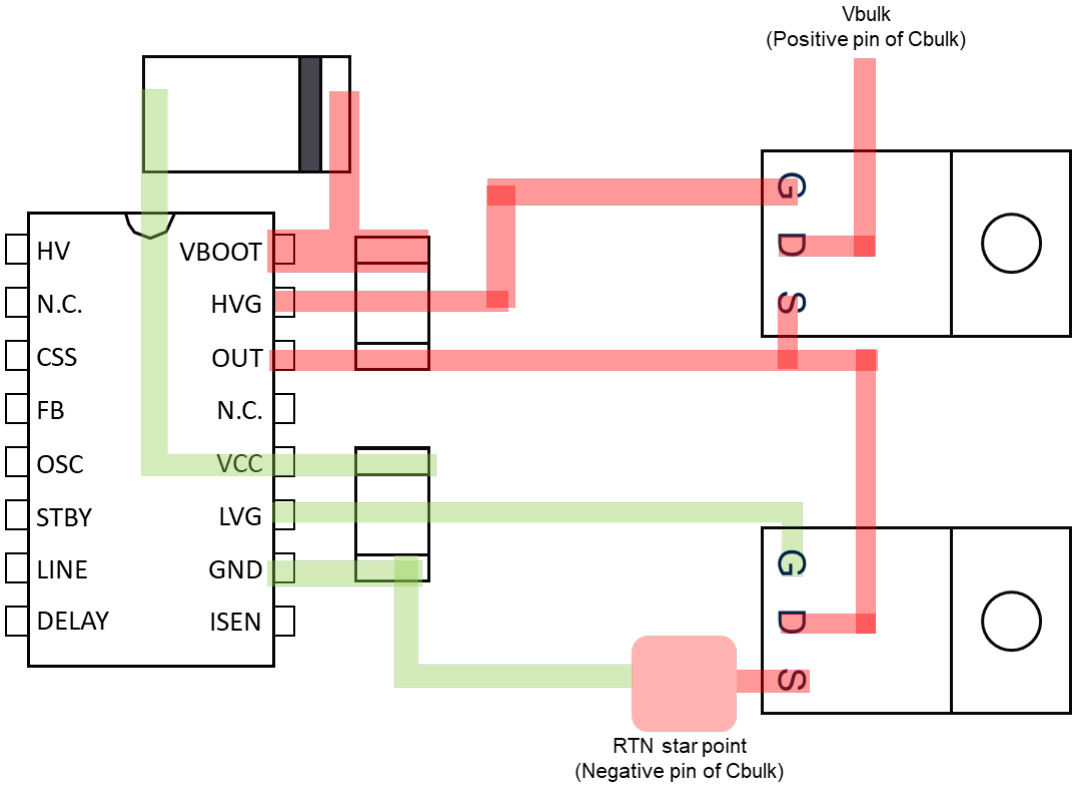
5. Do not place tracks relevant to pins VBOOT, HVG and OUT near signal tracks, especially the one carrying the feedback current, which is the track from the optocoupler collector to the pin FB. Pay attention to the minimum isolation distances of these tracks with respect to low-voltage ones.
6. Connect the ground terminals of the signal components and then to the pin GND (pin #10) of the STNRG599. Then, connect the latter pin to the RTN star point. These tracks must be kept the shortest and separated from any other ground connection, especially those carrying high current.
7. Connect the optocoupler emitter to the signal RTN, represented by the connection of the ground terminals of the signal components and the pin GND (pin #10) of STNRG599. Tracks from both the collector and the emitter of the optocoupler must be routed away from power tracks.

Figure 21. LLC stage signal connections



8. The routing of tracks from the STNRG599 to the half-bridge leg must avoid high dV/dt signal of high-voltage pins below the IC, because signal pins can suffer from this. Furthermore, it is preferable to place the IC and the power switches in a way that the layout is symmetrical and the length of the tracks as well as the loop areas of the gate driving pins are minimized. See Figure 22.

Figure 22. LLC stage half bridge connections



12 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 Package information

Table 6. SO16L (Narrow) package mechanical data

Ref	Dimensions [mm]						Notes
	Databook [mm]			Drawing [mm]			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
A	0.90		1.75	1.43	1.55	1.68	
A1	0.10		0.25	0.12	0.15	0.18	
A2	1.25			1.48	1.52	1.56	
b	0.31		0.51	0.375	0.40	0.425	
c	0.17		0.25			0.238	
D	9.80	9.90	10.00	9.82	9.85	9.88	
E	5.80	6.00	6.20	5.90	6.00	6.10	
E1	3.80	3.90	4.00	3.87	3.90	3.93	
e		1.27			1.27		
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	0.585	0.635	0.685	
k	0		8	2	4	8	Degrees
ccc			0.10			0.04	

Figure 23. **SO16L (Narrow) package outline**

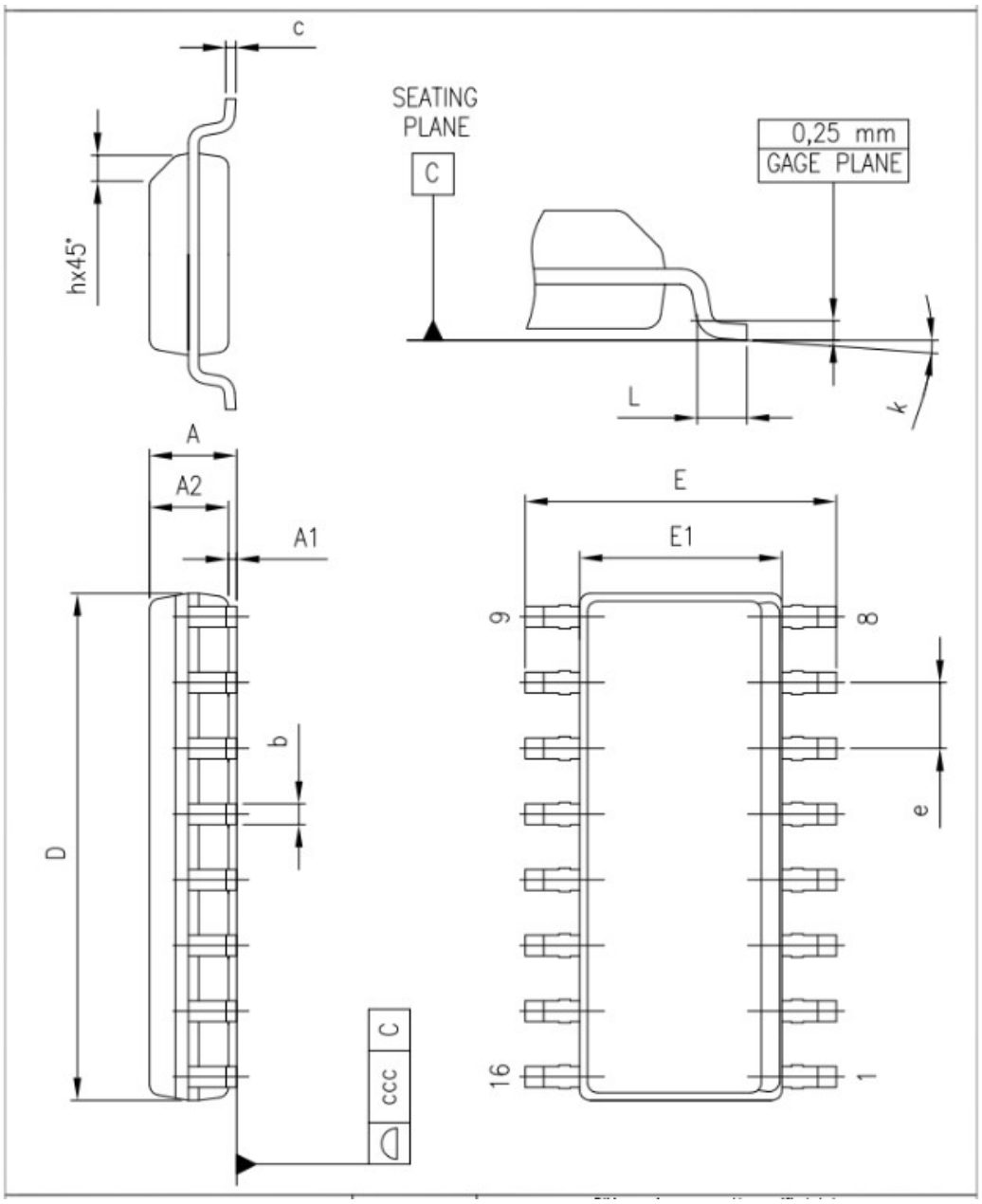
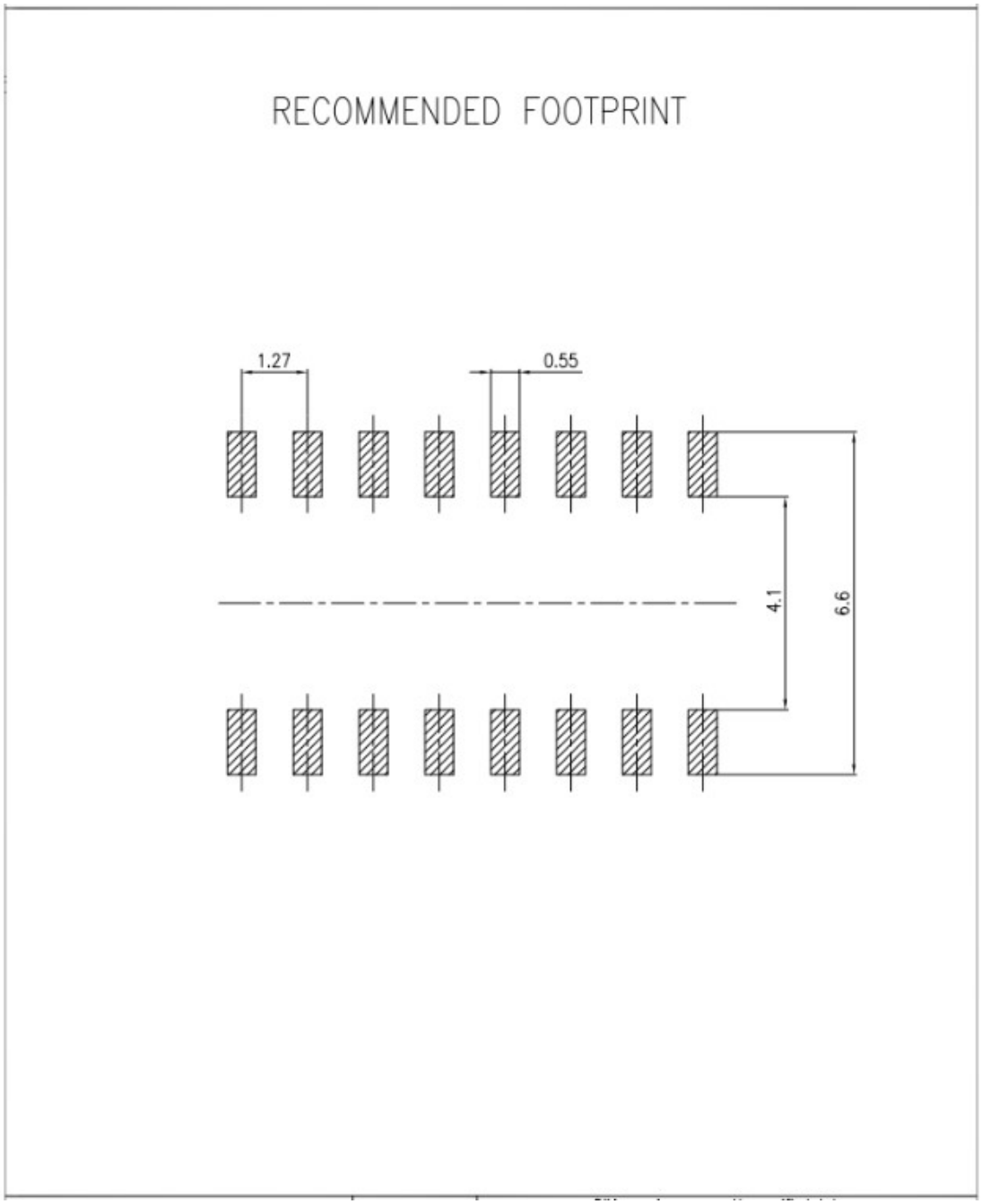


Figure 24. **SO16L (Narrow) recommended footprint (dimensions are in mm)**



Revision history

Table 7. **Document revision history**

Date	Version	Changes
17-Oct-2025	1	Initial release.
29-Oct-2025	2	Watermark removal.
07-Nov-2025	3	Added sustainability label

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