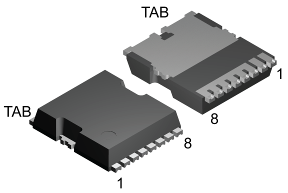
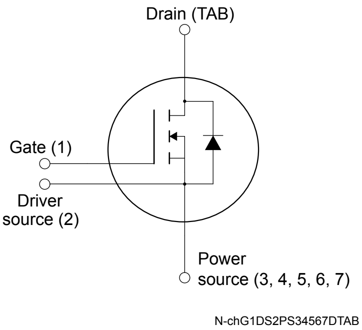
STO60N038M9

Datasheet

N-channel 600 V, 33 mΩ typ., 62 A, MDmesh M9 Power MOSFET in a TO-LL package



TO-LL type A2



Product status link
STO60N038M9

Product summary	
Order code	STO60N038M9
Marking	60N038M9
Package	TO-LL type A2
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO60N038M9	600 V	38 mΩ	62 A

- Very low FOM ($R_{DS(on)} \cdot Q_g$)
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested
- Excellent switching performance thanks to the extra driving source pin

Application

- AC-DC converters
- DC-DC converters
- Microinverter

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	62	A
	Drain current (continuous) at T_C = 100 °C	39	
I_{DM} (2)	Drain current (pulsed)	250	A
P_{TOT}	Total power dissipation at T_C = 25 °C	312	W
dv/dt (3)	Peak diode recovery voltage slope	50	V/ns
di/dt (3)	Peak diode recovery current slope	900	A/µs
dv/dt (4)	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-247 long leads package.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 31 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.4	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient (1)	43	°C/W
	Thermal resistance, junction-to-ambient (2)	22	

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*
2. *When mounted on 40x40 mm area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	7	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	786	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			200	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 31 A		33	38	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 250 kHz, V_{GS} = 0 V	-	4830	-	pF
C_{oss}	Output capacitance		-	90.5	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	1300	-	pF
R_g	Intrinsic gate resistance	f = 250 kHz, open drain	-	0.8	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 31 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	112	-	nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge		-	43	-	nC

1. *$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 31 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	28	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	77	-	ns
t_f	Fall time		-	4	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} [(1)]	Source-drain current		-		62	A
I_{SDM}[(2)]	Source-drain current (pulsed)		-		250	A
V_{SD}[(3)]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 62 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 62 A, di/dt = 100 A/μs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	277		ns
Q_{rr}	Reverse recovery charge		-	3.1		μC
I_{RRM}	Reverse recovery current		-	20		A
t_{rr}	Reverse recovery time	I_{SD} = 62 A, di/dt = 100 A/μs, V_{DD} = 60 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	445		ns
Q_{rr}	Reverse recovery charge		-	7		μC
I_{RRM}	Reverse recovery current		-	29		A

1. *Referred to TO-247 long leads package.*
2. *Pulse width is limited by safe operating area.*
3. *Pulsed: pulse duration = 300 μs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

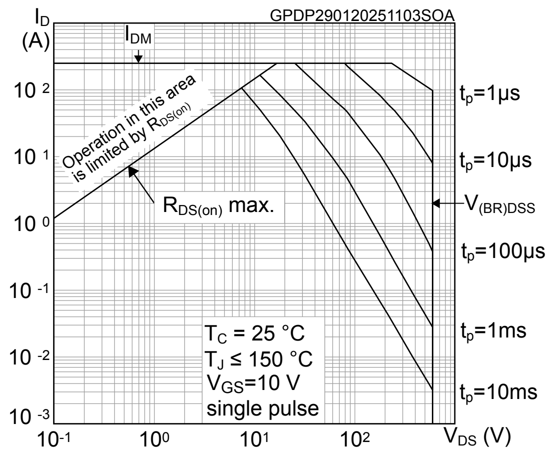


Figure 2. Maximum transient thermal impedance

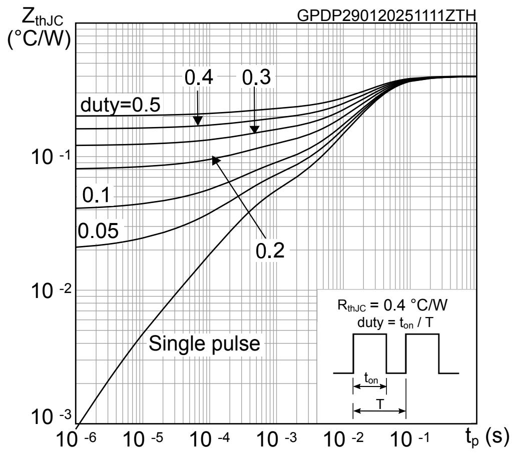


Figure 3. Typical output characteristics

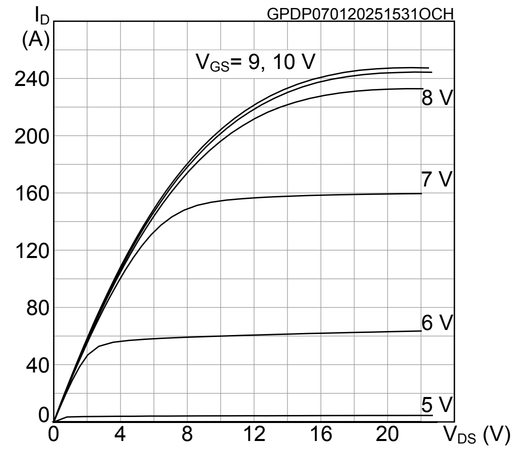


Figure 4. Typical transfer characteristics

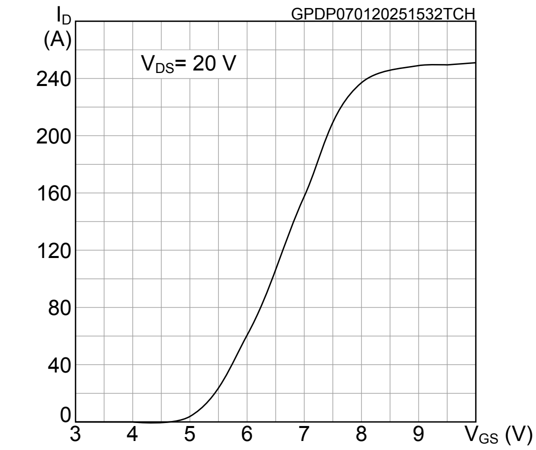


Figure 5. Typical gate charge characteristics

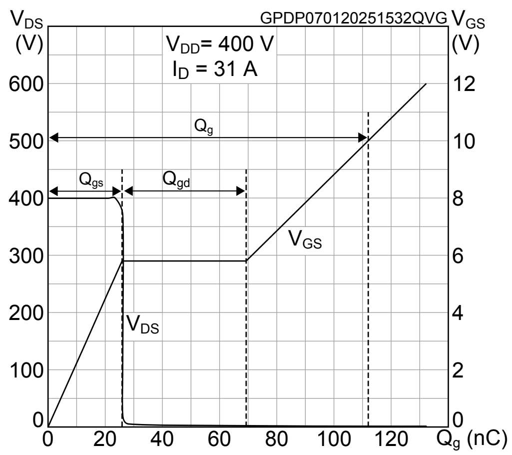


Figure 6. Typical drain-source on-resistance

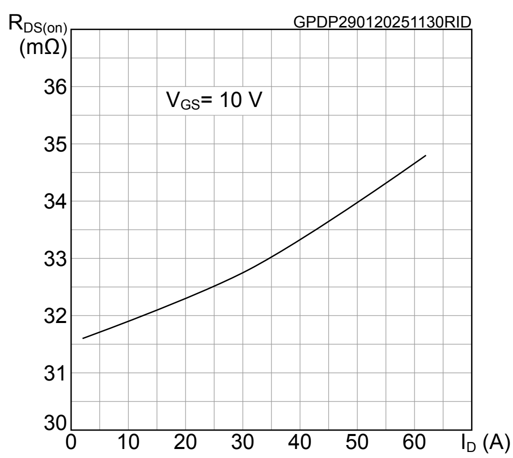


Figure 7. Typical capacitance characteristics

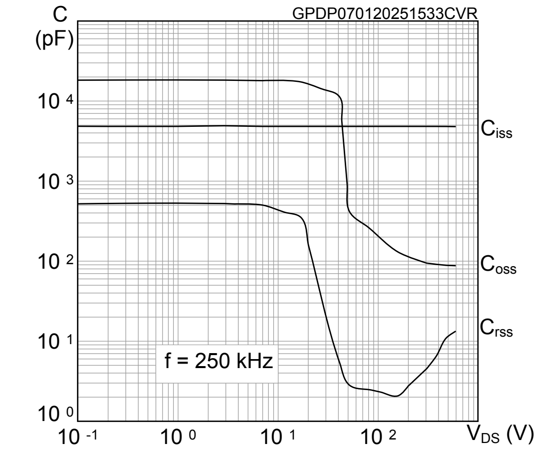


Figure 8. Typical output capacitance stored energy

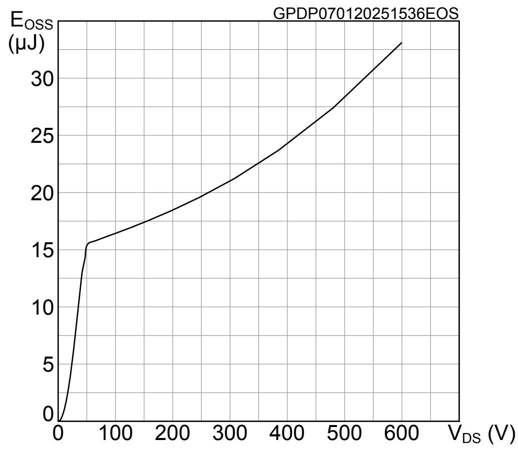


Figure 9. Normalized gate threshold vs temperature

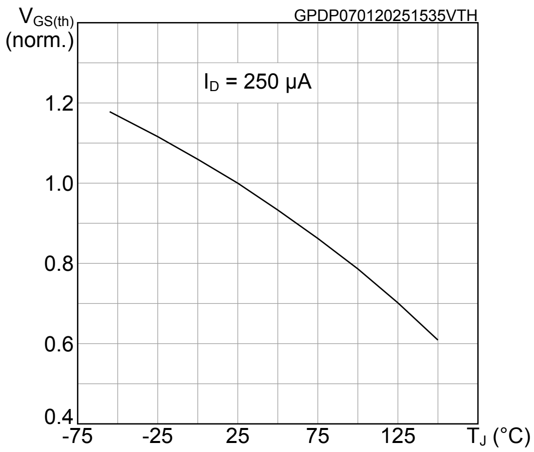


Figure 10. Normalized on-resistance vs temperature

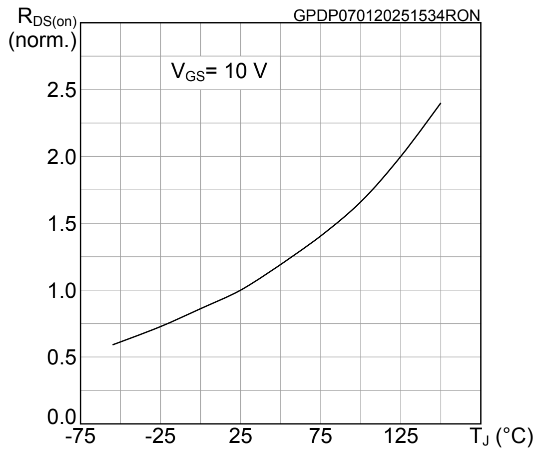


Figure 11. Normalized breakdown voltage vs temperature

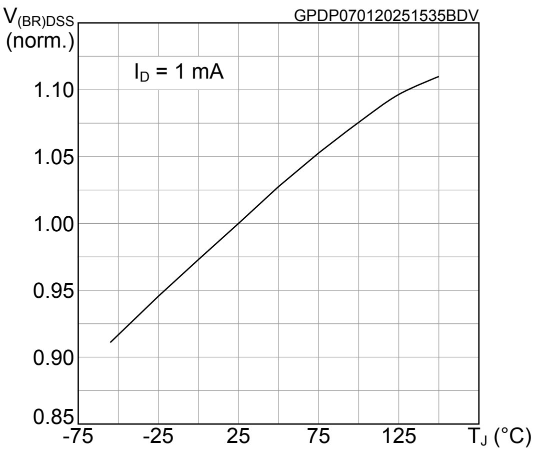
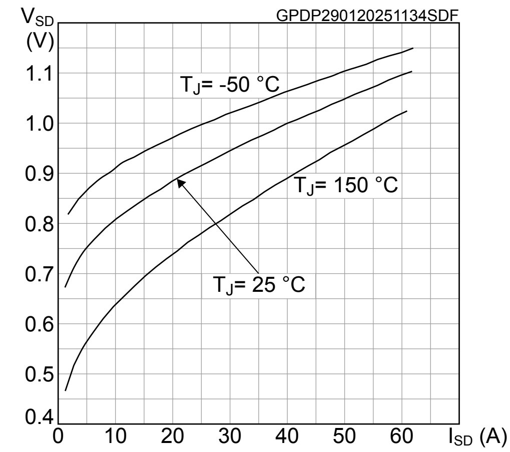


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. **Switching times test circuit for resistive load**

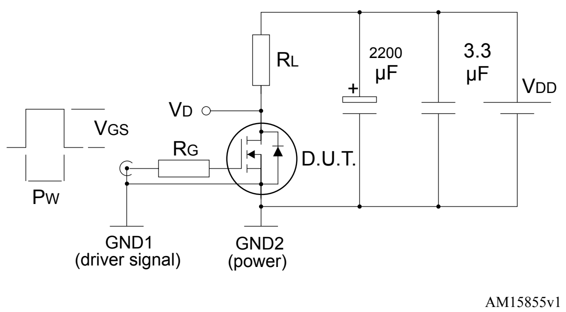


Figure 14. **Test circuit for gate charge behavior**

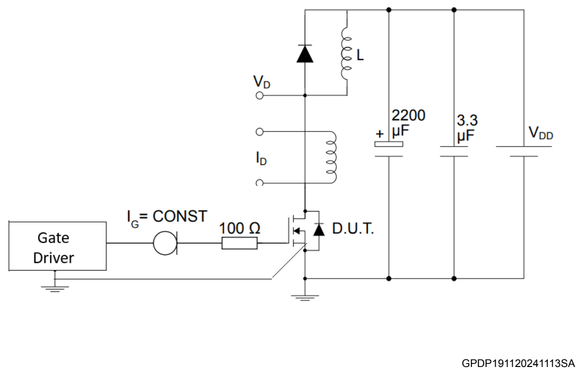


Figure 15. **Test circuit for inductive load switching and diode recovery times**

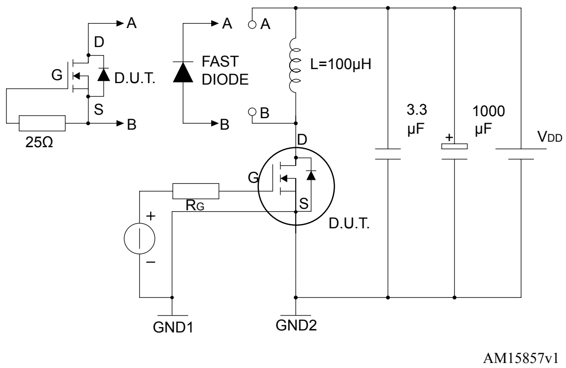


Figure 16. **Unclamped inductive load test circuit**

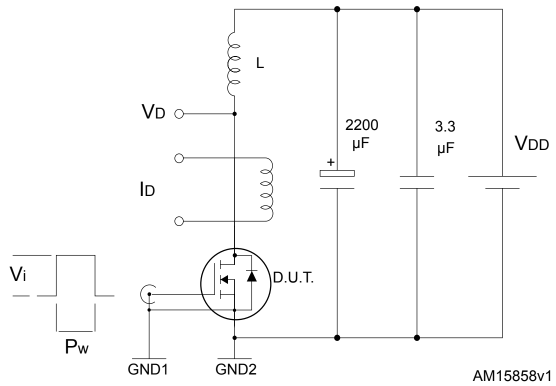


Figure 17. **Unclamped inductive waveform**

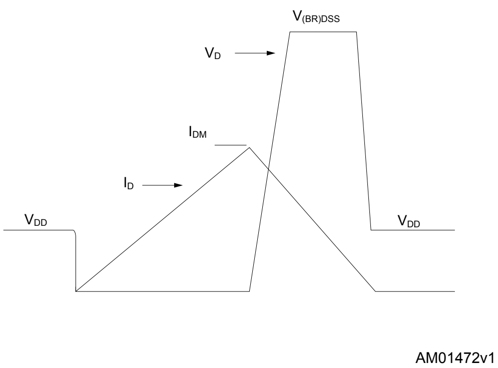
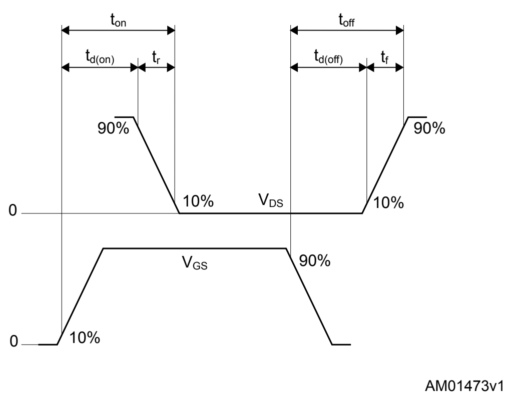


Figure 18. **Switching time waveform**



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL type A2 package information

Figure 19. TO-LL type A2 package outline

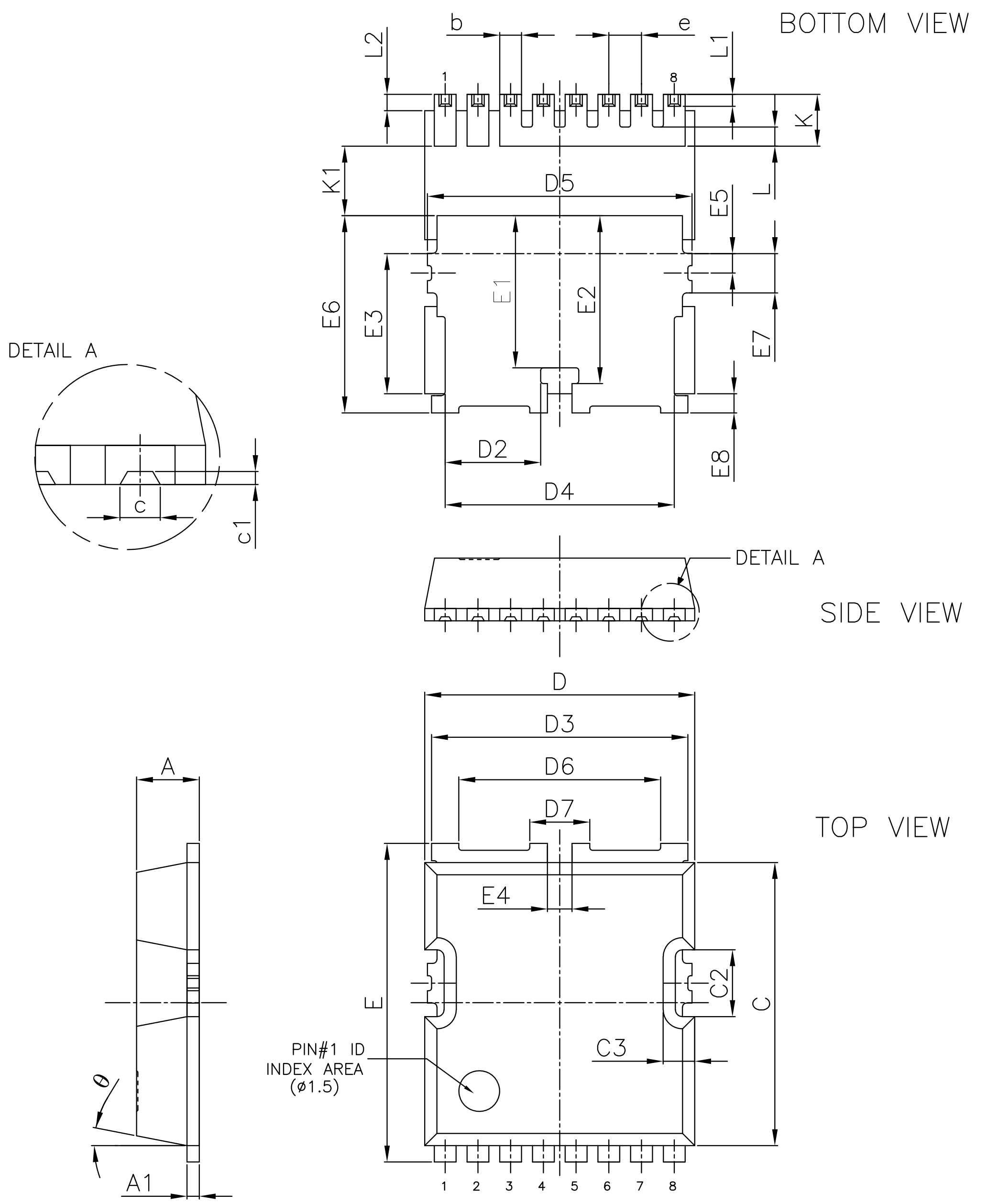
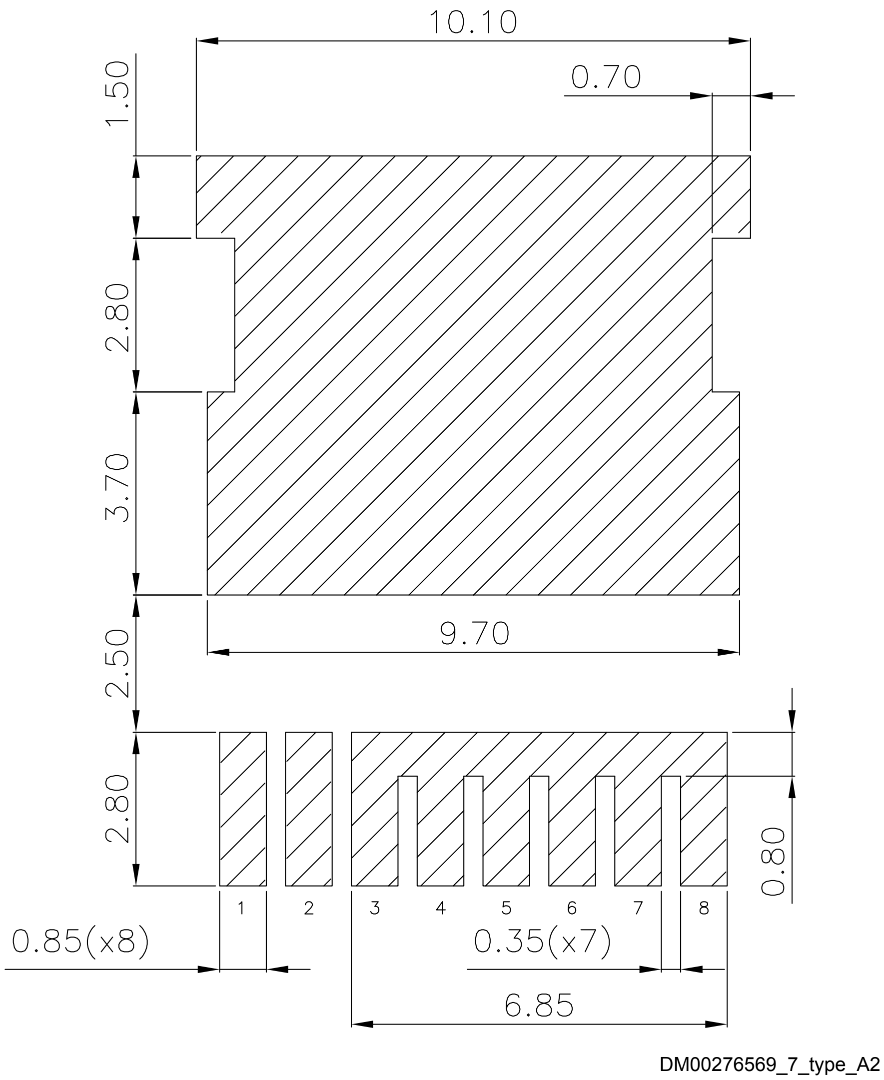


Table 8. TO-LL type A2 package mechanical data

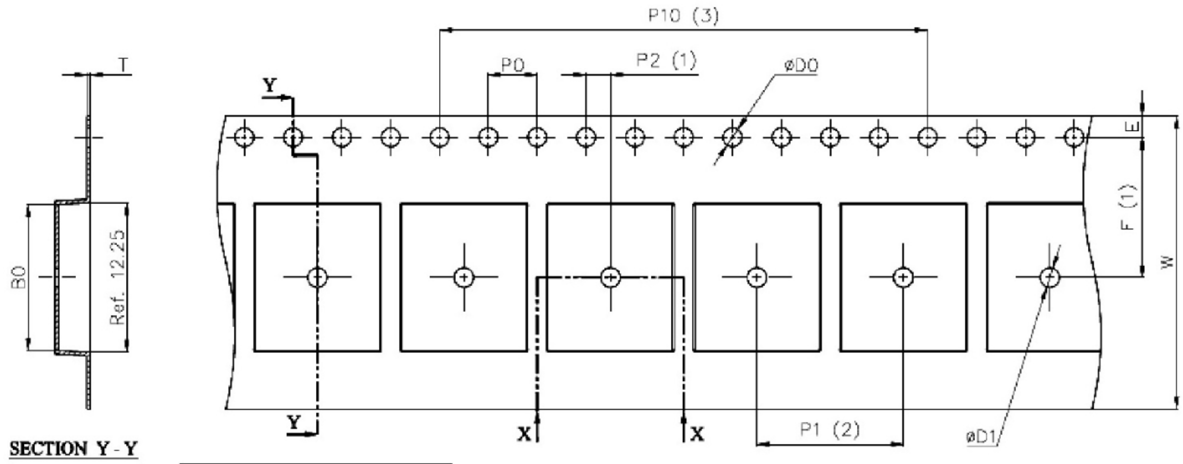
Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.40	0.48	0.60
b	0.70	0.80	0.90
c		0.46	
c1		0.15	
C	10.28	10.38	10.48
C2	2.35	2.45	2.55
C3		1.16	
D	9.80	9.90	10.00
D2	3.30	3.50	3.70
D3	9.30	9.40	9.50
D4	8.20	8.40	8.60
D5	9.50	9.70	9.90
D6		7.40	
D7		2.20	
e		1.20	
E	11.48	11.68	11.88
E1		5.58	
E2		6.15	
E3		5.14	
E4		0.90	
E5		0.72	
E6	7.03	7.23	7.43
E7		1.44	
E8	0.50	0.70	0.90
K	1.70	1.90	2.10
K1	2.40		
L		0.70	
L1		0.44	
L2	0.40	0.60	0.80
θ		11°	

Figure 20. **TO-LL type A2 recommended footprint (dimensions are in mm)**



4.2 TO-LL packing information

Figure 21. **Carrier tape outline and dimensions**



Dimension List			
Annote	Millimeter	Annote	Millimeter
A0	10.20±0.10	P2	2.00±0.10
B0	11.98±0.10	P10	40.00±0.20
K0	2.60±0.10	E	1.75±0.10
D0	$1.50^{+0.10}_{-0}$	F	11.50±0.10
D1	1.60±0.10	W	24.00±0.30
P0	4.00±0.10	T	0.30±0.05
P1	12.00±0.10		

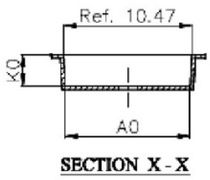
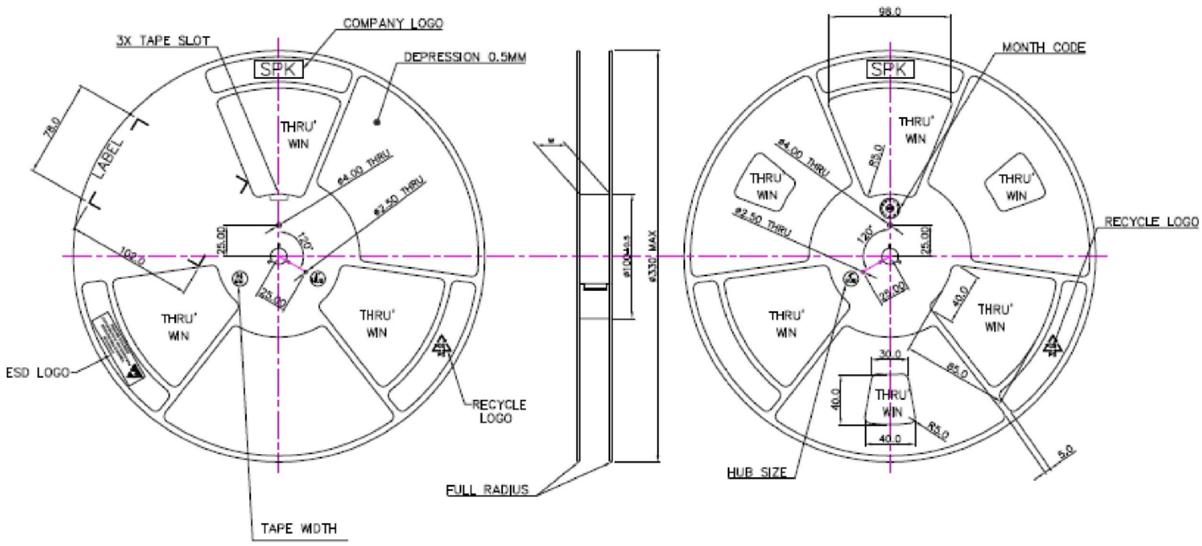


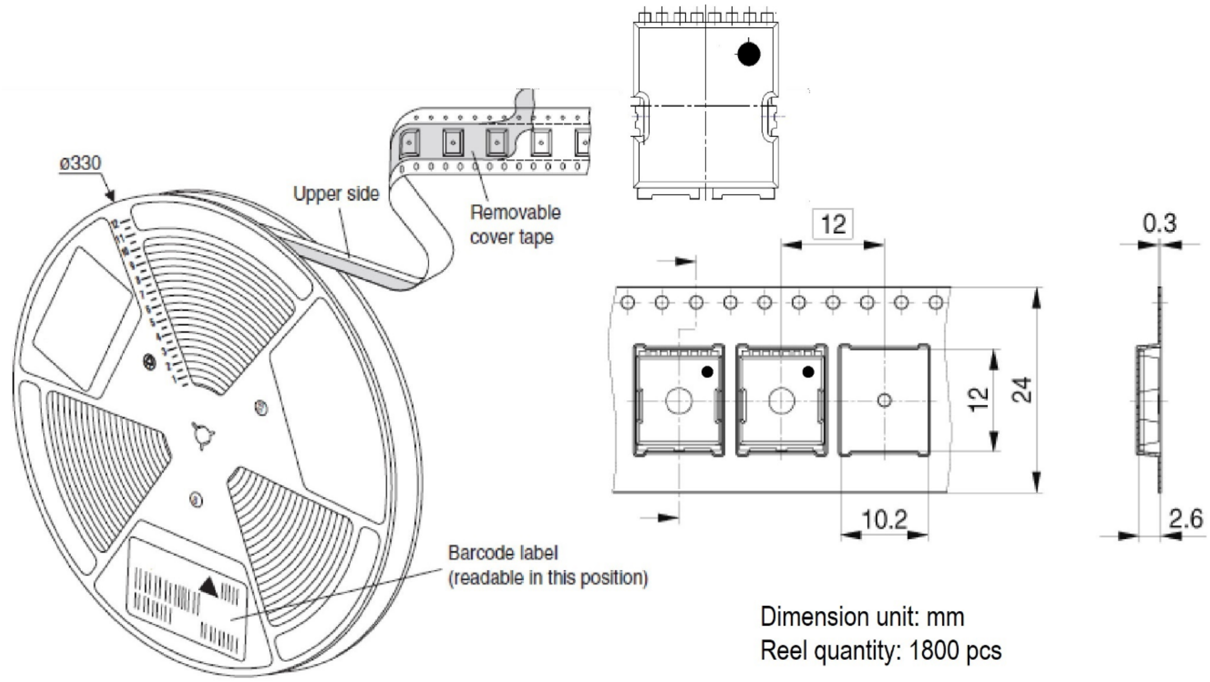
Figure 22. **Reel outline and dimensions**



SPECIFICATION							
TAPE WIDTH	W	U	X	V	Y	Z	P
24mm	24.4	1.50	24.5	20.0	0.55	6.00	2

Dimension unit: mm

Figure 23. TO-LL orientation in tape pocket



Revision history

Table 9. **Document revision history**

Date	Revision	Changes
04-Feb-2025	1	Fitrst release.

Contents