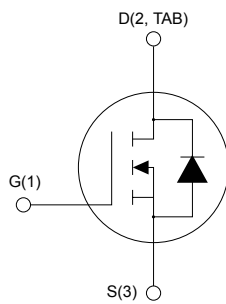
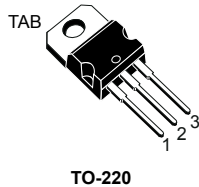


## N-channel 600 V, 280 mΩ typ., 11 A MDmesh II Power MOSFET in a TO-220 package



AM01475v1\_noZen


**Product status link**
[STP13NM60N](#)
**Product summary**

<b>Order code</b>	STP13NM60N
<b>Marking</b>	13NM60N
<b>Package</b>	TO-220
<b>Packing</b>	Tube

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP13NM60N	600 V	360 mΩ	11 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.9	
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max)	3.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	200	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.39	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	
$I_{GSS}$	Gate body leakage current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.5\text{ A}$		280	360	m $\Omega$

1. Specified by design, not tested in production.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	790	-	pF
$C_{oss}$	Output capacitance		-	60	-	pF
$C_{riss}$	Reverse transfer capacitance		-	3.6	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	135	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	4.7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 11\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	27	-	nC
$Q_{gs}$	Gate-source charge		-	4	-	nC
$Q_{gd}$	Gate-drain charge		-	14	-	nC

1.  $C_{oss\text{ eq.}}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 5.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	3	-	ns
$t_r$	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
$t_f$	Fall time		-	10	-	ns

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$	-	230		ns
$Q_{rr}$	Reverse recovery charge	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ ,	-	290		ns
$Q_{rr}$	Reverse recovery charge	$T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	2.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

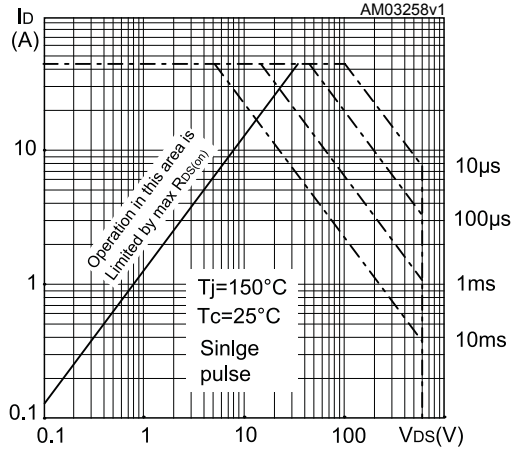


Figure 2. Normalized transient thermal impedance

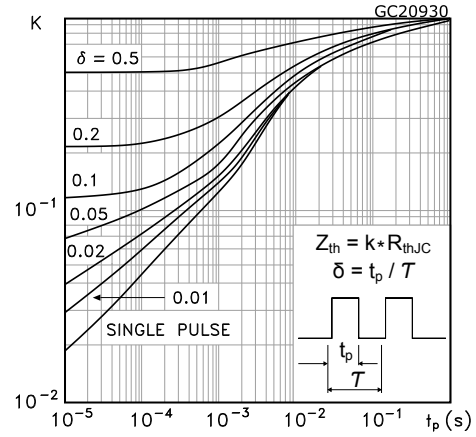


Figure 3. Typical output characteristics

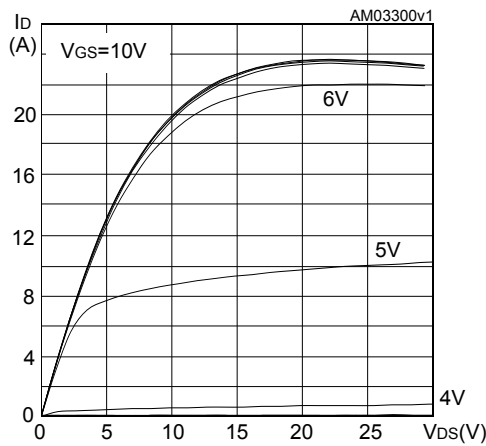


Figure 4. Typical transfer characteristics

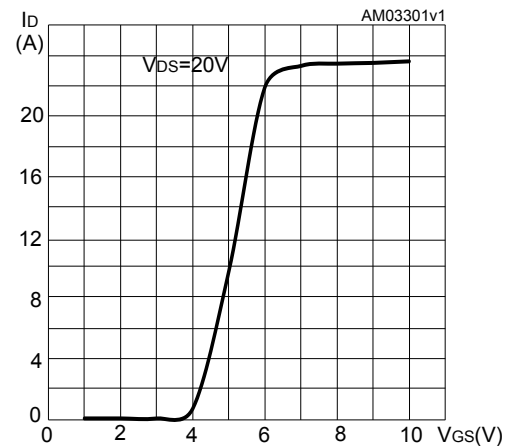


Figure 5. Normalized gate threshold vs temperature

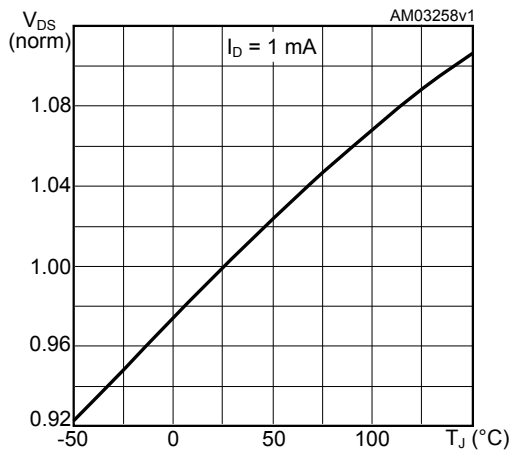
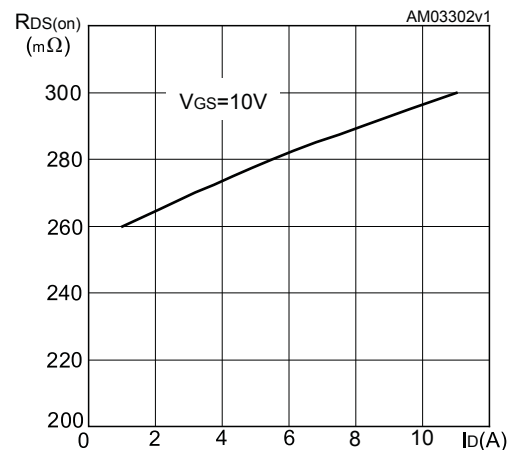
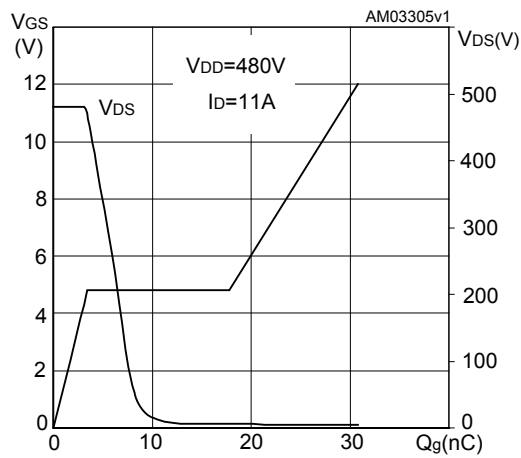


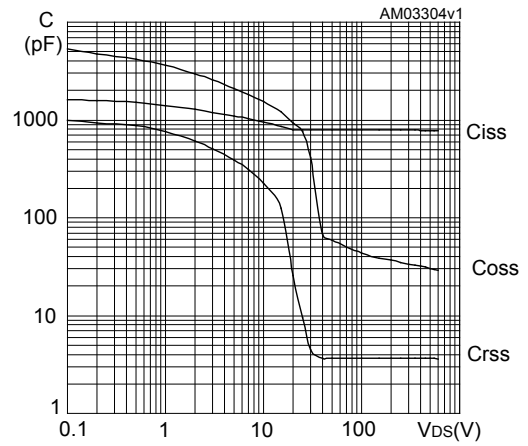
Figure 6. Typical drain-source on-resistance



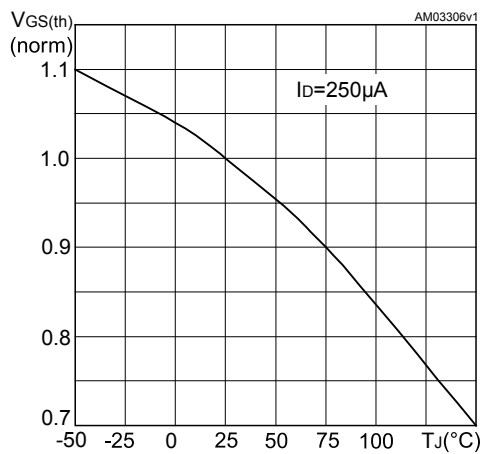
**Figure 7. Typical gate charge characteristics**



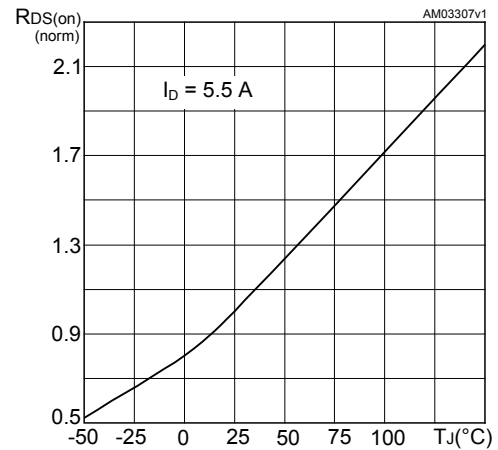
**Figure 8. Typical capacitance characteristics**



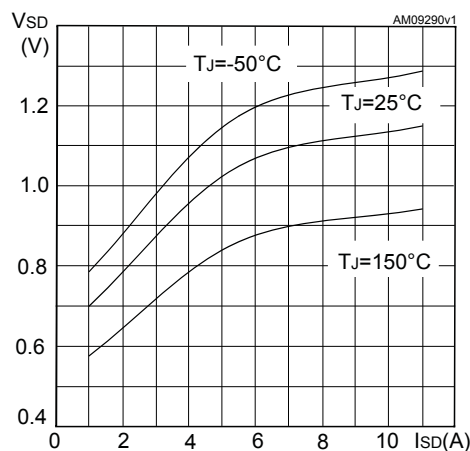
**Figure 9. Normalized gate threshold vs temperature**



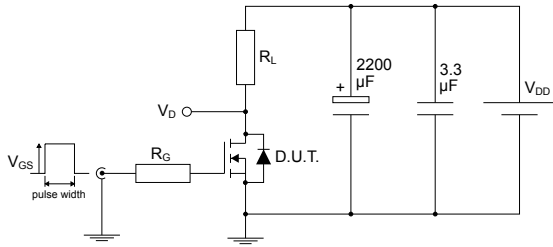
**Figure 10. Normalized on-resistance vs temperature**



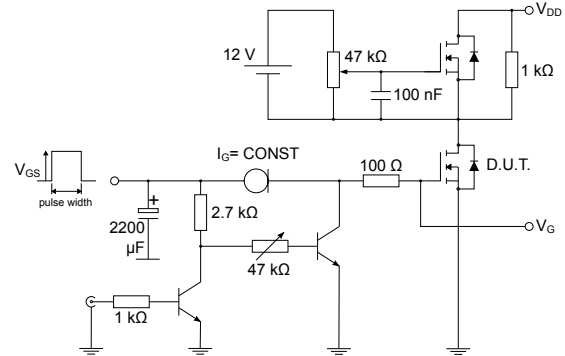
**Figure 11. Typical reverse diode forward characteristics**



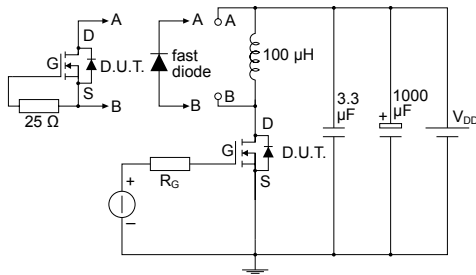
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


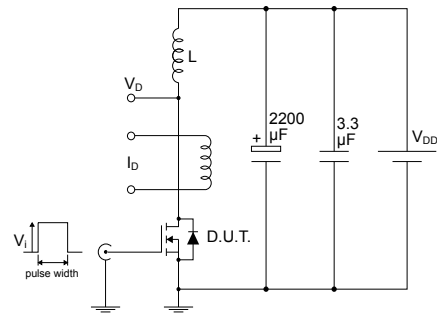
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**Figure 13. Test circuit for gate charge behavior**


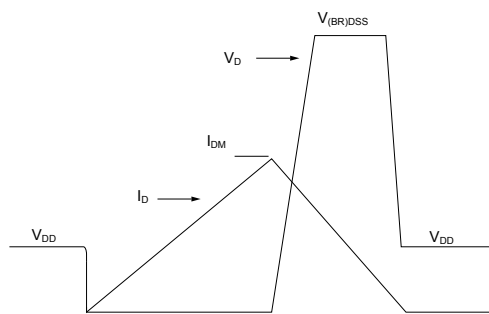
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**Figure 14. Test circuit for inductive load switching and diode recovery times**


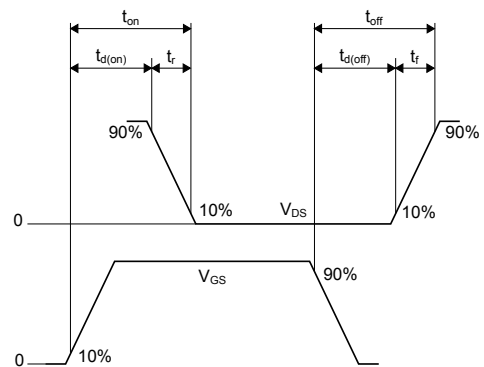
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**Figure 15. Unclamped inductive load test circuit**


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**Figure 16. Unclamped inductive waveform**


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**Figure 17. Switching time waveform**


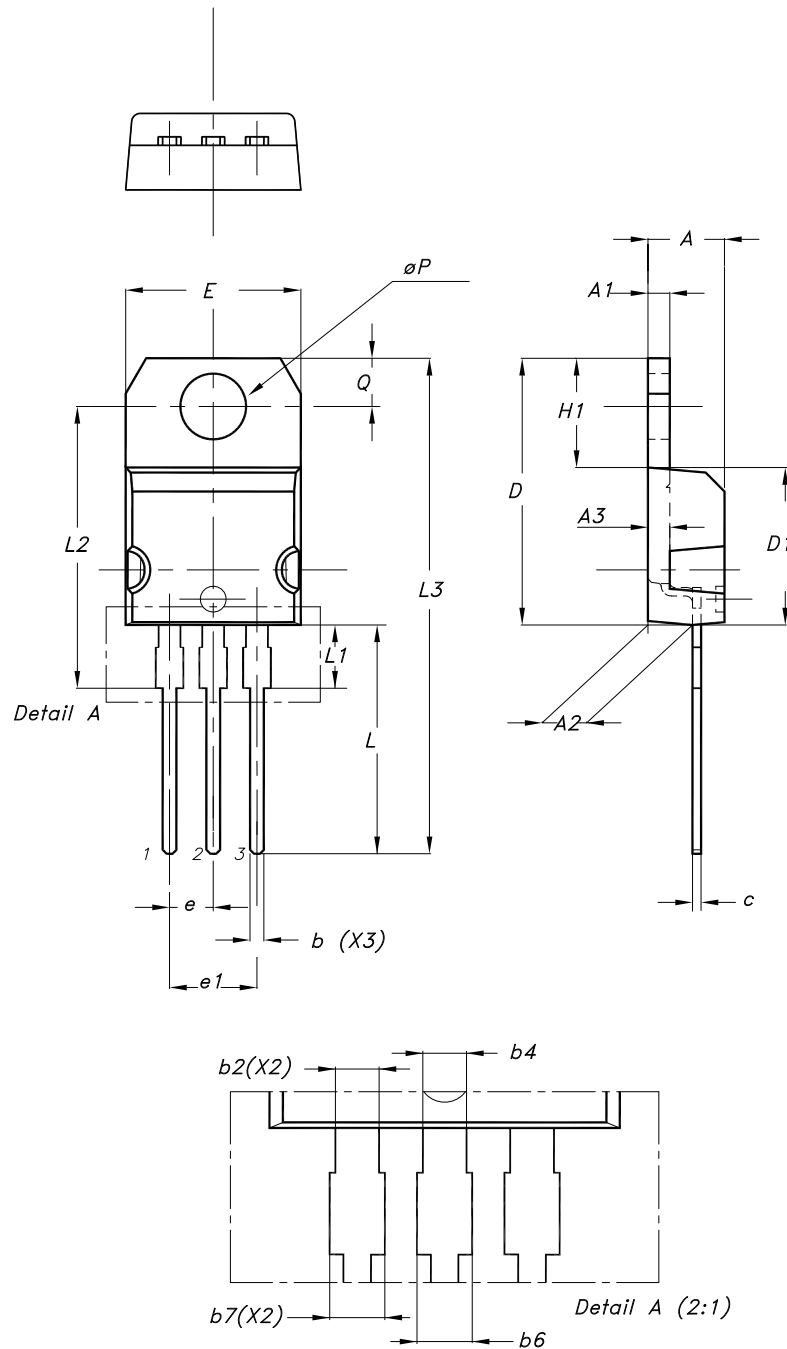
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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type H package information

Figure 18. TO-220 type H package outline



0015988\_H\_23



**Table 7. TO-220 type H package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	4.45	4.50
A1	1.22		1.32
A2	2.49	2.59	2.69
A3	1.17	1.27	1.37
b	0.78		0.87
b2	1.25		1.34
b4	1.20		1.29
b6			1.50
b7			1.45
c	0.49		0.56
D	15.40	15.50	15.60
D1	9.05	9.15	9.25
E	10.08	10.18	10.28
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
H1	6.25	6.35	6.45
L	13.20	13.40	13.60
L1	3.50	3.70	3.90
L2	16.30	16.40	16.50
L3	28.70	28.90	29.10
ØP	3.75	3.80	3.85
Q	2.70	2.80	2.90
Slug flatness		0.03	0.10

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
15-Dec-2023	1	First release. Part number STP13NM60N previously included in datasheet DS6112.

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