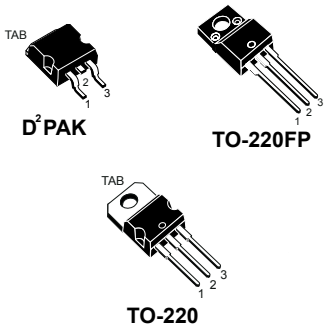
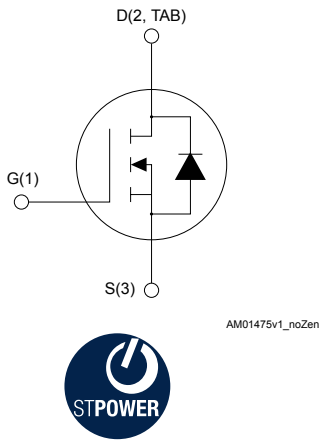
STB45N65M5, STF45N65M5, STP45N65M5

Datasheet

N-channel 650 V, 67 mΩ typ., 35 A MDmesh M5 Power MOSFETs in a D²PAK, TO-220FP and TO-220 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB45N65M5	650 V	78 mΩ	35 A
STF45N65M5			
STP45N65M5			

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Extremely low $R_{DS(on)}$
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status links
STB45N65M5
STF45N65M5
STP45N65M5

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK TO-220	TO-220FP	
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	35		A
I_D	Drain current (continuous) at T_C = 100 °C	22		A
I_{DM}(1)	Drain current (pulsed)	140		A
P_{TOT}	Total power dissipation at T_C = 25 °C	210	40	W
dv/dt(2)	Peak diode recovery voltage slope	15		V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	-	2.5	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range	150		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 35 A, di/dt ≤ 400 A/µs; V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DD} ≤ 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D^2PAK	TO-220	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	0.60		3.13	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30(1)	62.5		°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	810	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)	-	-	100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 17.5 A	-	67	78	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	3470	-	pF
C_{oss}	Output capacitance		-	82	-	
C_{rss}	Reverse transfer capacitance		-	7	-	
$C_{o(tr)}$(1)	Equivalent output capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	280	-	pF
$C_{o(er)}$(2)	Equivalent output capacitance energy related		-	79	-	pF
R_g	Gate input resistance	f = 1 MHz open drain	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 17.5 A, V_{GS} = 0 to 10 V (see the Figure 17. Test circuit for gate charge behavior)	-	82	-	nC
Q_{gs}	Gate-source charge		-	18.5	-	
Q_{gd}	Gate-drain charge		-	35	-	

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as Coss while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	V_{DD} = 400 V, I_D = 23 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 18. Test circuit for inductive load switching and diode recovery times and Figure 21. Switching time waveform)	-	79.5	-	ns
$t_{r(v)}$	Voltage rise time		-	11	-	
$t_{c(off)}$	Crossing time off		-	9.3	-	
$t_{f(i)}$	Current fall time		-	16	-	

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	35	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	140	
V_{SD}(2)	Forward on voltage	I_{SD} = 35 A, V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 35 A, di/dt = 100 A/µs V_{DD} = 100 V (see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	392	-	ns
Q_{rr}	Reverse recovery charge		-	7.4	-	µC
I_{RRM}	Reverse recovery current		-	38	-	A
t_{rr}	Reverse recovery time	I_{SD} = 35 A, di/dt = 100 A/µs V_{DD} = 100 V, T_J = 150 °C (see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	468	-	ns
Q_{rr}	Reverse recovery charge		-	9.7	-	µC
I_{RRM}	Reverse recovery current		-	42	-	A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK and TO-220

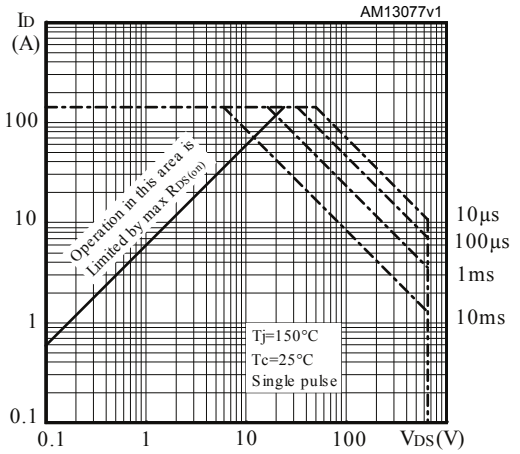


Figure 2. Normalized transient thermal impedance for D²PAK and TO-220

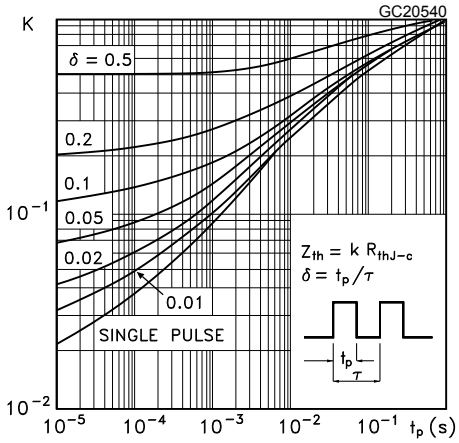


Figure 3. Safe operating area for TO-220FP

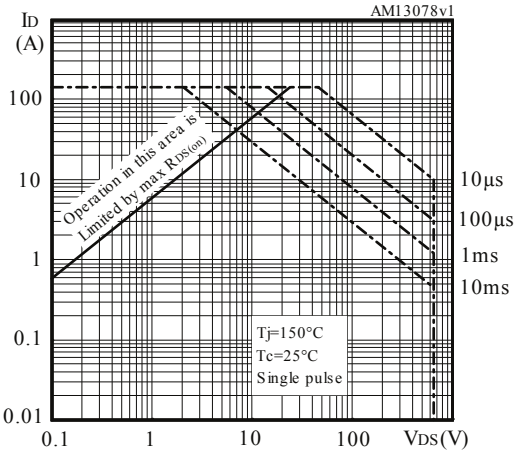


Figure 4. Normalized transient thermal impedance for TO-220FP

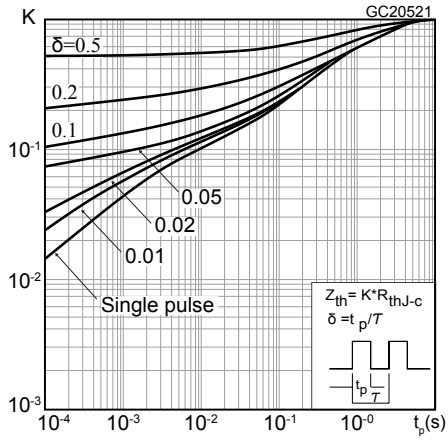


Figure 5. Output characteristics

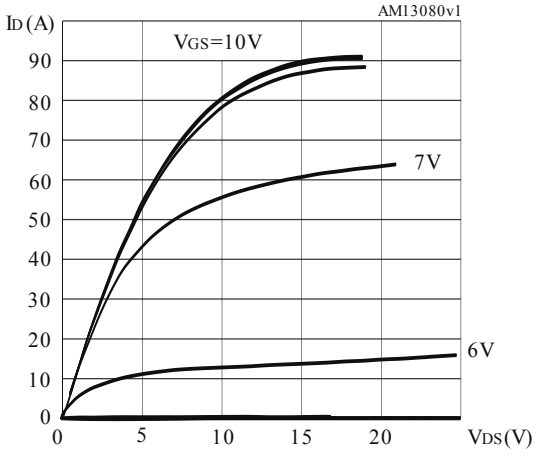


Figure 6. Transfer characteristics

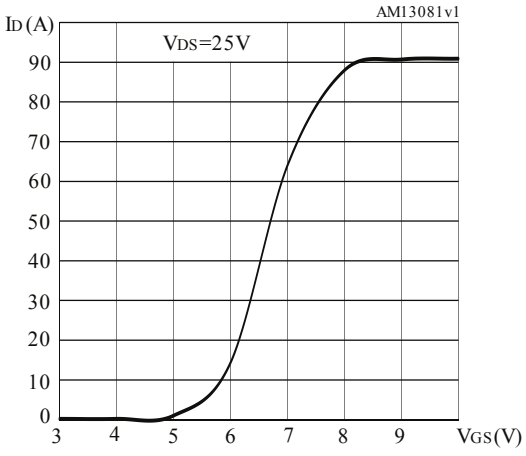


Figure 7. Gate charge vs gate-source voltage

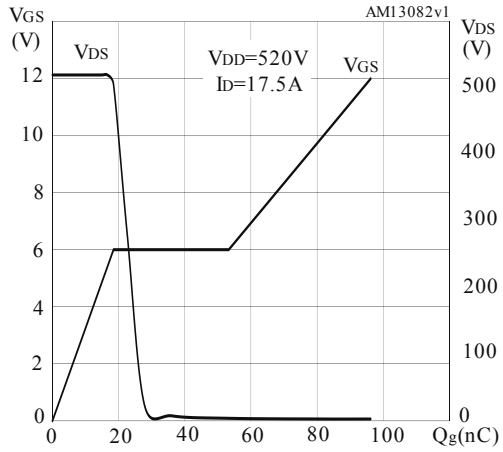


Figure 8. Static drain-source on-resistance

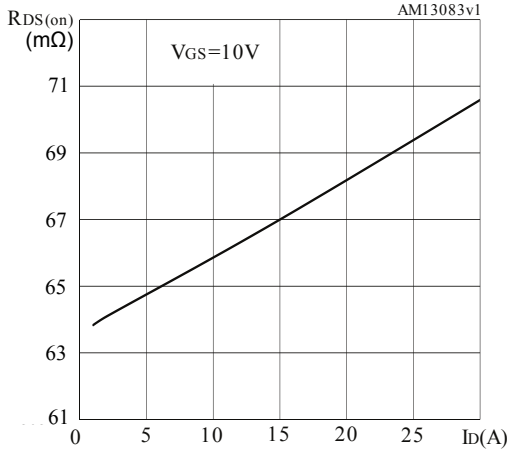


Figure 9. Capacitance variations

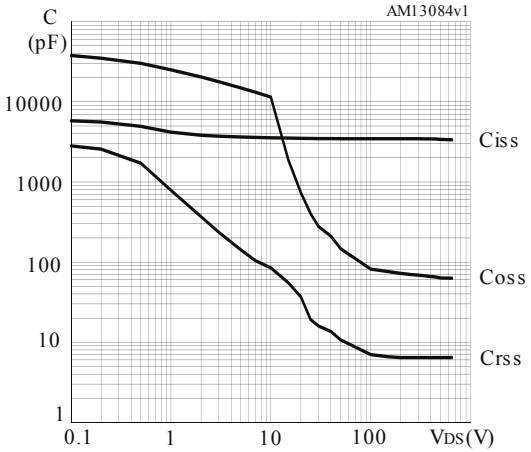


Figure 10. Output capacitance stored energy

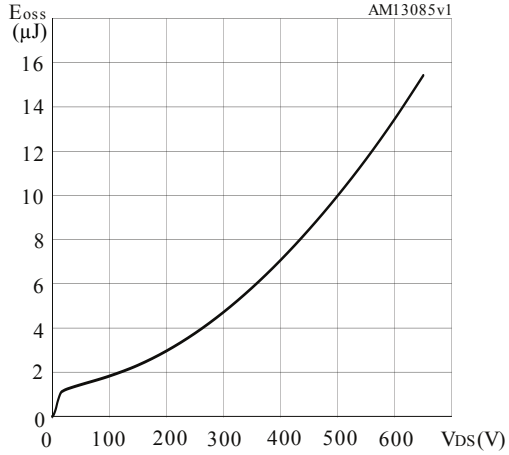


Figure 11. Normalized gate threshold voltage vs temperature

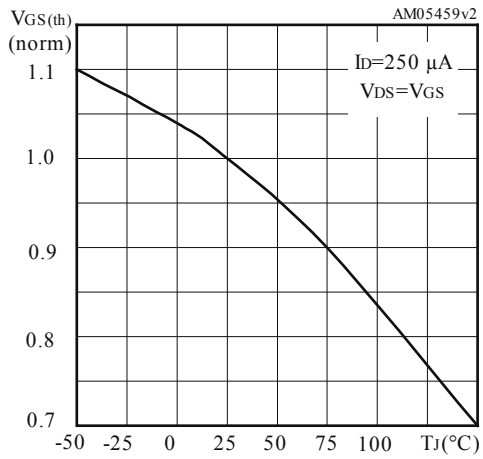


Figure 12. Normalized on-resistance vs temperature

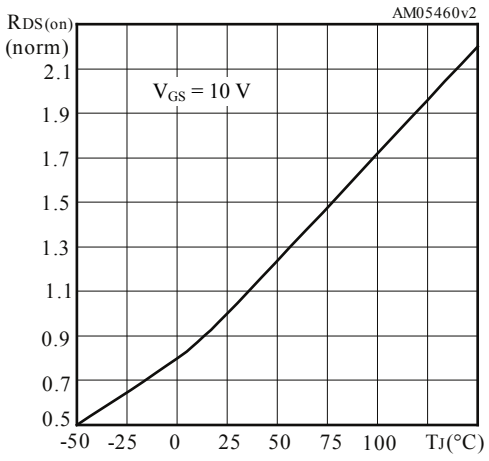


Figure 13. Drain-source diode forward characteristics

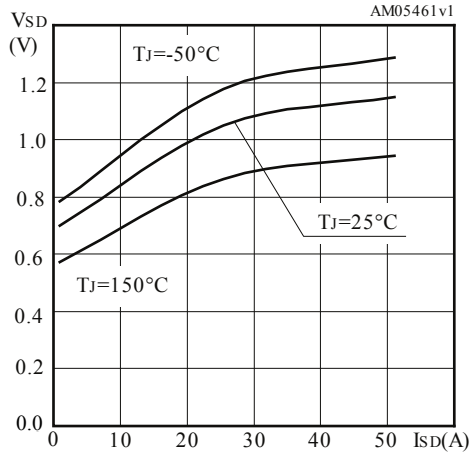


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

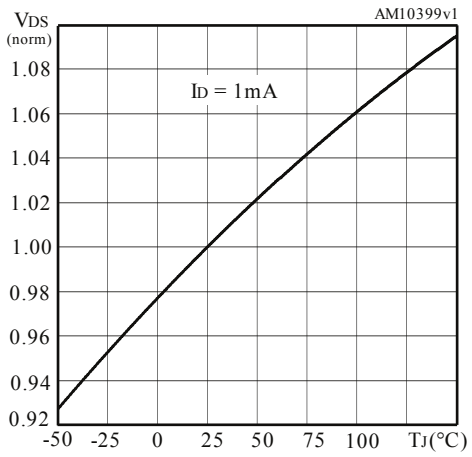
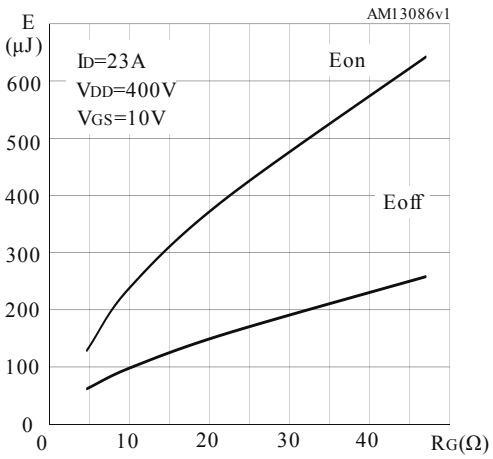


Figure 15. Switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

3 Test circuits

Figure 16. Test circuit for resistive load switching times

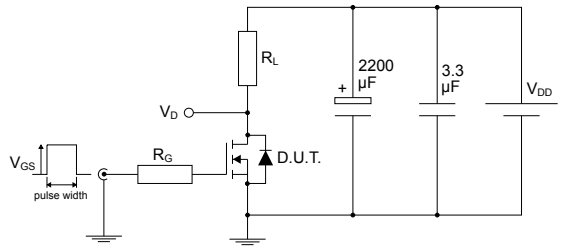


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Figure 17. Test circuit for gate charge behavior

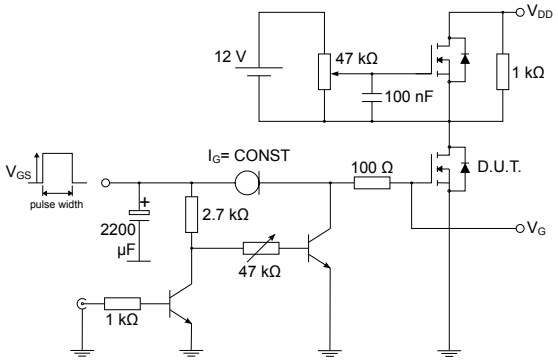

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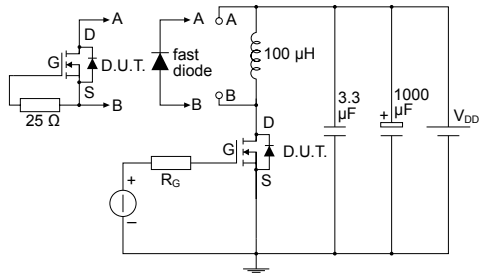
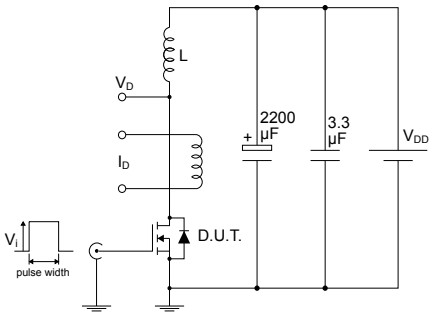
Figure 18. Test circuit for inductive load switching and diode recovery times



AM01470v1

Figure 19. Unclamped inductive load test circuit



AM01471v1

Figure 20. Unclamped inductive waveform

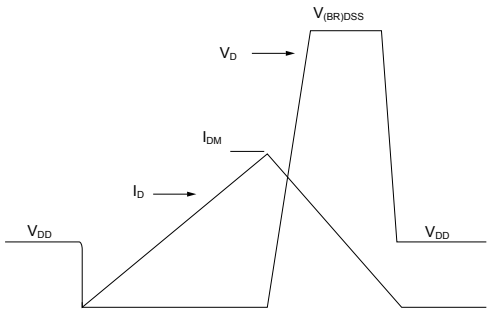


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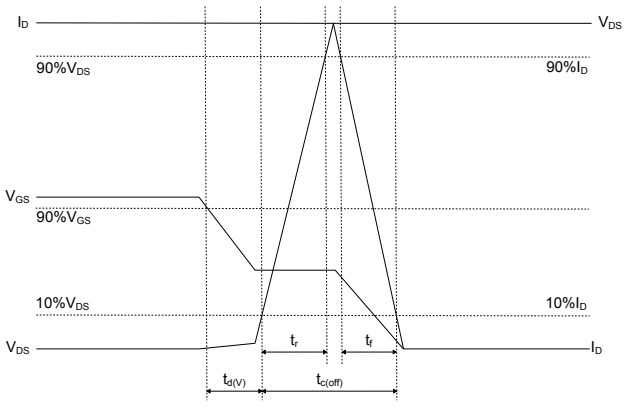
Figure 21. Switching time waveform



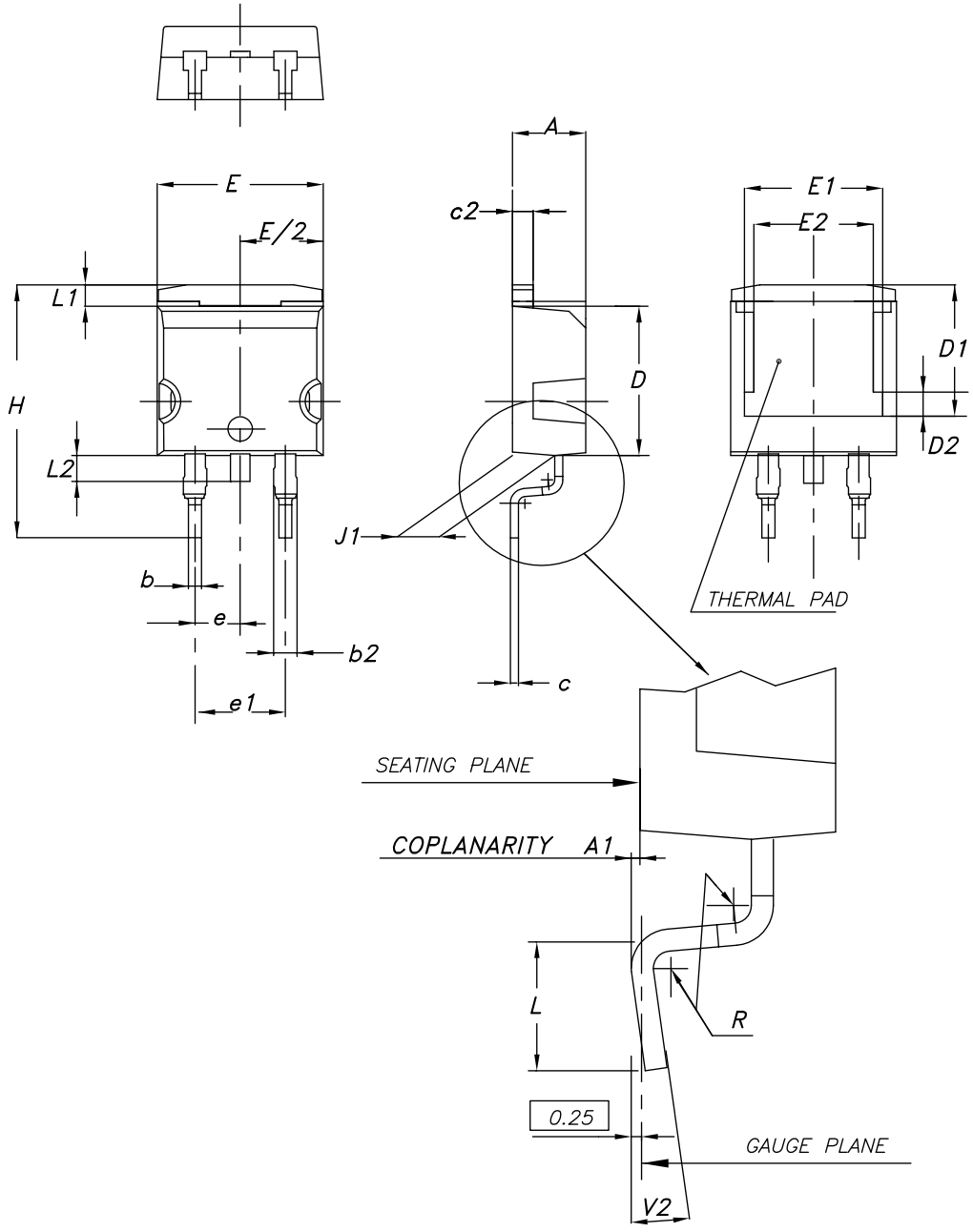
AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 22. D²PAK (TO-263) type A2 package outline

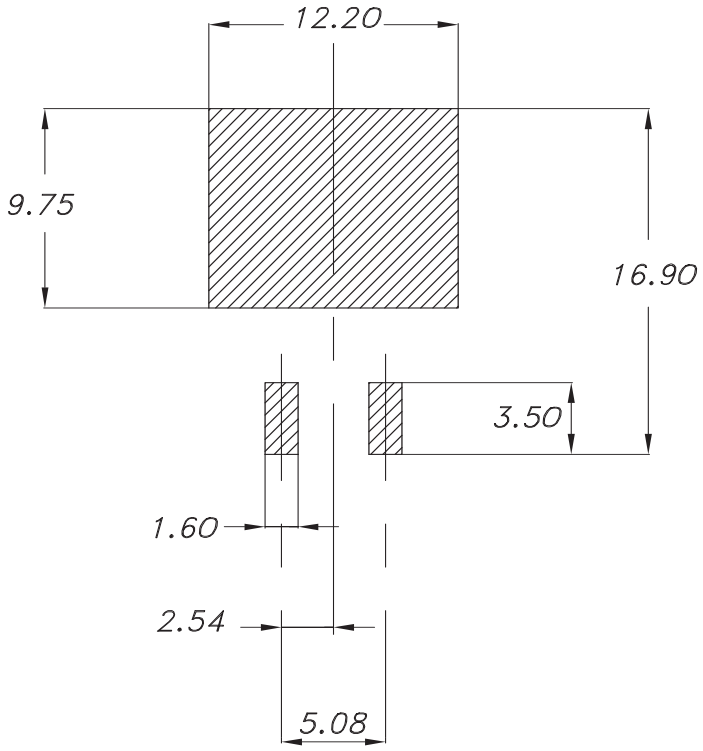


0079457_A2_27

Table 8. **D²PAK (TO-263) type A2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 23. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220FP type B package information

Figure 24. **TO-220FP type B package outline**

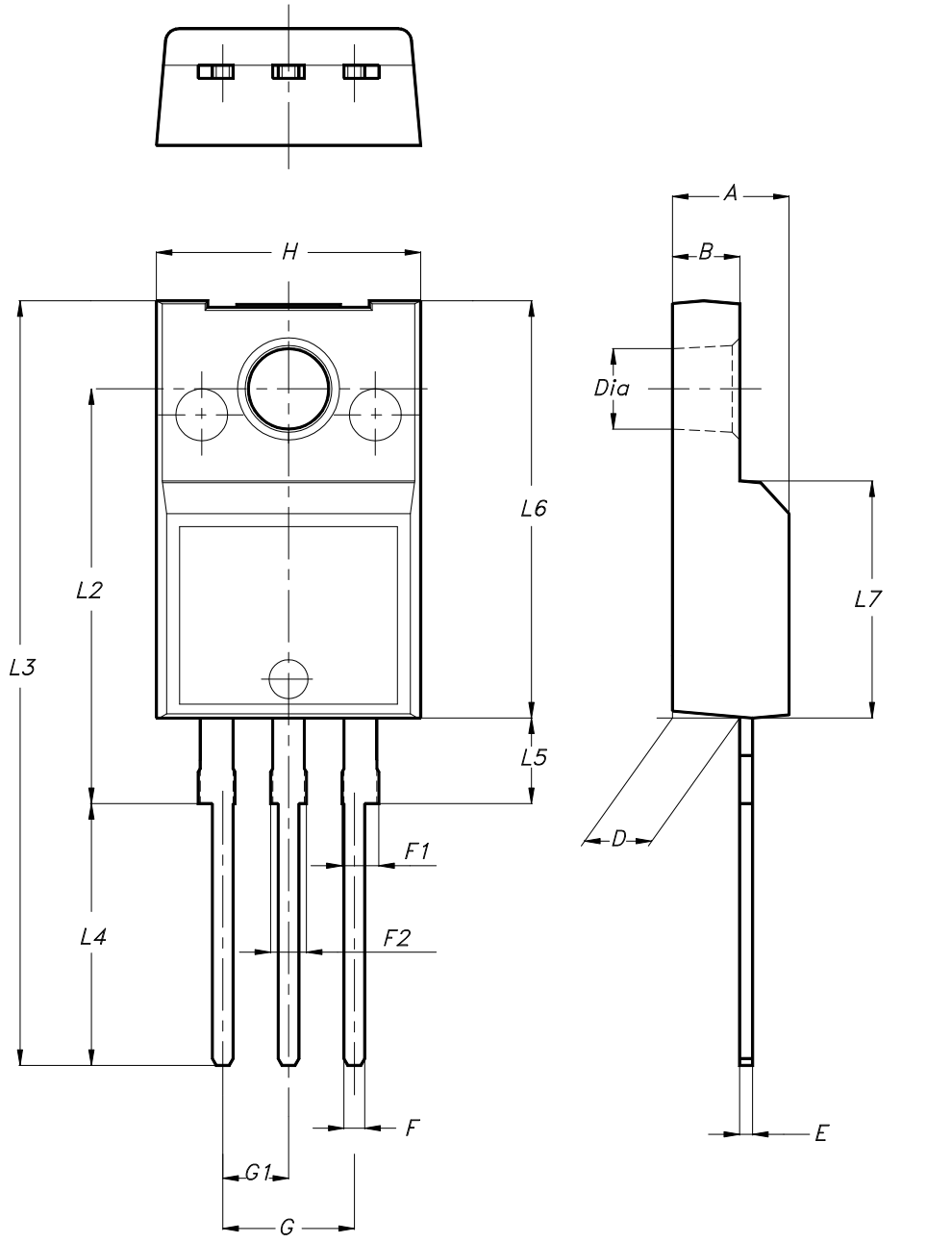


Table 9. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.3 TO-220 type A package information

Figure 25. **TO-220 type A package outline**

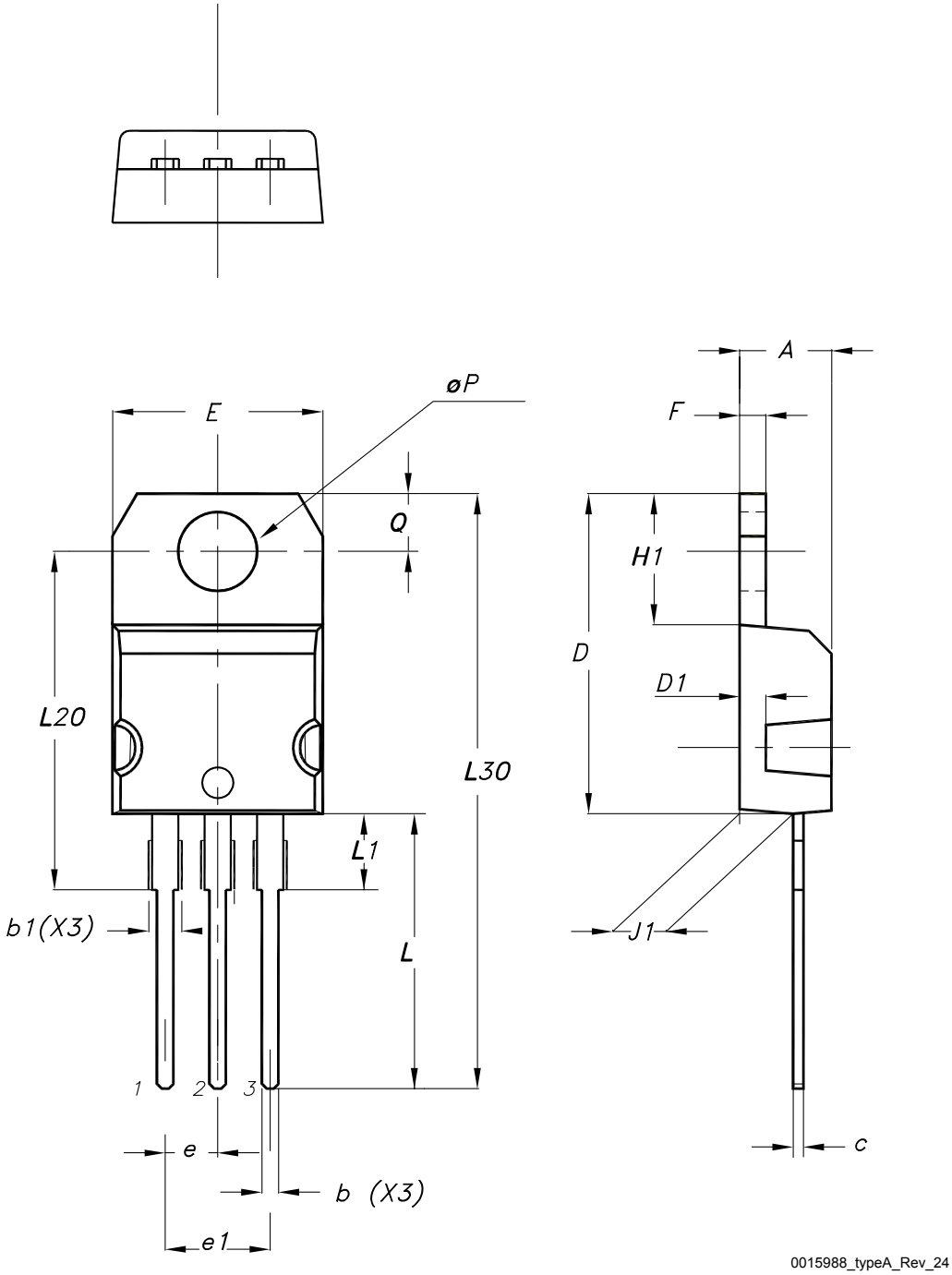
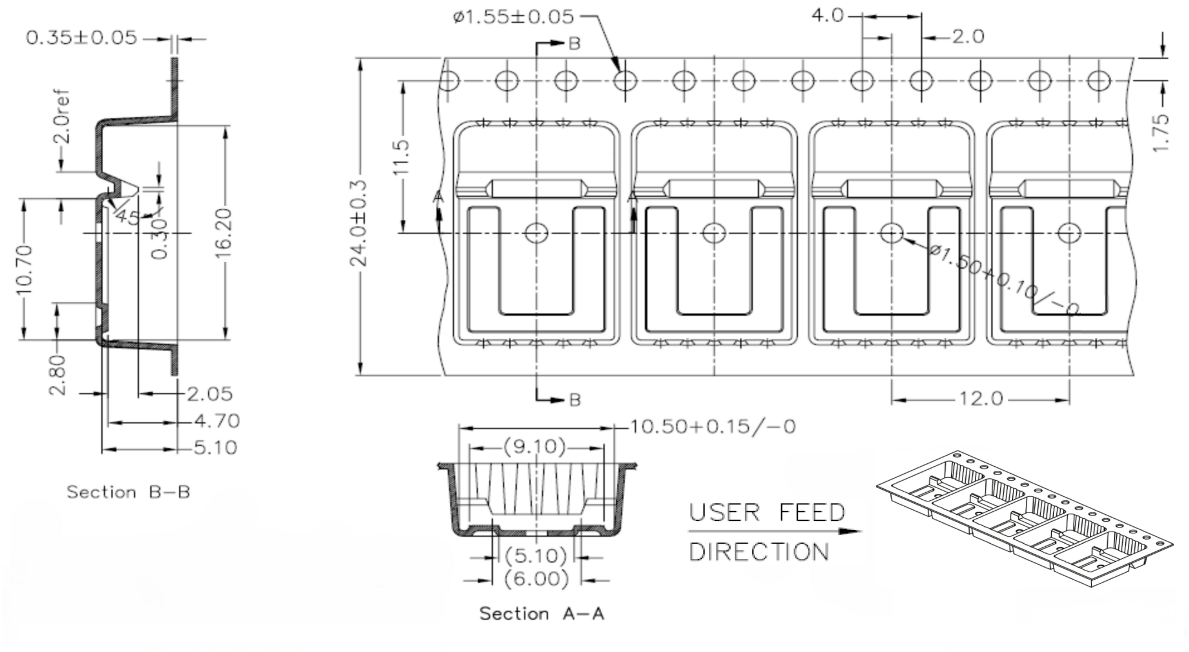


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 D²PAK packing information

Figure 26. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

5 Ordering information

Table 11. **Order codes**

Order codes	Marking	Package	Packing
STB45N65M5	45N65M5	D²PAK	Tape and reel
STF45N65M5		TO-220FP	Tube
STP45N65M5		TO-220	

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
22-Feb-2012	1	First release.
28-Aug-2012	2	Document status promoted from preliminary data to production data. Inserted *Section 2.1: Electrical characteristics (curves)*.
05-Dec-2012	3	The part number STW45N65M5 has been moved to a separate datasheet.
05-Mar-2013	4	Added dv/dt value on *Table 2: Absolute maximum ratings*. Minor text changes.
22-Sep-2025	5	Updated Section 4: Package information. Minor text changes.

Contents