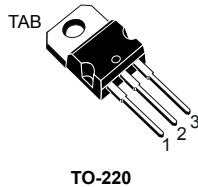
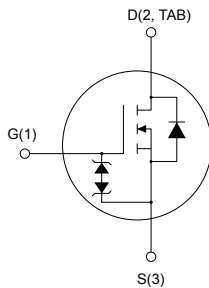


## N-channel 800 V, 2.1 $\Omega$ typ., 3 A MDmesh K5 Power MOSFET in a TO-220 package



TO-220



AM01476v1\_tab



### Product status link

[STP4LN80K5](#)

### Product summary

<b>Order code</b>	STP4LN80K5
<b>Marking</b>	4LN80K5
<b>Package</b>	TO-220
<b>Packing</b>	Tube

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP4LN80K5	800 V	2.6 $\Omega$	3 A

- Ultra-low gate charge
- Very low FoM (figure of merit)
- Zener-protected
- 100% avalanche tested

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	3	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.9	
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 3\text{ A}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
3.  $V_{DD} \leq 640\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	2.08	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	0.8	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	160	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			50	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1\text{ A}$		2.1	2.6	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	122	-	pF
$C_{oss}$	Output capacitance		-	11	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.3	-	pF
$C_{o(tr)}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }640\text{ V}$ , $V_{GS} = 0\text{ V}$	-	23	-	pF
$C_{o(er)}^{(2)}$	Equivalent output capacitance energy related		-	9	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	18	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}$ , $I_D = 2.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	3.7	-	nC
$Q_{gs}$	Gate-source charge		-	1	-	nC
$Q_{gd}$	Gate-drain charge		-	2.2	-	nC

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 1.25\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	7	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for gate charge behavior and Figure 18. Switching time waveform)	-	31	-	ns
$t_f$	Fall time		-	25	-	ns

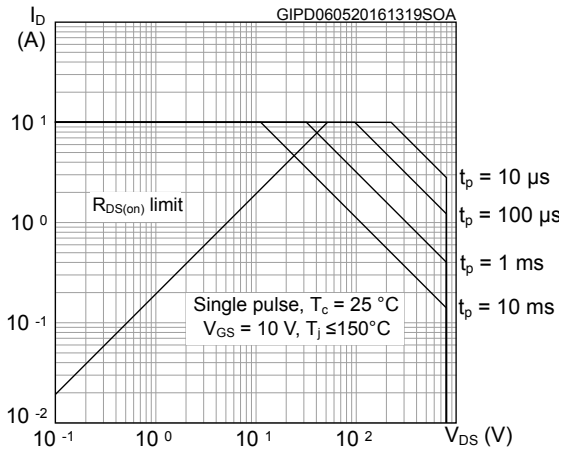
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		12	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 2.5\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	230		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	1.04		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	368		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	1.53		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8		A

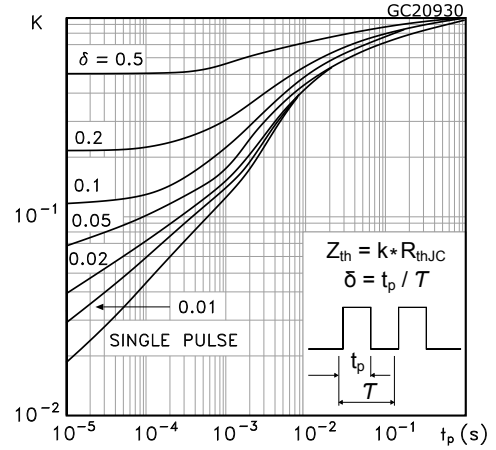
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

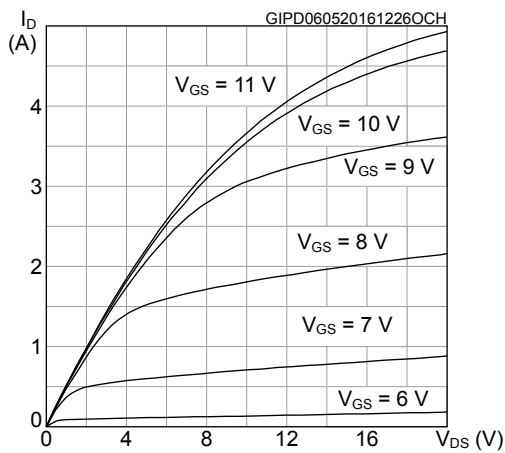
**Figure 1. Safe operating area**



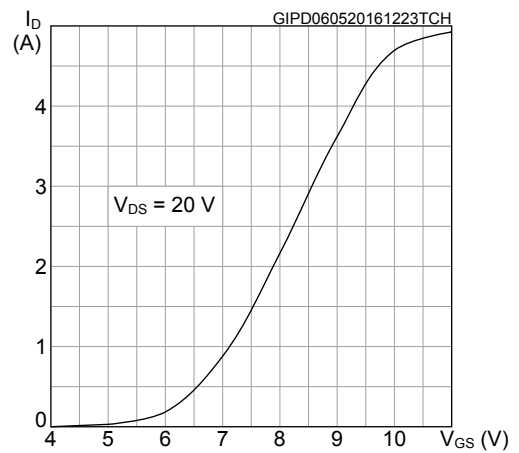
**Figure 2. Normalized transient thermal impedance**



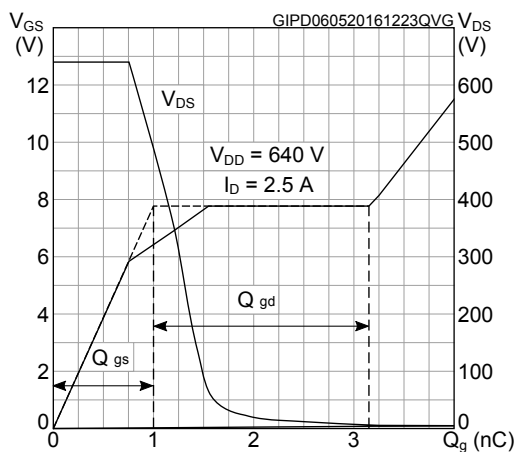
**Figure 3. Typical output characteristics**



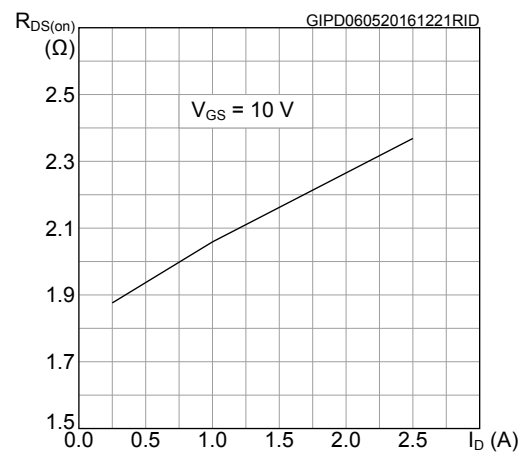
**Figure 4. Typical transfer characteristics**



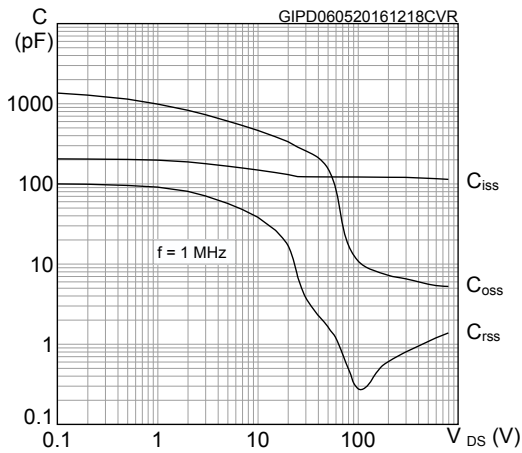
**Figure 5. Typical gate charge characteristics**



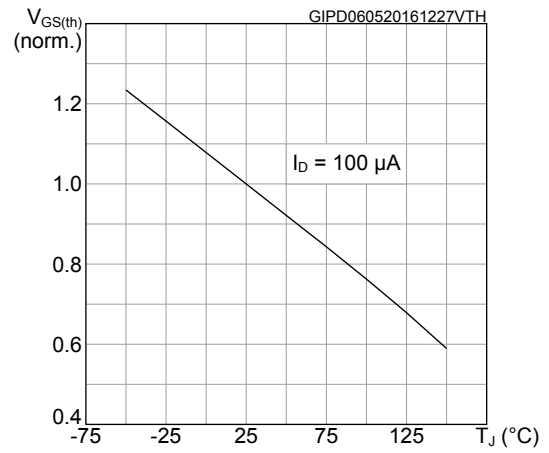
**Figure 6. Typical drain-source on-resistance**



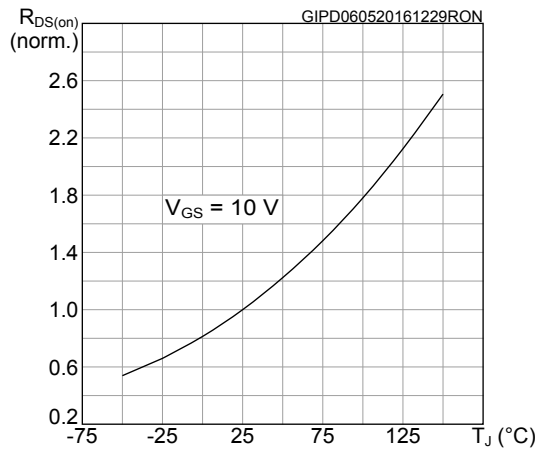
**Figure 7. Typical capacitance characteristics**



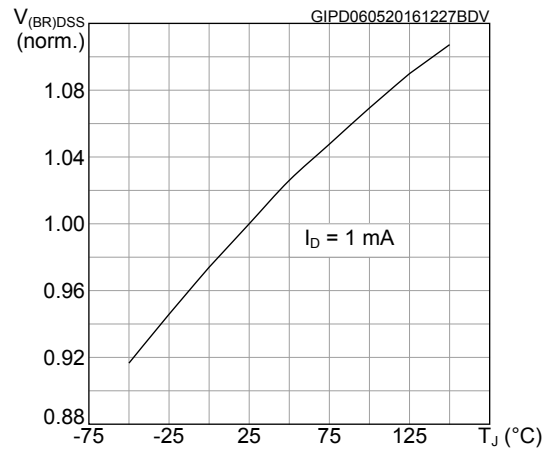
**Figure 8. Normalized gate threshold vs temperature**



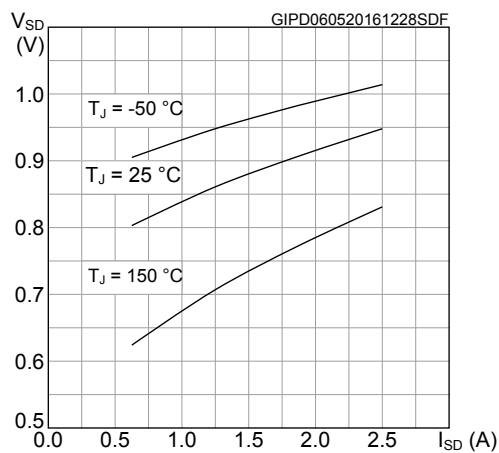
**Figure 9. Normalized on-resistance vs temperature**



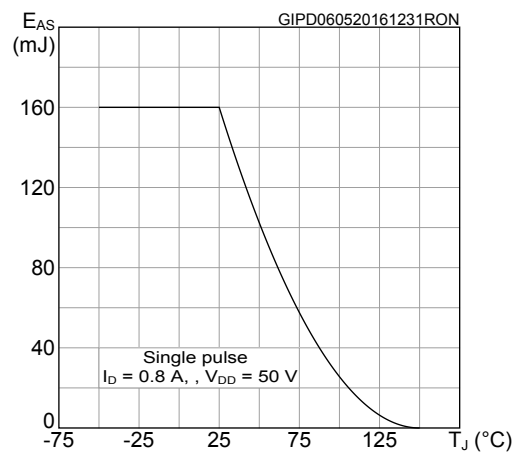
**Figure 10. Normalized breakdown voltage vs temperature**



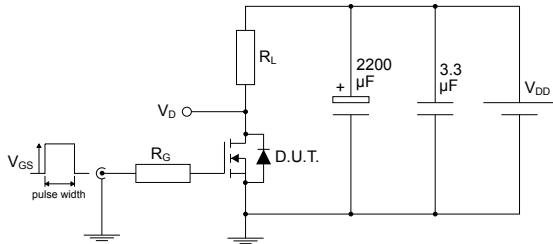
**Figure 11. Typical reverse diode forward characteristics**



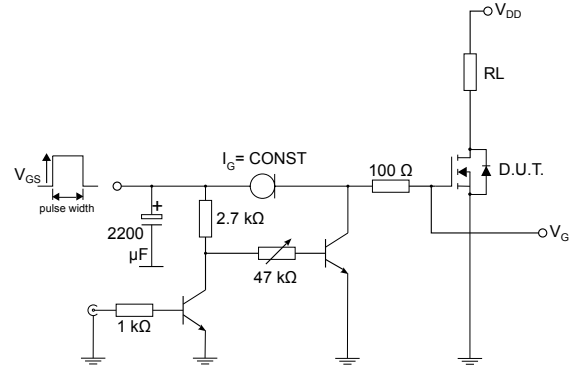
**Figure 12. Maximum avalanche energy vs temperature**



### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


AM01468v1

**Figure 14. Test circuit for gate charge behavior**


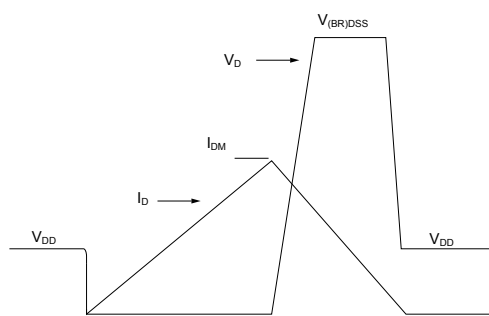
AM01469v10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


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**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**

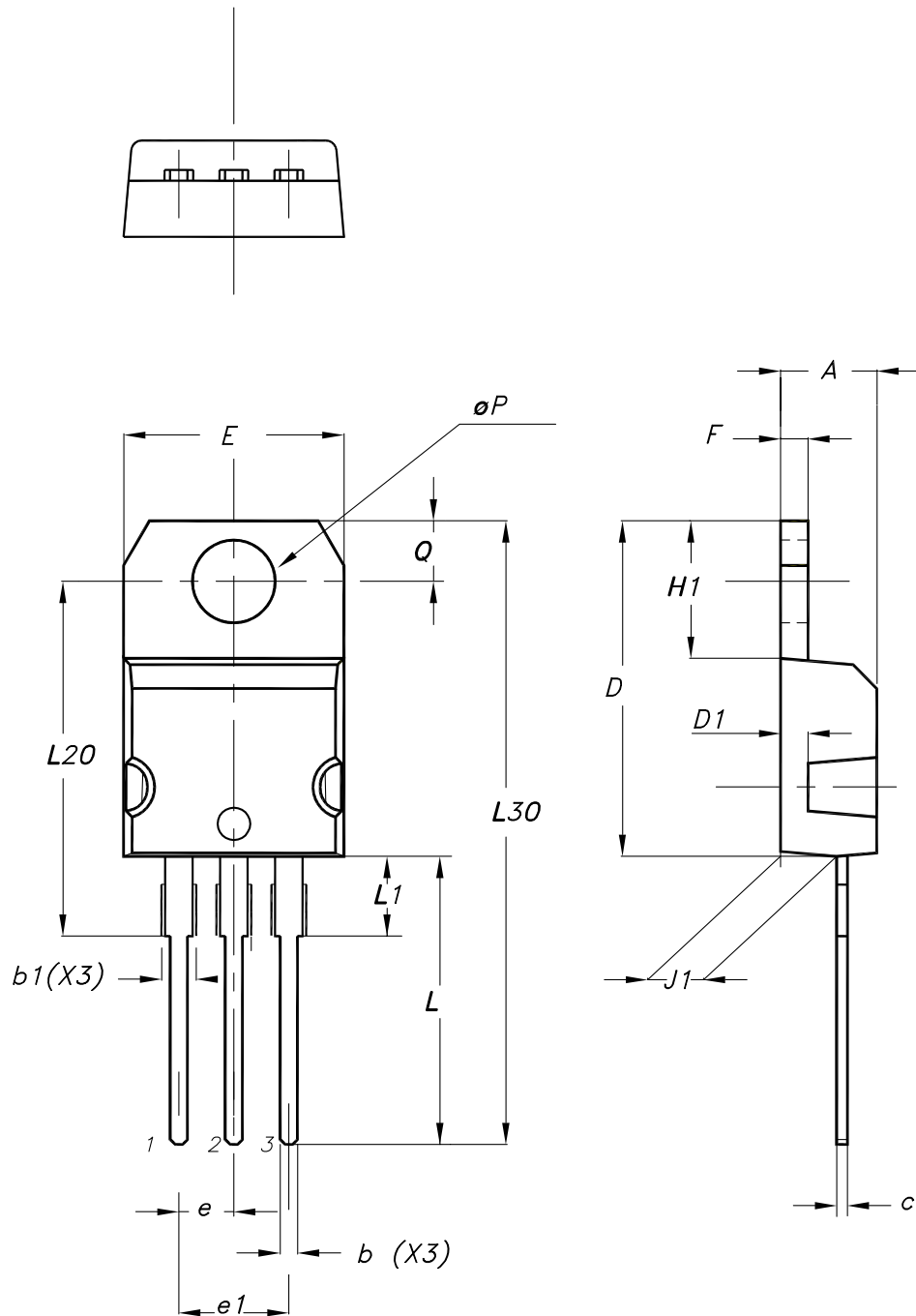

AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988\_typeA\_Rev\_24

**Table 8. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-May-2015	1	First release.
18-May-2016	2	Document status promoted from preliminary data to production data. Updated <i>Figure 1: "Internal schematic diagram"</i> . Updated <i>Section 1: "Electrical ratings"</i> , <i>Section 2: "Electrical characteristics"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Updated <i>Section 3: "Test circuits"</i> . Minor text changes.
25-Feb-2026	3	Updated <i>Section 4.1: TO-220 type A package information</i> . Minor text changes.

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