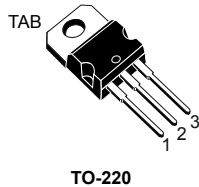
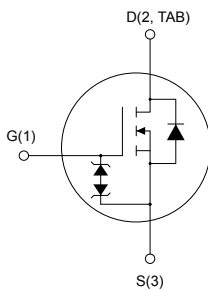


N-channel 620 V, 0.95 Ω typ., 5.5 A MDmesh K3 Power MOSFET in a TO-220 package



TO-220



AM01476v1_tab



Product status link

[STP6N62K3](#)

Product summary

Order code	STP6N62K3
Marking	6N62K3
Package	TO-220
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP6N62K3	620 V	1.2 Ω	5.5 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	620	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	5.5	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	3	
$I_{DM}^{(1)}$	Drain current (pulsed)	22	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	90	W
ESD	Gate-source human body model ($R=1.5\text{ k}\Omega$, $C=100\text{ pF}$)	2.5	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 5.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.39	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	5.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	140	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	620			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 620\text{ V}$			0.8	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 620\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			50	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 9	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.8\text{ A}$		0.95	1.2	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	875	-	pF
C_{oss}	Output capacitance		-	100	-	pF
C_{rss}	Reverse transfer capacitance		-	17	-	pF
$C_{oss(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	28	-	pF
$C_{oss(tr)}^{(2)}$	Equivalent output capacitance time related		-	63	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 496\text{ V}$, $I_D = 5.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	34	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain charge		-	22	-	nC

1. $C_{oss(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{oss(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$, $I_D = 2.75\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	22	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	49	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		27	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.5 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 5.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	290		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	1.9		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 5.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	335		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	2.4		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	14.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

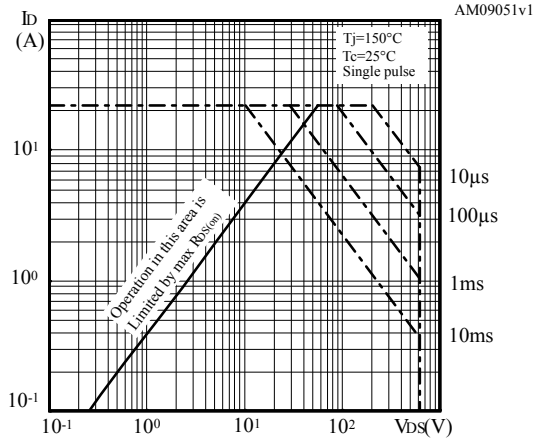


Figure 2. Normalized transient thermal impedance

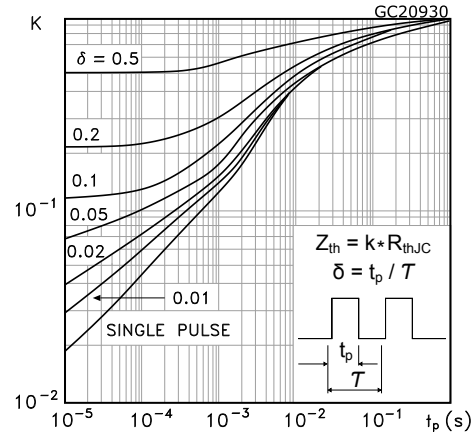


Figure 3. Typical output characteristics

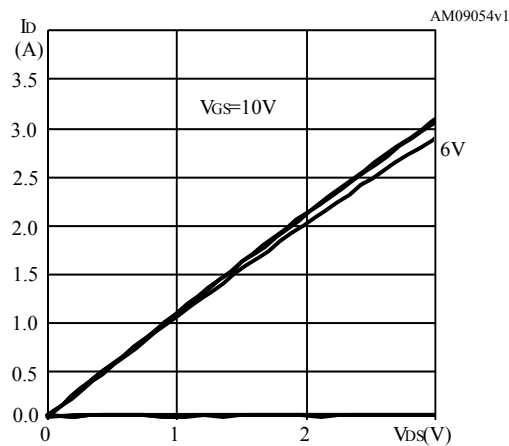


Figure 4. Typical transfer characteristics

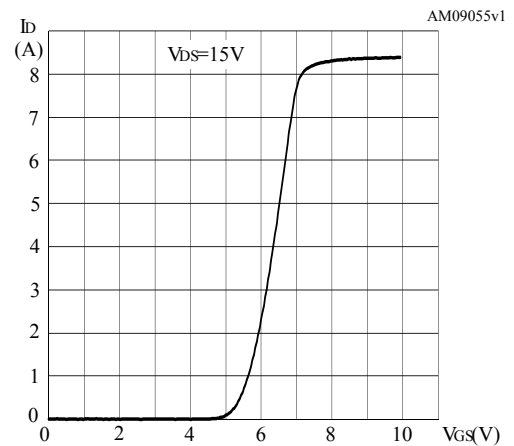


Figure 5. Typical gate charge characteristics

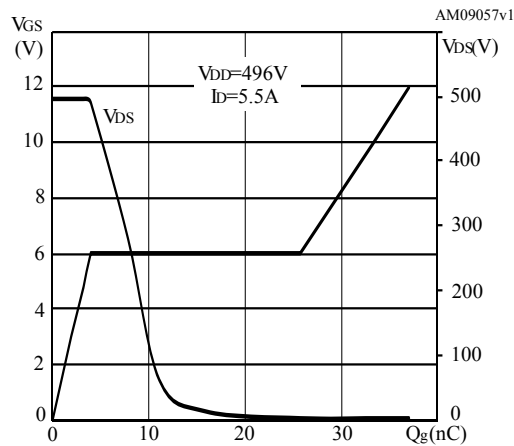


Figure 6. Typical capacitance characteristics

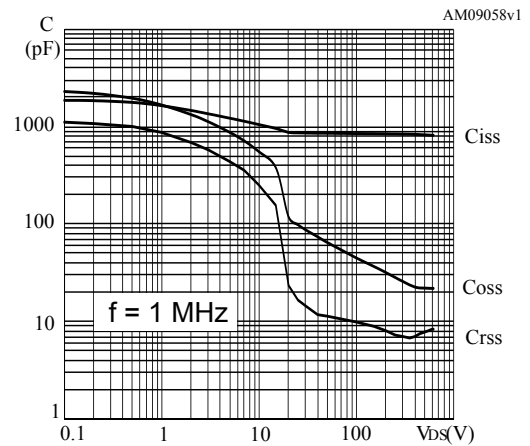


Figure 7. Normalized gate threshold vs temperature

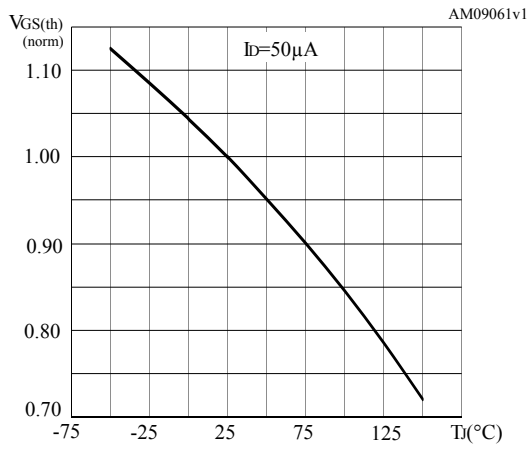


Figure 8. Normalized breakdown voltage vs temperature

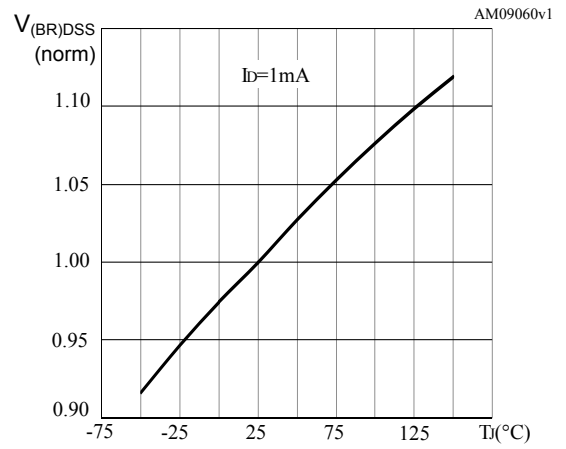


Figure 9. Typical drain-source on-resistance

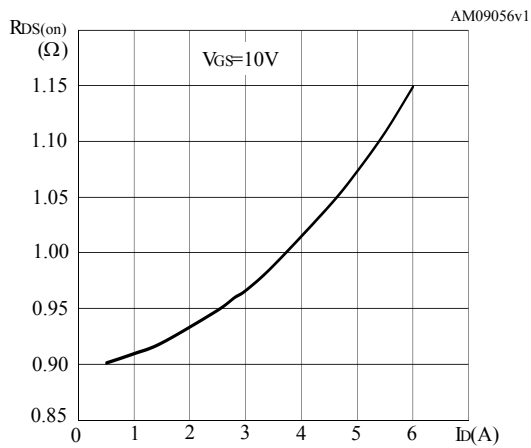


Figure 10. Normalized on-resistance vs temperature

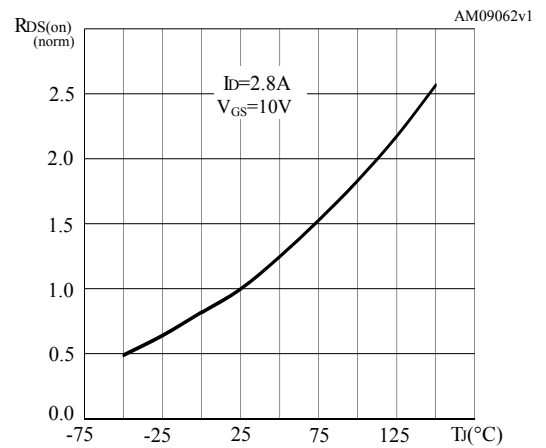


Figure 11. Typical output capacitance stored energy

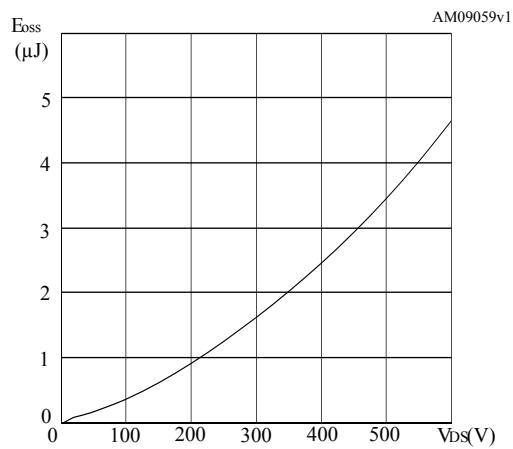


Figure 12. Typical reverse diode forward characteristics

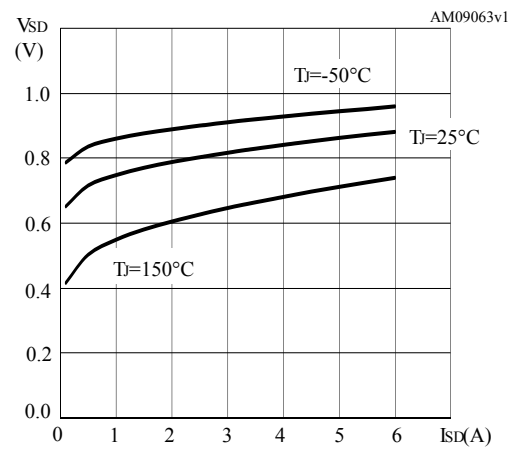
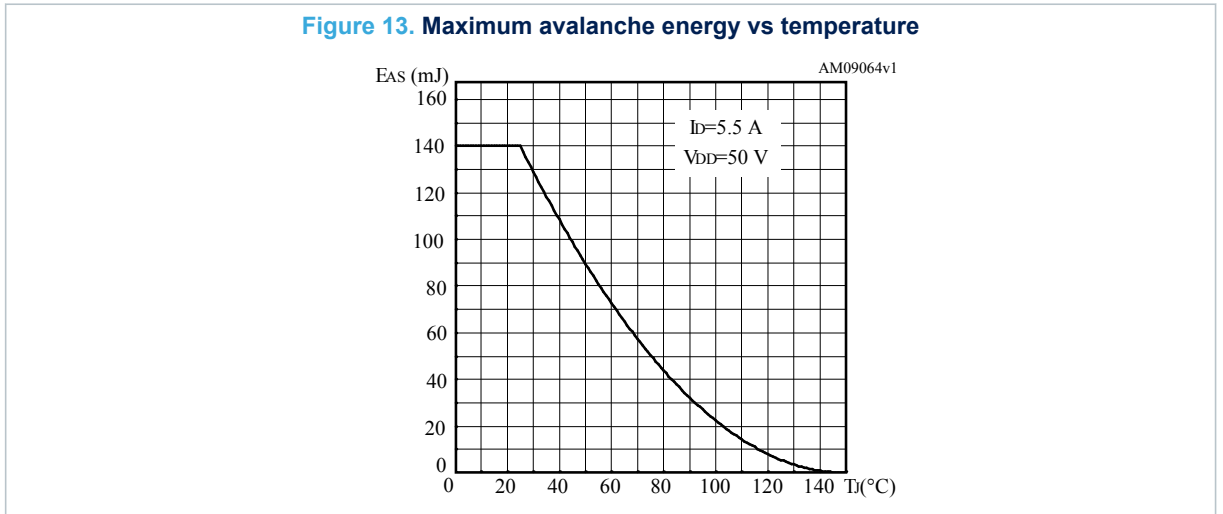
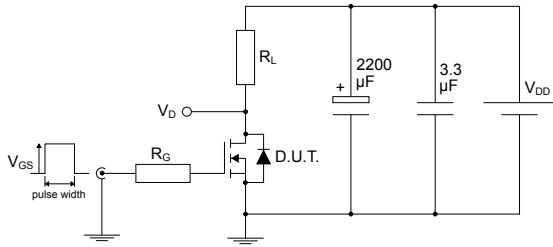


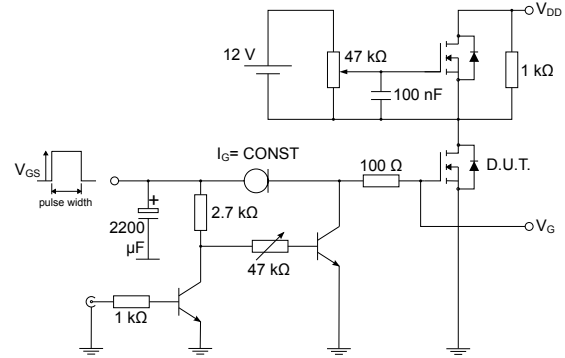
Figure 13. Maximum avalanche energy vs temperature



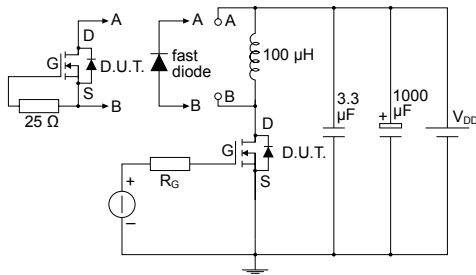
3 Test circuits

Figure 14. Test circuit for resistive load switching times


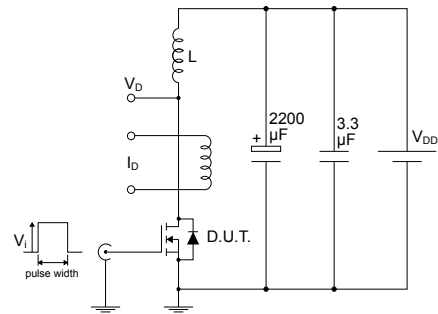
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Figure 15. Test circuit for gate charge behavior


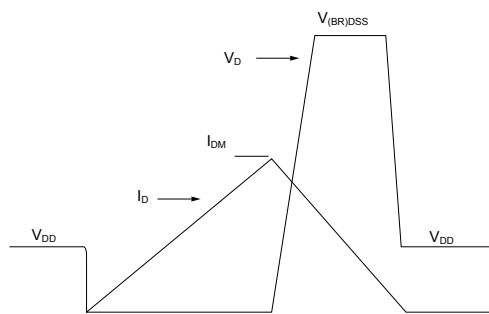
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Figure 16. Test circuit for inductive load switching and diode recovery times


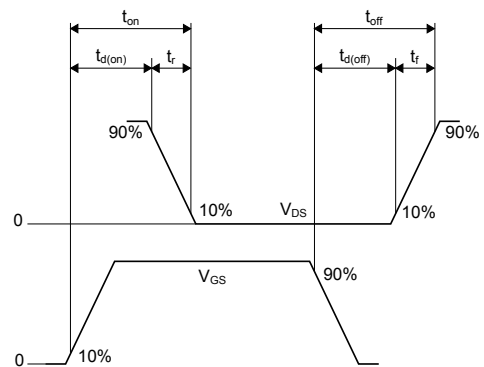
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


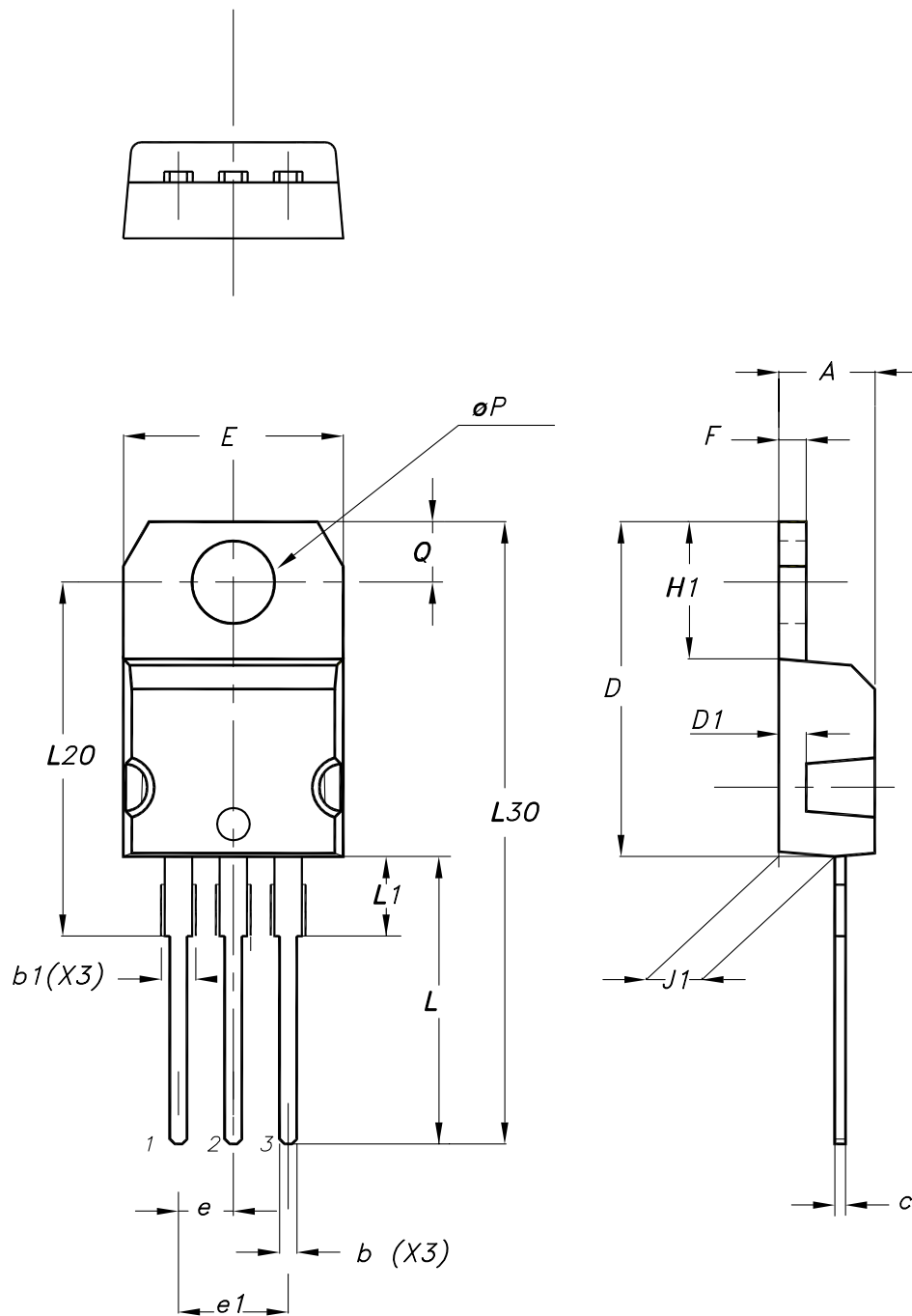
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 20. TO-220 type A package outline



0015988_typeA_Rev_23

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Oct-2023	1	First release. Part number STP6N62K3 previously included in datasheet DS5818.

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