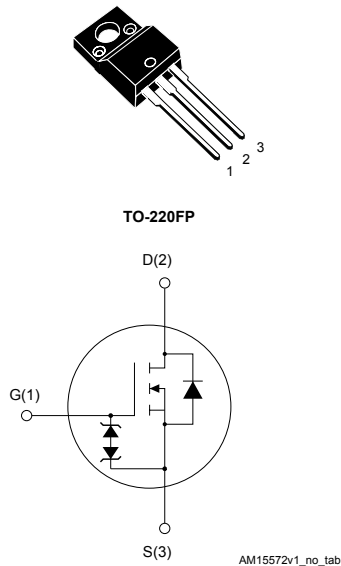


## N-channel 700 V, 1 $\Omega$ typ., 7.5 A SuperMESH Power MOSFET in a TO-220FP package



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP9NK70ZFP	700 V	1.2 $\Omega$	7.5 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.



#### Product status link

[STP9NK70ZFP](#)

#### Product summary

<b>Order code</b>	STP9NK70ZFP
<b>Marking</b>	P9NK70ZFP
<b>Package</b>	TO-220FP
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	700	V
$V_{GS}$	Gate-source voltage	±30	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	7.5	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	4.7	
$I_{DM}^{(1)}$	Drain current (pulsed)	30	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	35	W
ESD	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	4	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ °C}$ )	2.5	kV
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_J$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 7.5\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	3.6	°C/W
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	°C/W

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max.)	7.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	230	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	700	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 700\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 700\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$	-	-	50	
$I_{GSS}$	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4\text{ A}$	-	1	1.2	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1370	-	pF
$C_{oss}$	Output capacitance		-	143	-	pF
$C_{rss}$	Reverse transfer capacitance		-	32	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }560\text{ V}$	-	90	-	pF
$Q_g$	Total gate charge	$V_{DD} = 560\text{ V}$ , $I_D = 8\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	48	68 <sup>(2)</sup>	nC
$Q_{gs}$	Gate-source charge		-	10	-	nC
$Q_{gd}$	Gate-drain charge		-	27	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

2. Specified by design, not tested in production.

**Table 6. Switching times**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 350\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	22	-	ns
$t_r$	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	45	-	ns
$t_f$	Fall time		-	13	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	7.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	30	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7.5 \text{ A}, V_{GS} = 0 \text{ V}$	-	-	1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	570	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 25 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	5.2	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	19.5	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

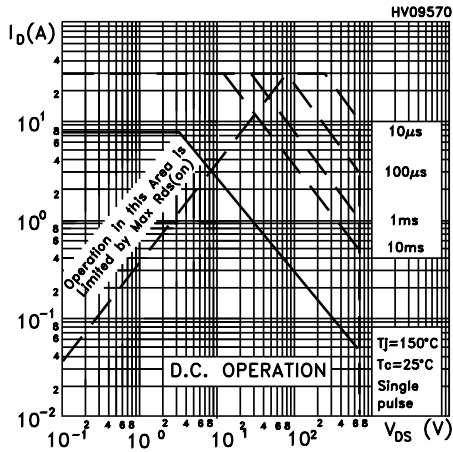


Figure 2. Normalized transient thermal impedance

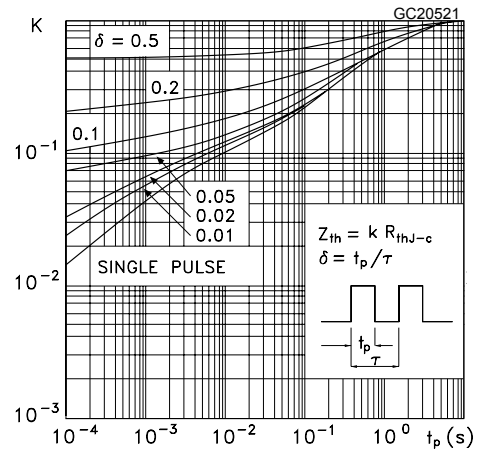


Figure 3. Typical output characteristics

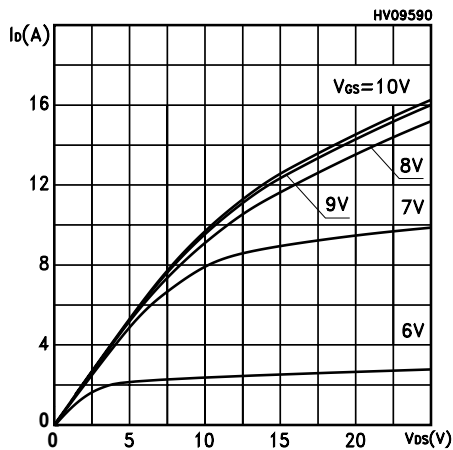


Figure 4. Typical transfer characteristics

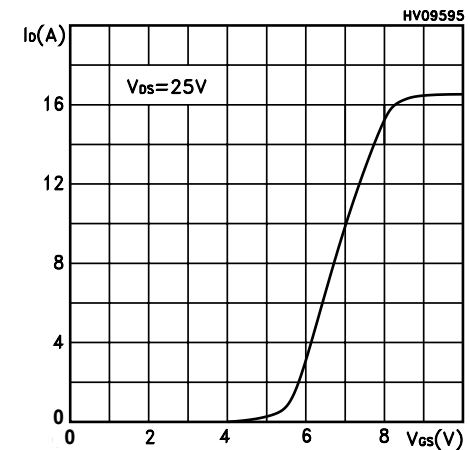


Figure 5. Typical gate charge characteristics

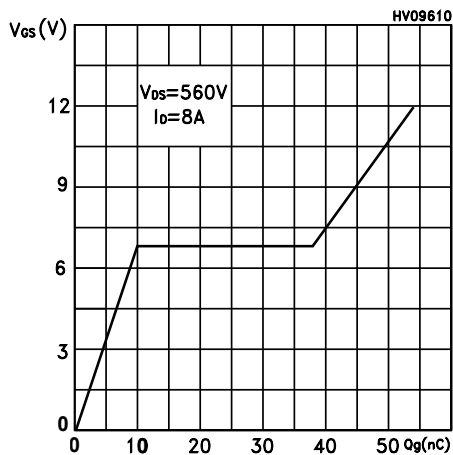


Figure 6. Typical drain-source on-resistance

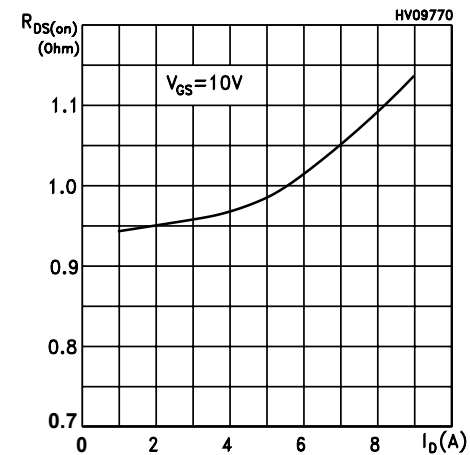


Figure 7. Typical capacitance characteristics

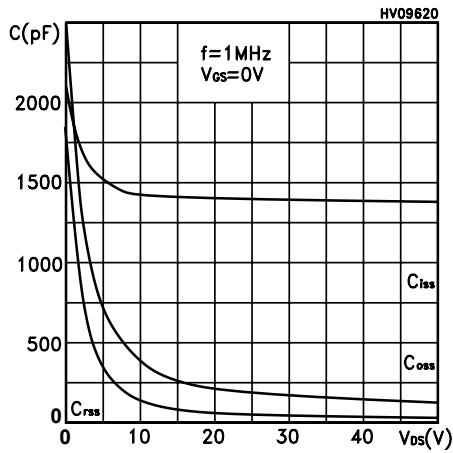


Figure 8. Normalized gate threshold vs temperature

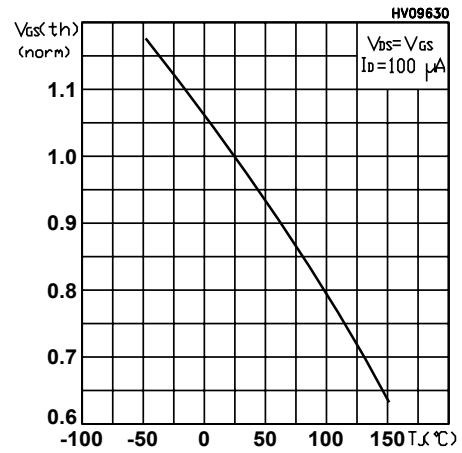


Figure 9. Normalized on-resistance vs temperature

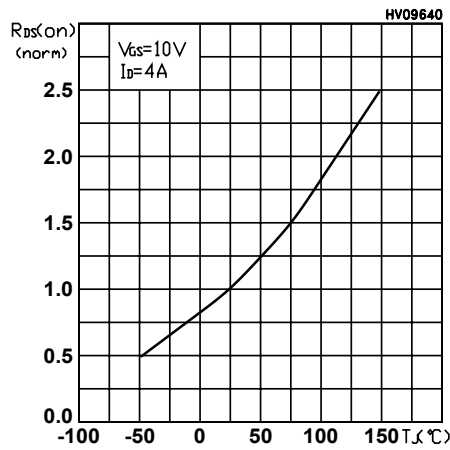


Figure 10. Normalized breakdown voltage vs temperature

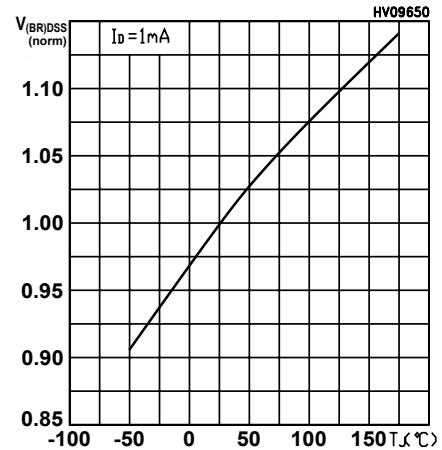


Figure 11. Maximum avalanche energy vs temperature

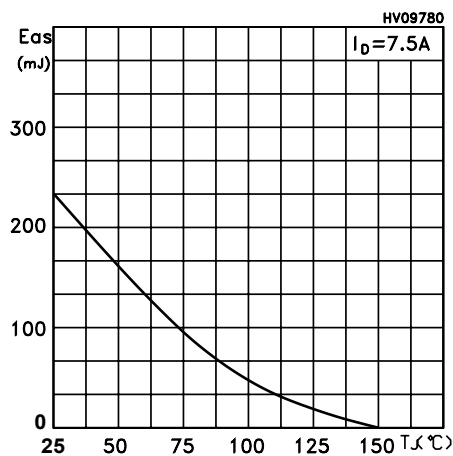
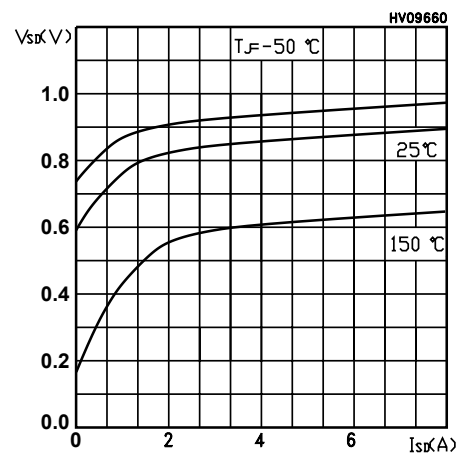
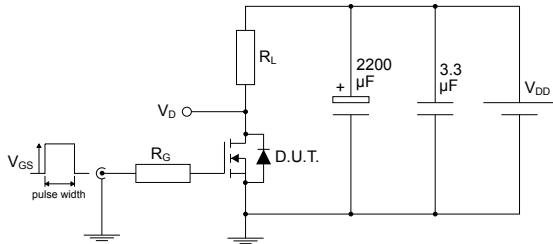


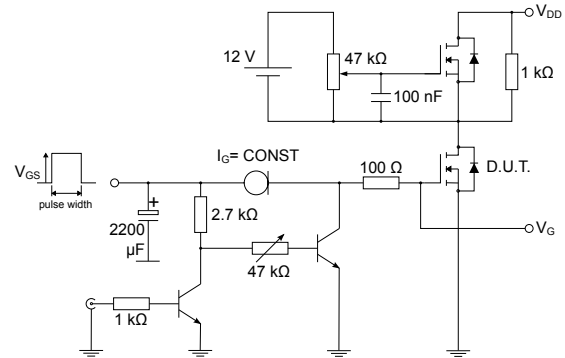
Figure 12. Typical reverse diode forward characteristics



### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


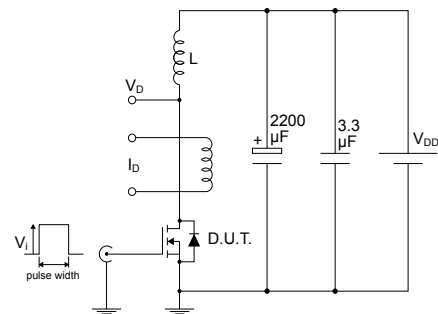
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


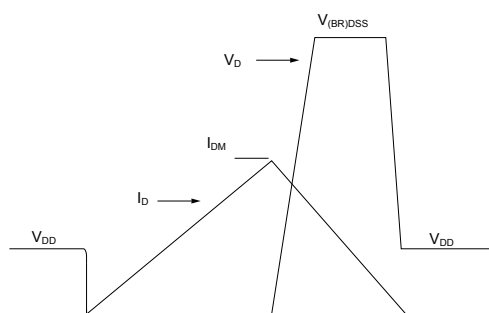
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**Figure 15. Test circuit for inductive load switching and diode recovery times**

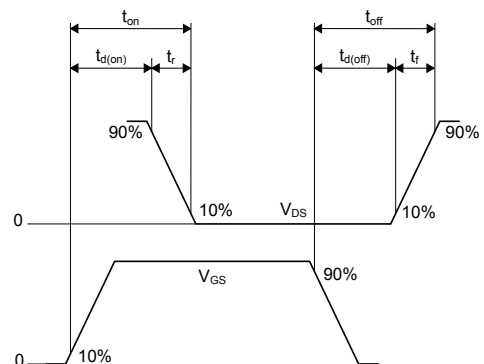

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**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


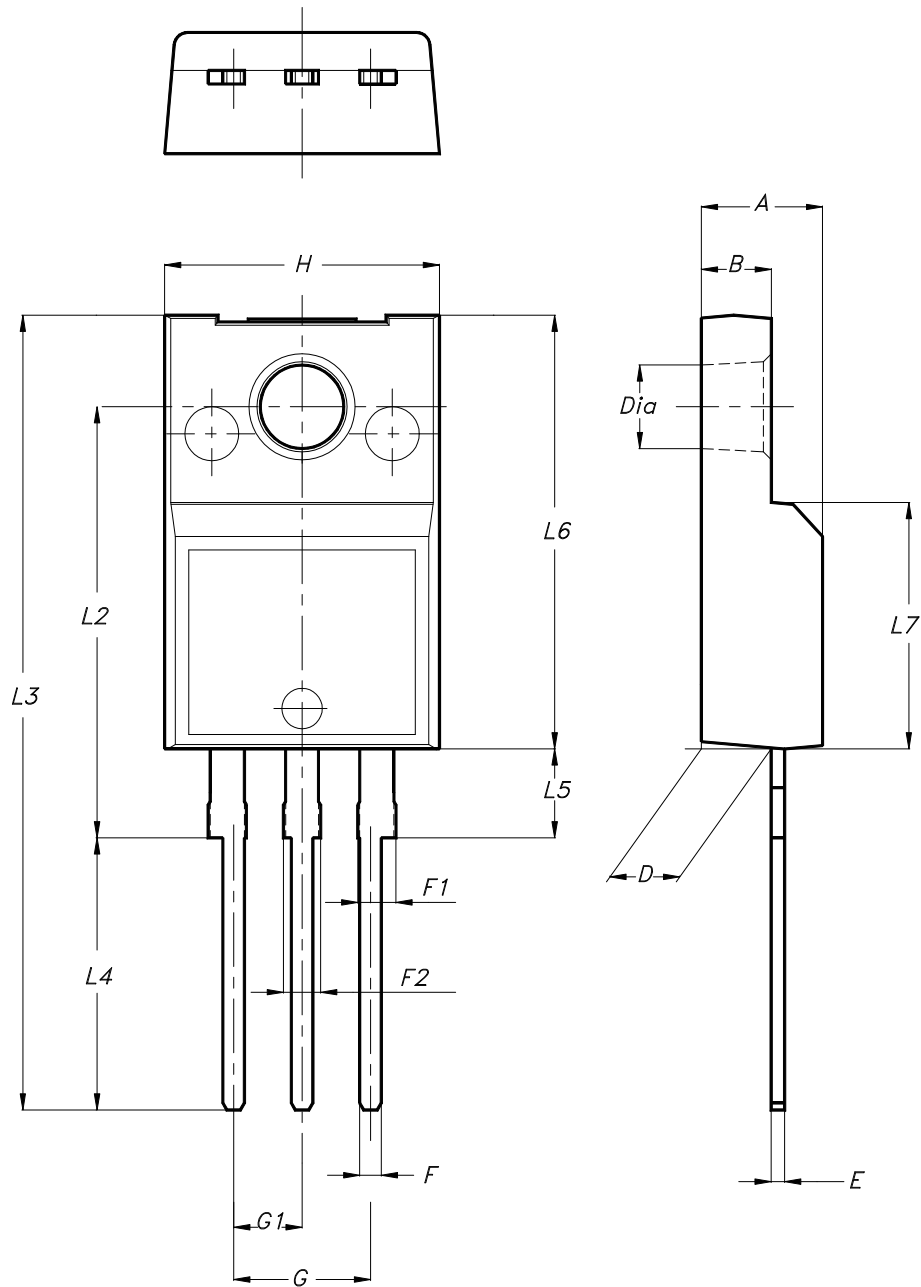
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220FP type B package information

Figure 19. TO-220FP type B package outline



7012510\_B\_rev.14

**Table 8. TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
11-Feb-2026	3	Removed order code STB9NK70Z, STB9NK70Z-1, STP9NK70Z and STW9NK70Z. Updated Section 4: Package information. Minor text changes.

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## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	<b>Electrical characteristics (curves)</b> .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>7</b>
<b>4</b>	<b>Package information</b> .....	<b>8</b>
<b>4.1</b>	<b>TO-220FP type B package information</b> .....	<b>8</b>
	<b>Revision history</b> .....	<b>10</b>

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