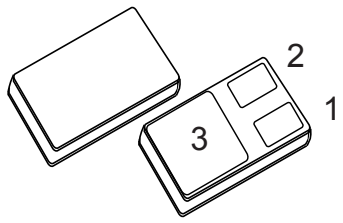
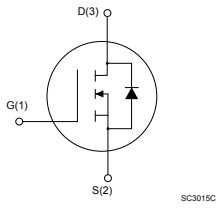
STRH40N6

Datasheet

Rad-Hard 60 V, 30 A, N-channel Power MOSFET



SMD.5



Product status link
STRH40N6

Features

V_{DS}	I_D	$R_{DS(on)}$ typ.	Q_g
60 V	30 A	36 mΩ	43 nC

- Fast switching
- 100 % avalanche tested
- Hermetic package
- 50 krad TID
- SEE radiation hardened

Description

The STRH40N6 is a N-channel Power MOSFET able to operate under severe environment conditions and radiation exposure. It provides high reliability performance and immunity to the total ionizing dose (TID) and single event effects (SEE).

Qualified as per ESCC detail specification No. 5205/024 and available in SMD.5 hermetic package it is specifically recommended for space and harsh environment applications and suitable for in-Satellite power conversion, motor control and power switch circuits.

In case of discrepancies between this datasheet and the relevant agency specification, the latter takes precedence.

Product summary

Product summary					
Part numbers	Quality level	ESCC Part number	Package	Lead finish	Radiation level
STRH40N6S1	Engineering model	5205/024	SMD.5	Gold	-
STRH40N6SG	ESCC flight				50 krad
STRH40N6ST				Solder-dip	

Note: See Table 8 for ordering information.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}(1)	Drain-source voltage (V_{GS} = 0)	60	V
V_{GS}(2)	Gate-source voltage	±20	V
I_D	Drain current (continuous)	30	A
	Drain current (continuous) at T_{amb} = 100 °C	19	A
I_{DM}(3)	Drain current (pulsed)	120	A
P_{TOT}	Total dissipation at T_C = 25 °C	75	W
P_{TOT}	Total dissipation at T_a = 25 °C	2.5	W
dv/dt(4)	Peak diode recovery voltage slope	2.5	V/ns
T_{op}	Operating temperature range	-55 to 150	°C
T_j	Max. operating junction temperature range	150	°C

1. *This rating is guaranteed at $T_J \geq 25$ °C (see Figure 9).*
2. *This value is guaranteed over the full range of temperature.*
3. *Pulse width limited by safe operating area.*
4. *$I_{SD} \leq 40$ A, di/dt ≤ 1060 A/µs, $V_{DD} = 80\ \% V_{(BR)DSS}$*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.67	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

2 Avalanche data

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max.)	15	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = 20 A, V_{DD} = 40 V)	354	mJ
E_{AS}	Single pulse avalanche energy (starting T_j = 110 °C, I_D = 20 A, V_{DD} = 40 V)	105	
E_{AR}	Repetitive avalanche (V_{DD} = 50 V, I_{AR} = 17.5 A, f = 10 KHz, T_J = 25 °C, duty cycle = 50 %)	20	mJ
	Repetitive avalanche (V_{DD} = 40 V, I_{AR} = 15 A, f = 100 KHz, T_J = 25 °C, duty cycle = 10 %)	1.3	
	Repetitive avalanche (V_{DD} = 40 V, I_{AR} = 15 A, f = 100 KHz, T_J = 110 °C, duty cycle = 10 %)	0.4	

1. *Maximum rating value.*

3 Electrical characteristics

Table 4. Electrical characteristics (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80 % $V_{(BR)DSS}$		10	µA
		80 % $V_{(BR)DSS}$, T_C = 125 °C		100	µA
I_{GSS}	Gate body leakage current, (V_{DS} = 0)	V_{GS} = 20 V		100	nA
		V_{GS} = -20 V	-100		
		V_{GS} = -20 V, T_C = 125 °C		200	
		V_{GS} = 20 V, T_C = 125 °C	-200		
$V_{(BR)DSS}$(1)	Drain-to-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	60		V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	2	4.5	V
		V_{DS} = V_{GS}, I_D = 1 mA, T_C = 125 °C	1.5	3.7	
		V_{DS} = V_{GS}, I_D = 1 mA, T_C = -55 °C	2.1	5.5	
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 12 V, I_D = 15 A		0.045	Ω
		V_{GS} = 12 V, I_D = 15 A, T_a = 125 °C		0.076	
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	1312	1968	pF
C_{oss} (2)	Output capacitance		281	421	pF
C_{rss}	Reverse transfer capacitance		111	167	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 40 A, V_{GS} = 12 V	35	52	nC
Q_{gs}	Gate-to-source charge		9	13	nC
Q_{gd}	Gate-to-drain (“Miller”) charge		12	18	nC
R_G(2)	Gate input resistance	f = 1 MHz gate DC bia s= 0, test signal level = 20 mV open drain	1.04	1.56	Ω
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 12 V	13	21	ns
t_r	Rise time		26	92	
$t_{d(off)}$	Turn-off delay time		18	48	
t_f	Fall time		7	16	
I_{SD}	Source-drain current			30	A
I_{SDM}(3)	Source-drain current (pulsed)			120	A
V_{SD}(4)	Diode forward voltage	I_{SD} = 30 A, V_{GS} = 0 V		1.5	V
		I_{SD} = 30 A, V_{GS} = 0 V, T_a = 125 °C		1.275	
t_{rr}(2)	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD}= 48 V, T_j = 25 °C	288	432	
t_{rr}(2)	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD}= 48 V, T_j = 150 °C	352	529	

1. *This rating is guaranteed at T_J ≥ 25 °C (see Figure 9. Normalized $V_{(BR)DSS}$ vs temperature).*
2. *Not tested in production, garanteed by process.*
3. *Pulse width limited by safe operating area.*
4. *Pulsed: pulse duration = 300 µs, duty cycle ≤ 1.5%*

4 Radiation characteristics

This products is guaranteed in radiation as per ESCC 5205/024 and ESCC 22900 specification at 50 krad. Each lot tested in radiation is accepted according to the characteristics as per Table 5.

4.1 Total dose radiation (TID) testing

The bias with V_{GS} = + 15 V and V_{DS} = 0 V is applied during irradiation exposure.

The parameters listed in Table 5 are measured:

- Before irradiation
- After irradiation
- After 24 hrs at room temperature
- after 168 hrs at 100 °C anneal

Table 5. Post-irradiation electrical characteristics (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Drift values Δ	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80 % $V_{(BR)DSS}$	+20	µA
I_{GSS}	Gate body leakage current, (V_{DS} = 0)	V_{GS} = 20 V	1.5	nA
		V_{GS} = -20 V	-1.5	
$V_{(BR)DSS}$	Drain-to-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	-20%	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	-60% / +20%	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 20 A	±10%	Ω
V_{SD}	Diode forward voltage	I_{SD} = 40 A, V_{GS} = 0 V	±5%	V

1. *Pulsed: pulse duration = 300 µs, duty cycle ≤ 1.5%*

4.2 Single event effect RBSOA

The STRH40N6 is extremely resistant to heavy ions exposure as per MIL-STD-750E, test method 1080, bias circuit of Figure 2.

SEB and SEGR tests are performed with a fluence of 3e+5 ions/cm² with the following acceptance criteria:

- SEB test: drain voltage checked, trigger level is set to VDS = - 5 V. Stop condition: as soon as a SEB occurs or if the fluence reaches 3e+5 ions/cm².
- SEGR test: the gate current is monitored every 200 ms. A gate stress is performed before and after irradiation. Stop condition: as soon as the gate current reaches 100 nA (during irradiation or during PIGS test) or if the fluence reaches 3e+5 ions/cm².

Table 6. Single event effect (SEE), reverse biased safe operating area (RBSOA)

Ion	Let (Mev/(mg/cm^2))	Energy (MeV)	Range (µm)
Kr	32	768	94
Br	38	300	38
I	61	330	31

Figure 1. Single event effect, RBSOA

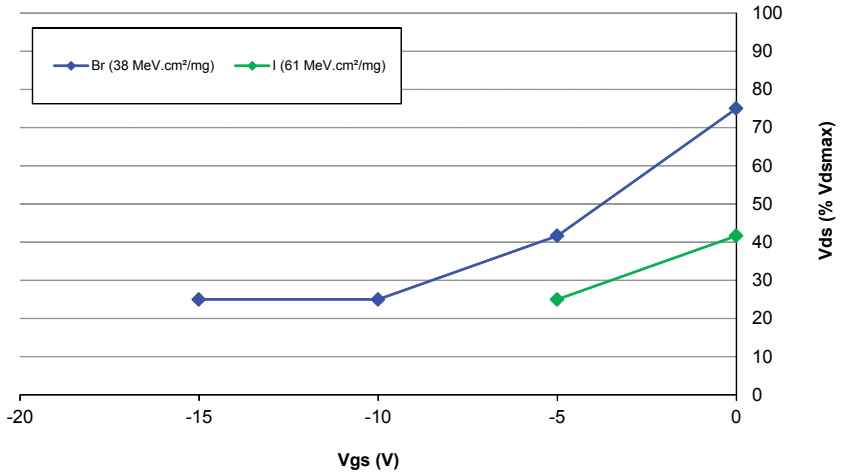
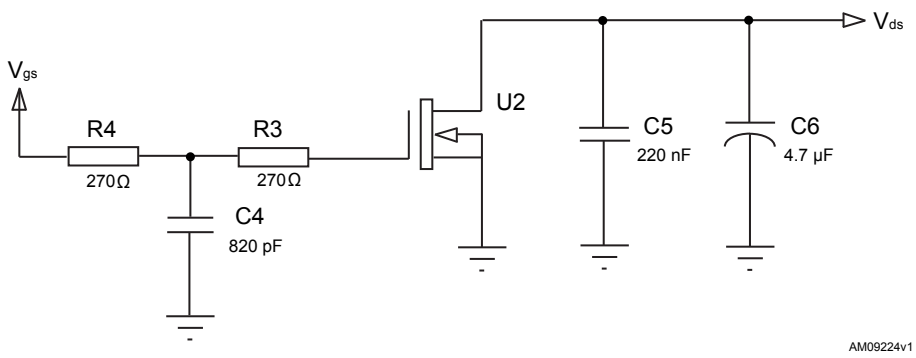


Figure 2. Single event effect, bias circuit



5 Electrical characteristics (curves)

Figure 3. Safe operating area

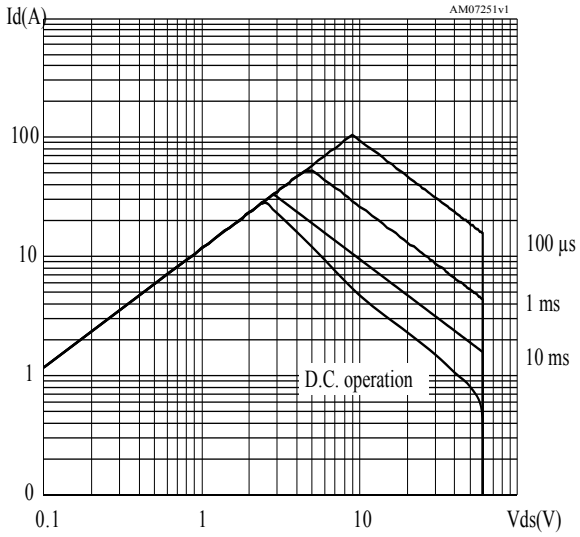


Figure 4. Thermal impedance

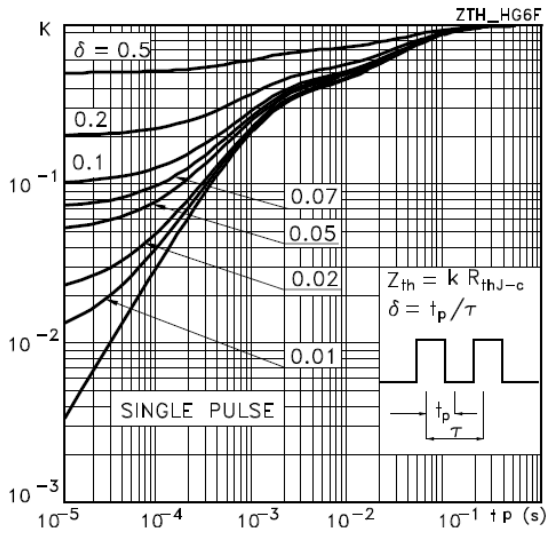


Figure 5. Output characteristics

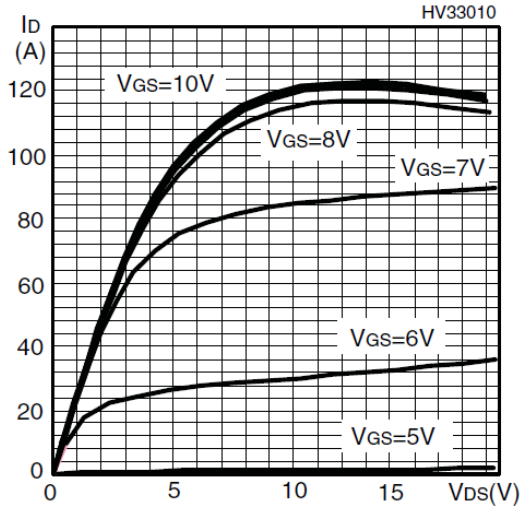


Figure 6. Transfer characteristics

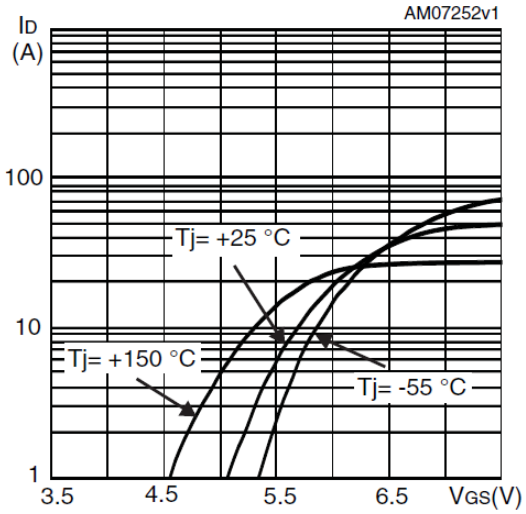


Figure 7. Gate charge vs gate-source voltage

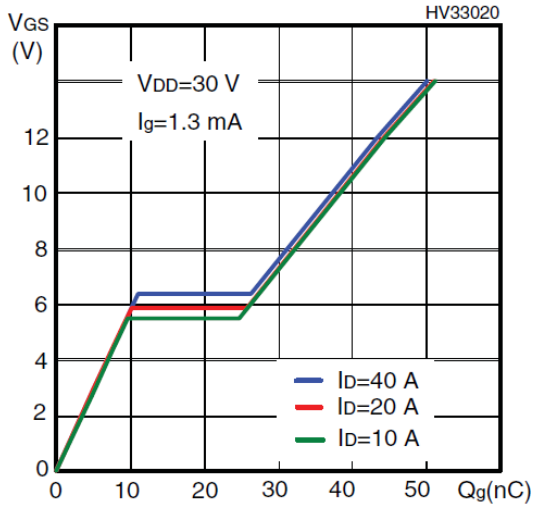


Figure 8. Capacitance variations

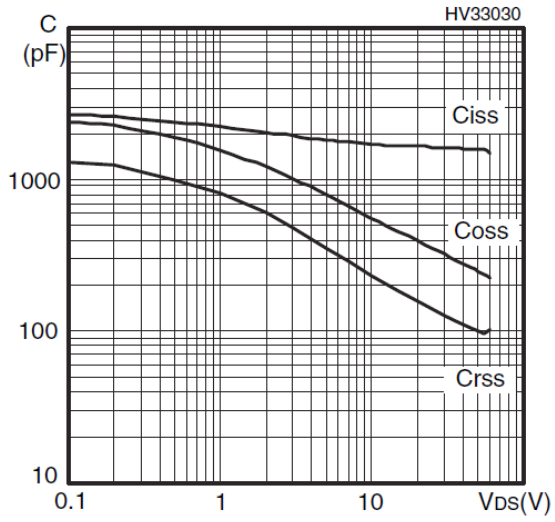


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

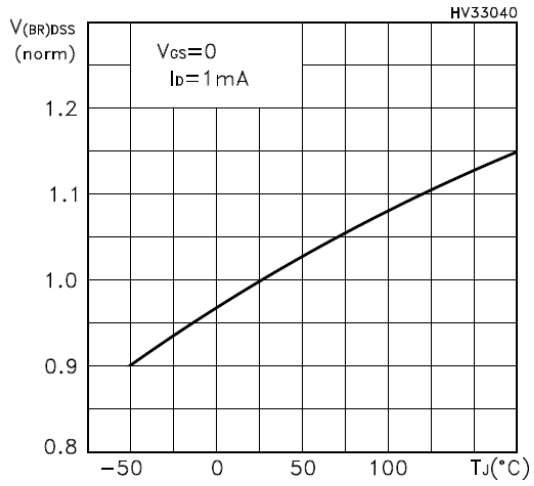


Figure 10. Static drain-source on-resistance

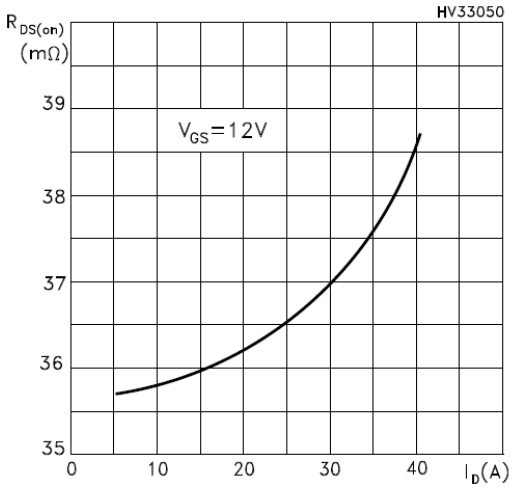


Figure 11. Normalized gate threshold voltage vs temperature

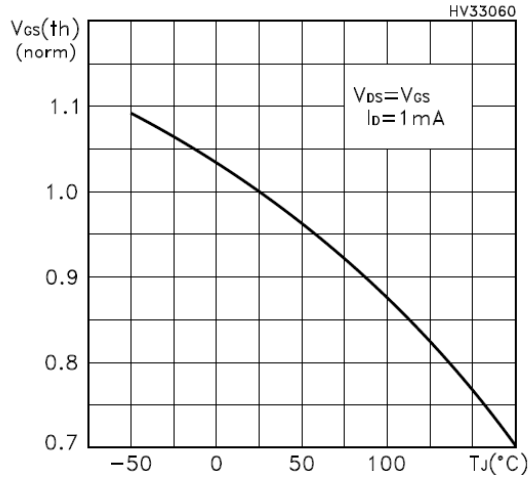


Figure 12. Normalized on-resistance vs temperature

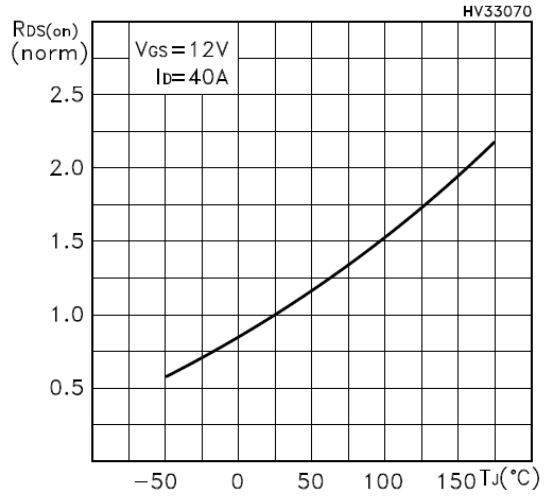
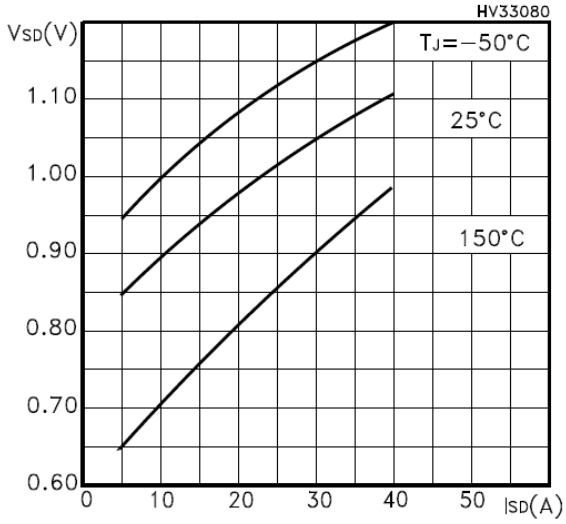
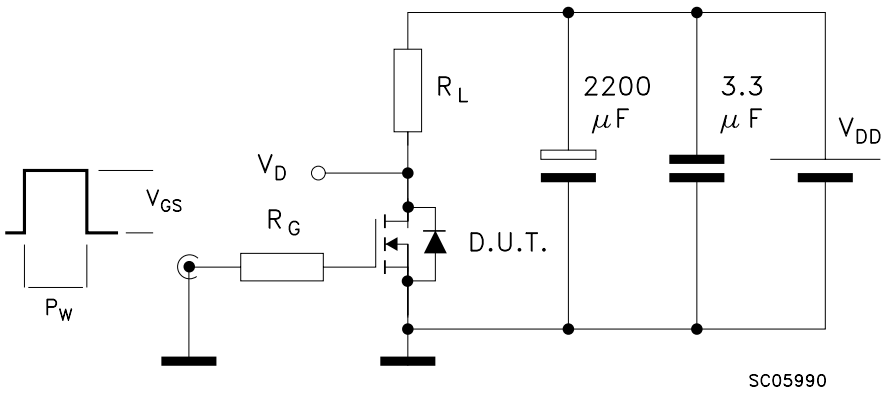


Figure 13. Source drain-diode forward characteristics



6 Test circuits

Figure 14. **Switching times test circuit for resistive load**



Note: Max driver V_{GS} slope = 1 V/ns (no DUT)

Figure 15. **Source drain diode waveform**

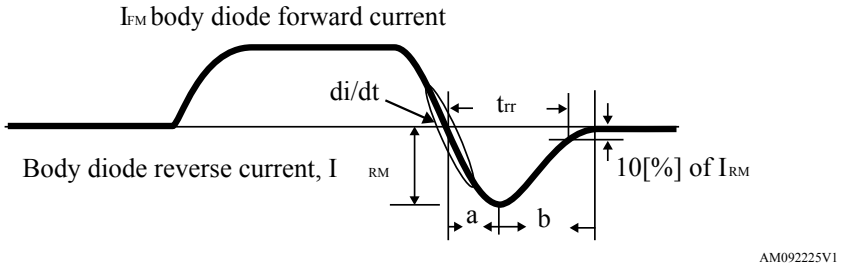
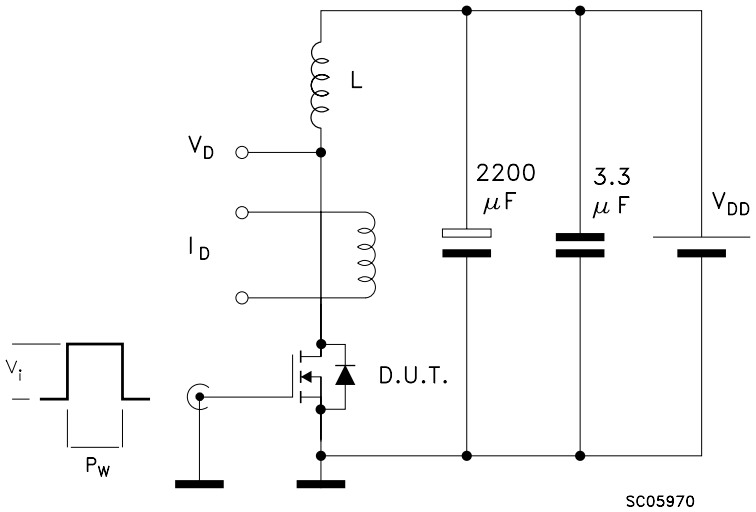


Figure 16. **Unclamped inductive load test circuit (single pulse and repetitive)**



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SMD.5 package information

Figure 17. SMD.5 package outline

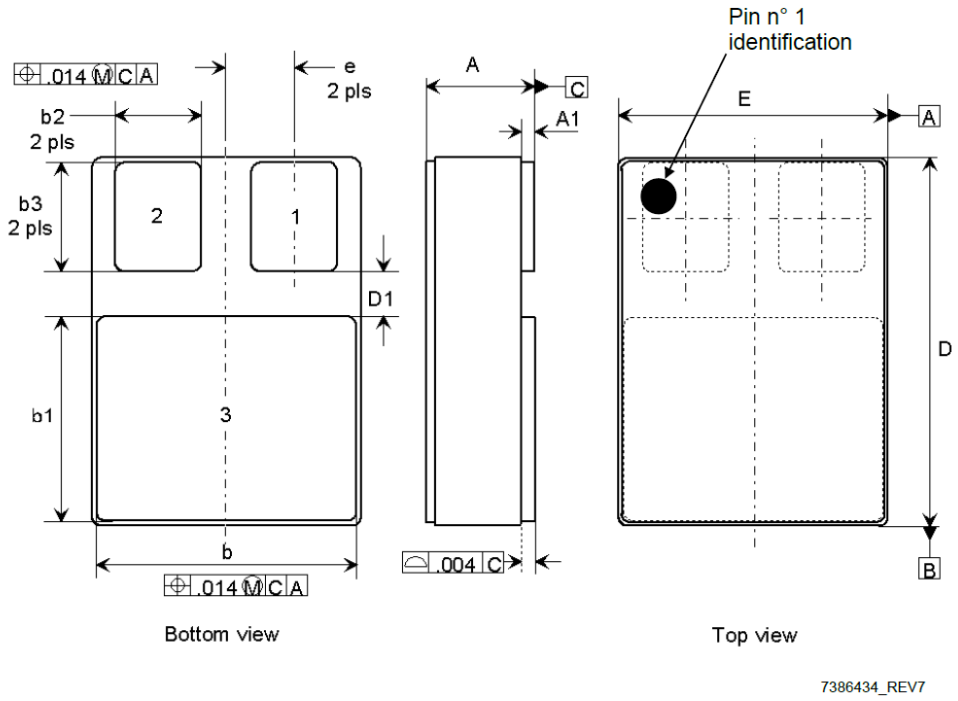


Table 7. SMD.5 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.84		3.30
A1	0.25	0.38	0.51
b	7.13	7.26	7.39
b1	5.58	5.72	5.84
b2	2.28	2.41	2.54
b3	2.92	3.05	3.18
D	10.03	10.16	10.28
D1	0.76		
E	7.39	7.52	7.64
e		1.91	

Note: The lid is not connected to any pin.

8 Order codes

Table 8. **Ordering information**

Part number	Agency specification	Quality level	Radiation level	Package	Weight	Lead finish	Marking[1]	Packing
STRH40N6S1	-	Engineering model	-	SMD.5	1 g	Gold	STRH40N6S1	Strip pack
STRH40N6SG	5205/024/01	ESCC flight	50 krad				520502401F	
STRH40N6ST	5205/024/02					Solder-dip	520502402F	

1. *Specific marking only. The full marking includes in addition: For the Engineering Models: ST logo, date code; country of origin (FR). For ESCC flight parts: STlogo, date code, country of origin (FR), ESA logo, serial number of the part within the assembly lot.*

Contact ST sales office for information about specific conditions for products in die form.

9 Other information

9.1 Traceability information

Date code information is described in the table below.

Table 9. Date codes

Model	Date code[1]
EM	3yywwN
Flight	yywwN

1. *yy = year, ww = week number, N = lot index in the week.*

9.2 Documentation

Table 10. Documentation provided for each type of product

Quality level	Radiation level	Documentation
Engineering model	-	Certificate of conformance
Flight	50 krad	Certificate of conformance ESCC qualification maintenance lot reference Radiation data at 25 / 50 krad at 0.1 rad / s.

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
03-Jan-2011	1	First release.
25-Aug-2011	2	Updated order codes in Table 1: Device summary and Table 14: Ordering information. Minor text changes.
09-Nov-2011	3	Updated dynamic values on Table 7: Pre-irradiation switching times. Document status changed from preliminary data to datasheet.
28-Mar-2012	4	Updated title in cover page.
03-Oct-2012	5	Figure 4: Safe operating area has been modified.
01-Jul-2013	6	Updated order codes in Table 1: Device summary, Table 12: Single event effect (SEE), safe operating area (SOA), Figure 2: Single event effect, SOA and Table 14: Ordering information. Added Section 7.1: Other information. Minor text changes.
09-Sep-2013	7	Updated features in cover page.
14-May-2014	8	Updated Table 5: Pre-irradiation on/off states.
19-May-2014	9	Updated Table 9: Post-irradiation on/off states @ TJ= 25 °C, (Co60 g rays 50 K Rad(Si)).
04-Mar-2016	10	Updated: Features, Table 5, Table 8,Table 9,Table 10, Table 11 and Table 15. Updated Section 6: Package information. Minor text changes.
15-Jun-2021	11	Updated SMD.5 package information. Minor text changes.
07-Jul-2021	12	Updated ESCC detail specification No. from 5205/021 to 5205/024.
04-Oct-2021	13	Updated Table 8 and Table 10.