

N-channel 30 V, 0.019 Ω typ., 8 A, P-channel 30 V, 0.024 Ω typ., 6 A
STripFET™ Power MOSFET in a SO-8 package

Datasheet - preliminary data

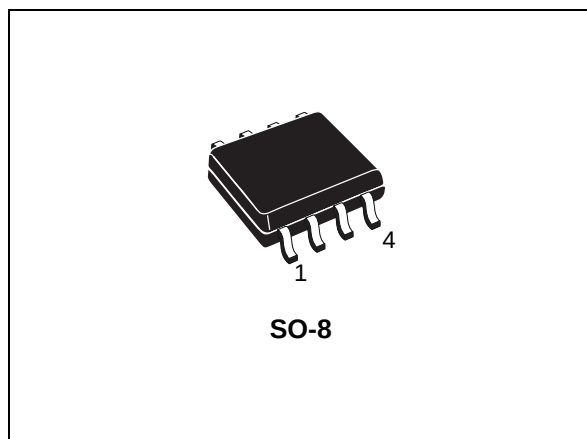
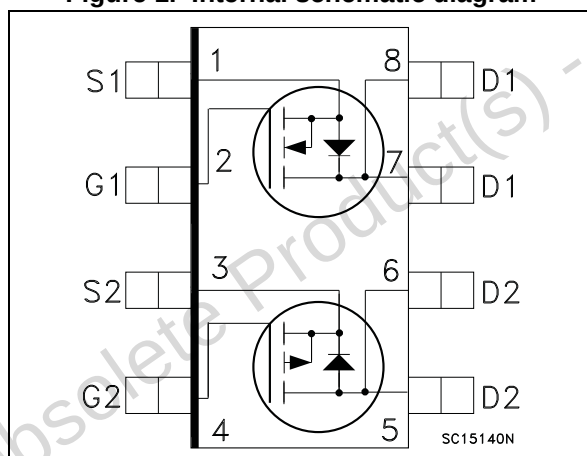


Figure 1. Internal schematic diagram



Features

Order code	Channel	V _{DS}	R _{DS(on)} max	I _D
STS8C6H3LL	N	30 V	0.021 Ω	8 A
	P		0.030 Ω	5 A

- STripFET™V N-channel Power MOSFET
- STripFET™VI DeepGATE™ P-channel Power MOSFET
- R_{DS(on)}* Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a complementary pair transistor. The P-channel Power MOSFET is developed using STripFET™VI DeepGATE™ and the N-channel using the STripFET™ V technology. The resulting device exhibits low on-state resistance and an FOM among the lowest in its voltage class.

Table 1. Device summary

Order code	Marking	Package	Packaging
STS8C6H3LL	86DK3L	SO-8	Tape and reel

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		N-channel	P-channel	
V_{DS}	Drain-source voltage ($v_{gs} = 0$)	30		V
V_{GS}	Gate- source voltage	± 20		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$ single operating	8	6	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$ single operating	5	3.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	24	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.7		W
T_{stg}	Storage temperature	-55 to 150		$^\circ\text{C}$
T_j	Operating junction temperature	150		$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient single operation	47	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10$ sec

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	N P	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30\text{ V}$	N			1	μA
			P				
		$V_{DS}=30\text{ V}$, $T_C=125\text{ °C}$	N			10	μA
			P				
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$	N			± 100	nA
			P				
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	N	1			V
			P				
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$	N		0.019	0.021	Ω
			P		0.024	0.030	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 3\text{ A}$	N		0.023	0.028	Ω
			P		0.038	0.050	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 24\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	N	-	475	-	pF
			P	-	1450	-	pF
C_{oss}	Output capacitance		N	-	97	-	pF
			P	-	178	-	pF
C_{rss}	Reverse transfer capacitance		N	-	19	-	pF
			P	-	120	-	pF
Q_g	Total gate charge		N	-	4.6	-	nC
			P	-	12	-	nC
Q_{gs}	Gate-source charge		N	-	1.7	-	nC
			P	-	4.4	-	nC
Q_{gd}	Gate-drain charge		N	-	1.9	-	nC
			P	-	5	-	nC

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

Table 6. Switching times

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 24\text{ V}$, $I_D = 3\text{ A}$ $R_G=4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ <i>Figure 24</i>	N	-	4	-	ns
			P	-	15	-	ns
t_r	Rise time		N	-	22	-	ns
			P	-	15	-	ns
$t_{d(off)}$	Turn-off delay time		N	-	13	-	ns
			P	-	24	-	ns
t_f	Fall time		N	-	2.8	-	ns
			P	-	21	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit	
I_{SD}	Source-drain current		N	-		8	A	
			P	-		6	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		N	-		32	A	
			P	-		24	A	
$V_{SD}^{(2)}$	Forward on voltage		$I_{SD} = 6A, V_{GS} = 0$	N	-	1.1	V	
				P	-			
t_{rr}	Reverse recovery time		$I_{SD} = 5\text{ A}, di/dt = 100\text{ A}/\mu s$ $V_{DD} = 16\text{ V}, T_j = 150\text{ }^{\circ}\text{C}$ <i>Figure 26</i>	N	-	16.2		ns
				P	-	15		ns
Q_{rr}	Reverse recovery charge			N	-	8.1		nC
				P	-	6.5		nC
I_{RRM}	Reverse recovery current			N	-	1		A
				P	-	0.9		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

2.1 Electrical characteristics (curves) for N-channel

Figure 2. Safe operating area

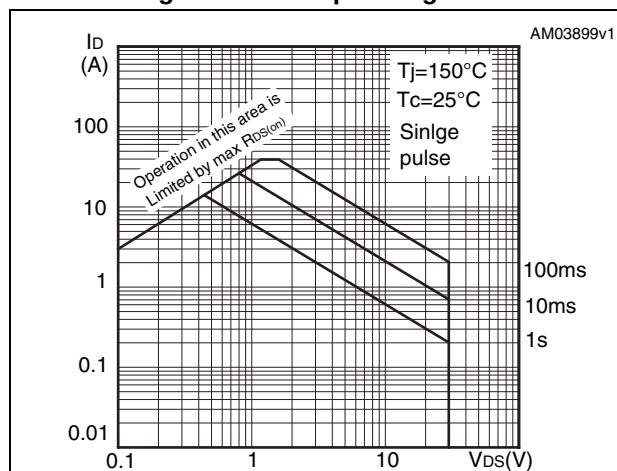


Figure 3. Thermal impedance

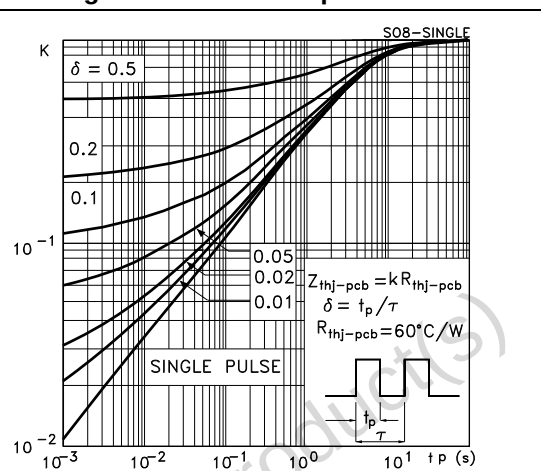


Figure 4. Output characteristics

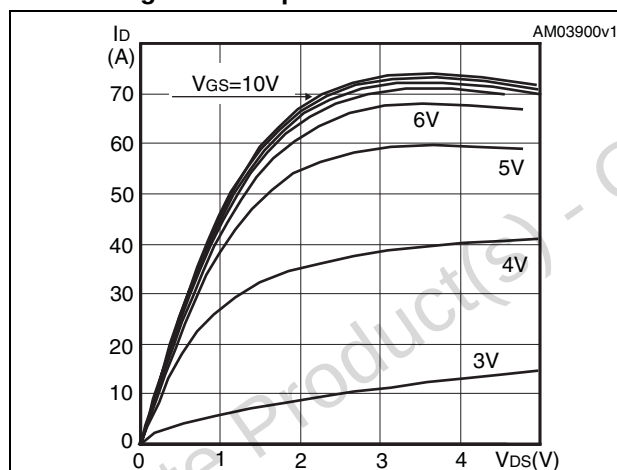


Figure 5. Transfer characteristics

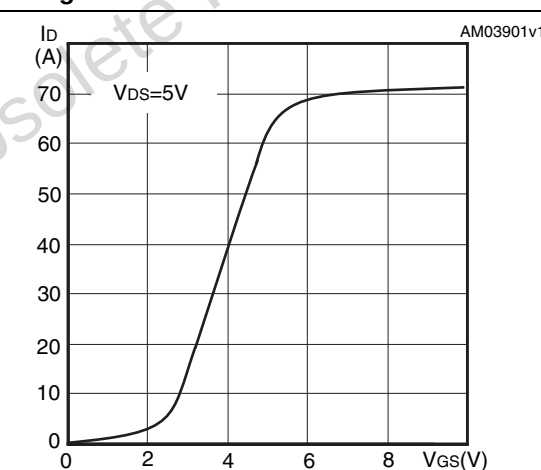
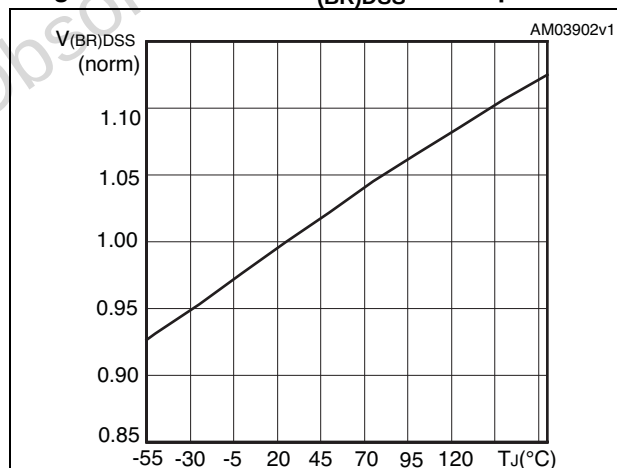
Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

Figure 7. Static drain-source on-resistance

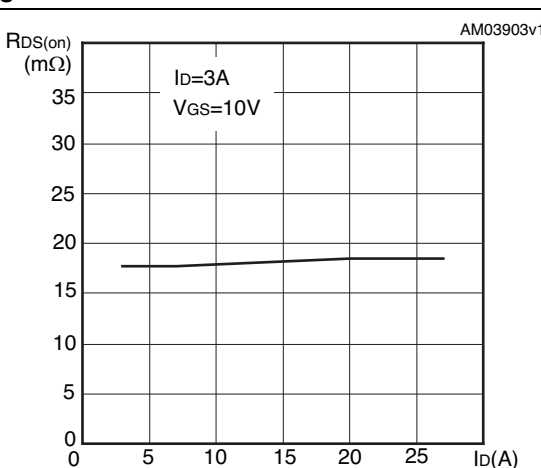


Figure 8. Gate charge vs gate-source voltage

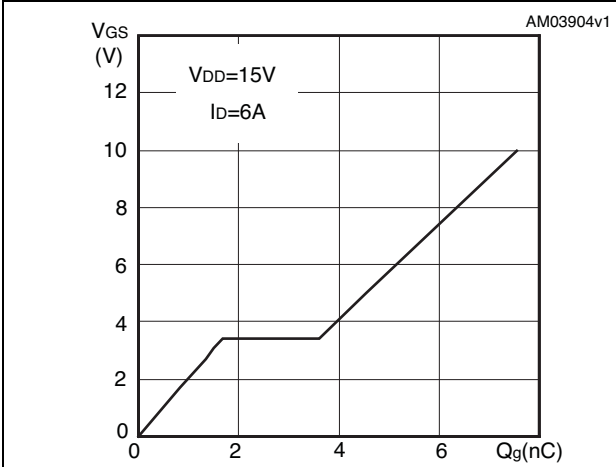


Figure 9. Capacitance variations

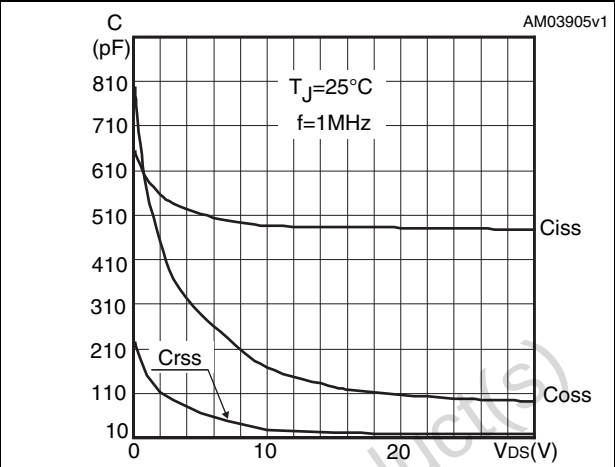


Figure 10. Normalized gate threshold voltage vs temperature

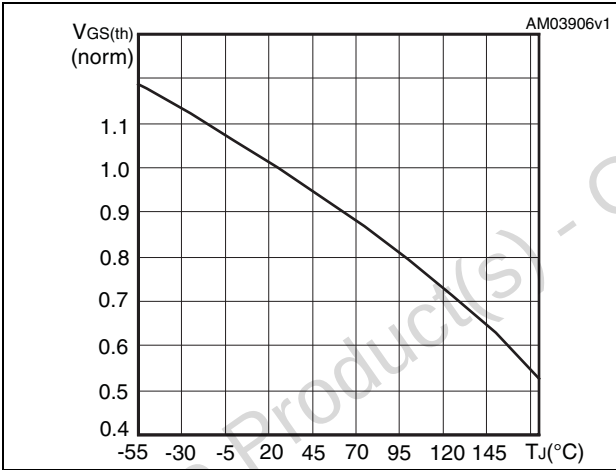


Figure 11. Normalized on-resistance vs temperature

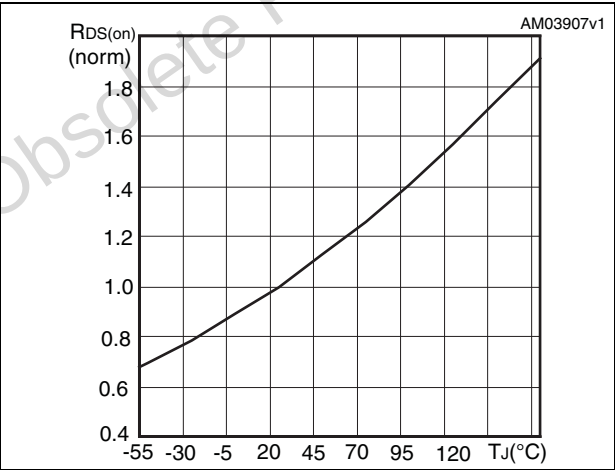
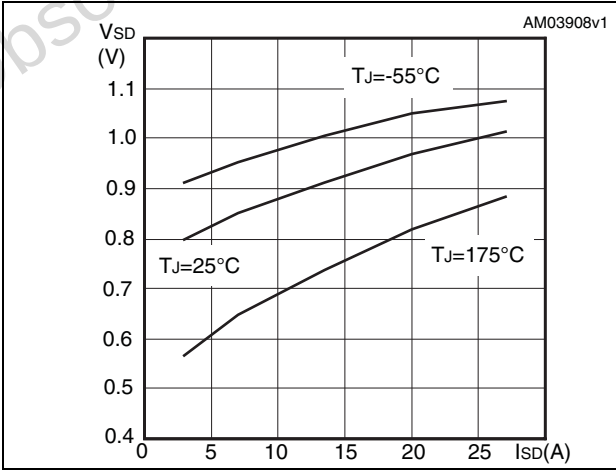


Figure 12. Source-drain diode forward characteristics



2.2 Electrical characteristics (curves) for P-channel

Figure 13. Safe operating area

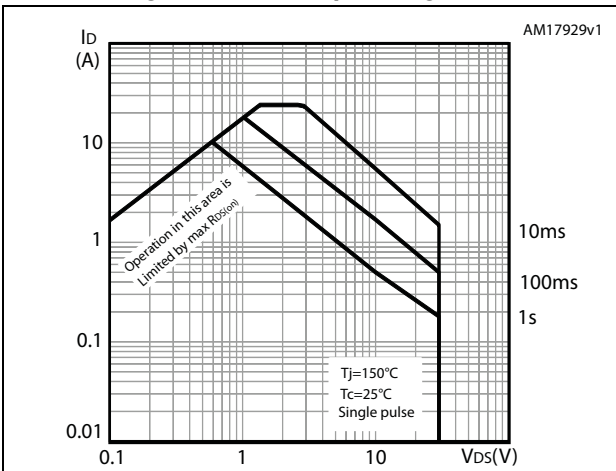


Figure 14. Thermal impedance

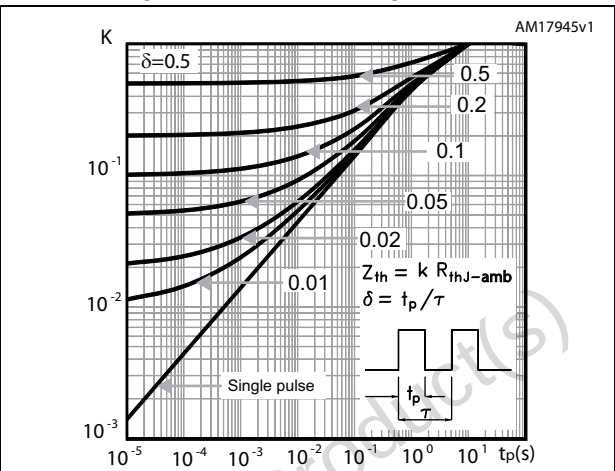


Figure 15. Output characteristics

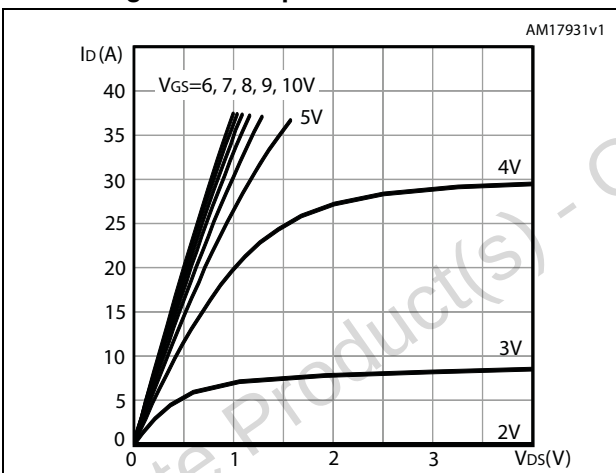


Figure 16. Transfer characteristics

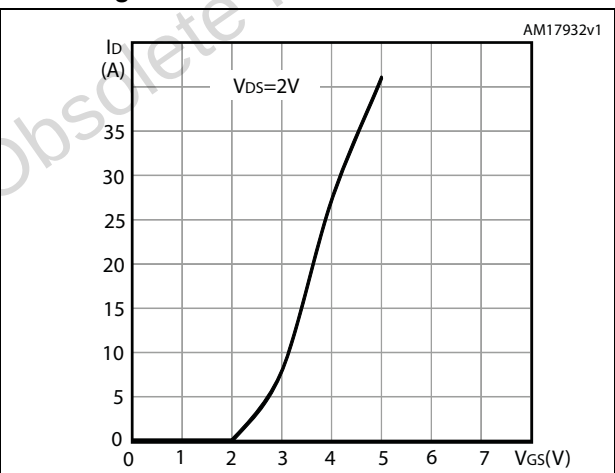


Figure 17. Gate charge vs gate-source voltage

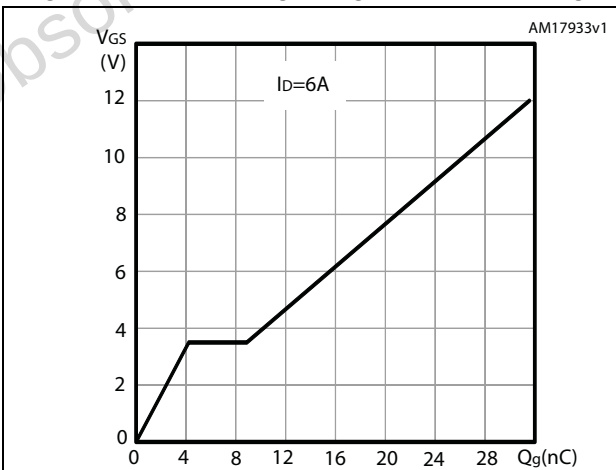


Figure 18. Static drain-source on-resistance

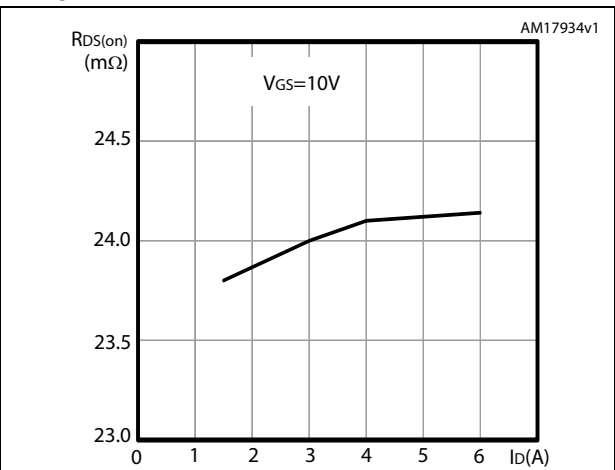


Figure 19. Capacitance variations

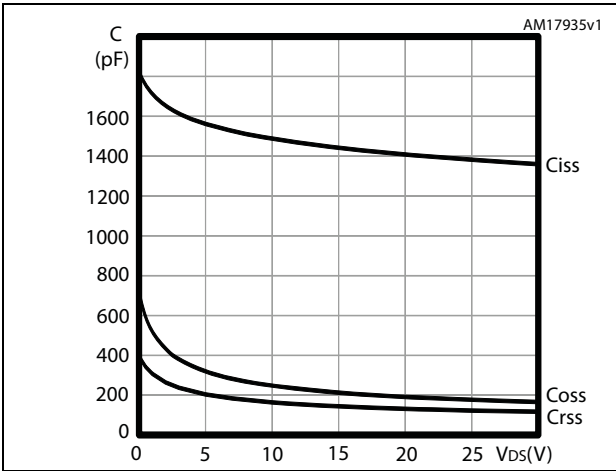


Figure 20. Normalized gate threshold voltage vs temperature

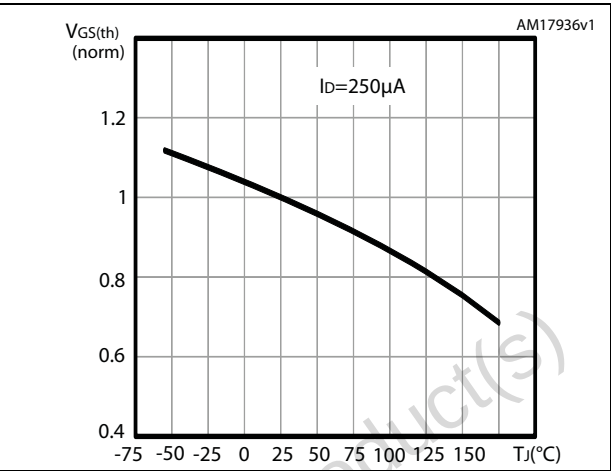


Figure 21. Normalized on-resistance vs temperature

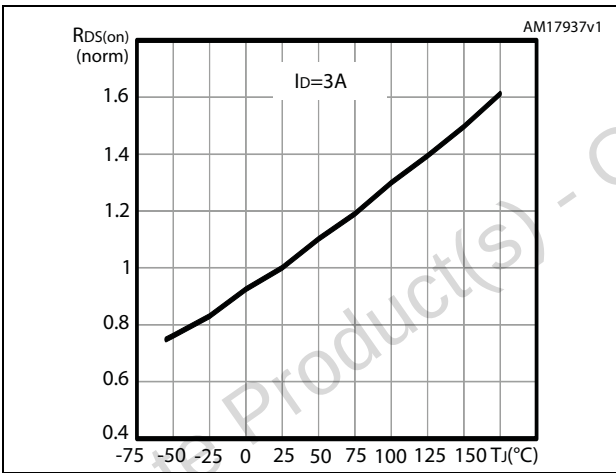


Figure 22. Normalized $V_{(BR)DSS}$ vs temperature

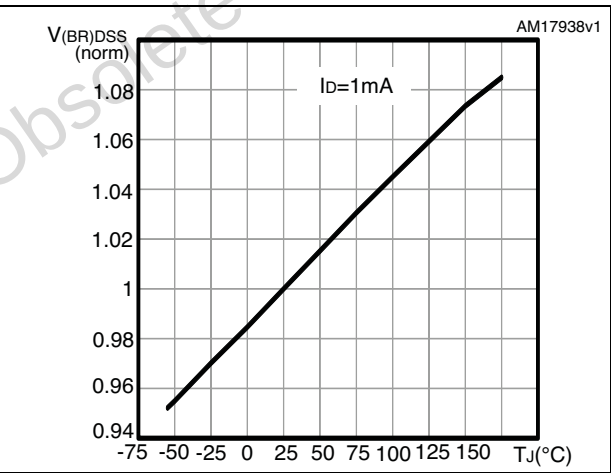
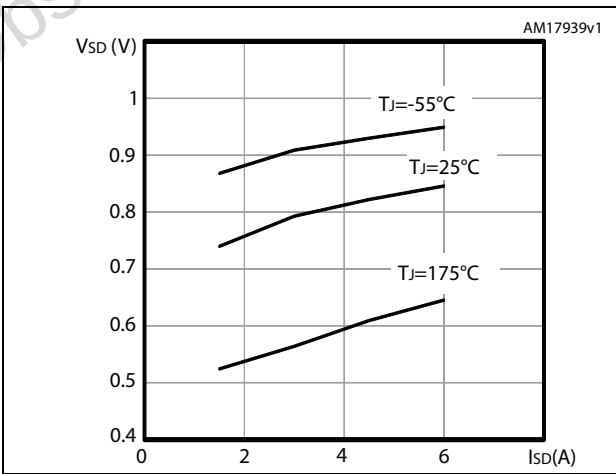


Figure 23. Source-drain diode forward characteristics



3 Test circuits for N-channel

Figure 24. Switching times test circuit for resistive load

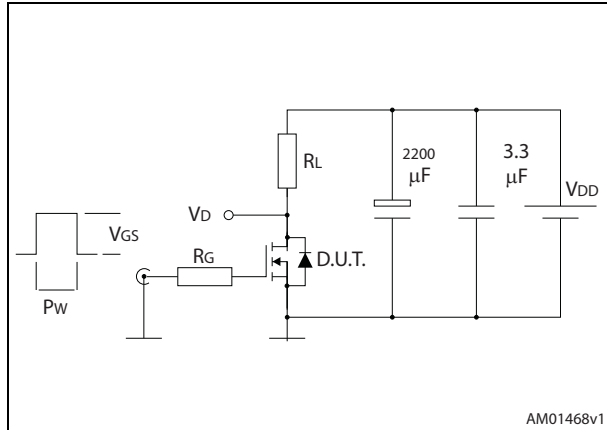


Figure 25. Gate charge test circuit

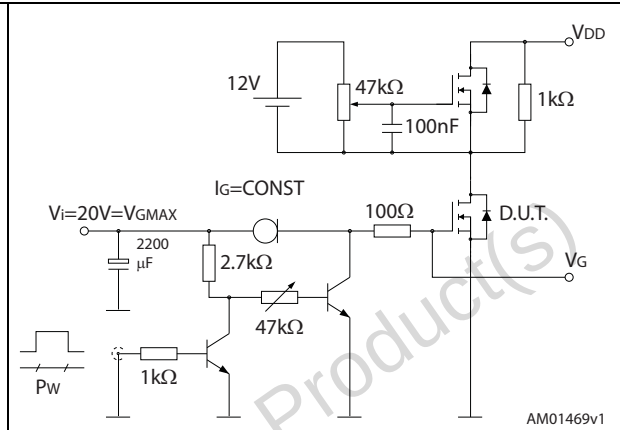


Figure 26. Test circuit for inductive load switching and diode recovery times

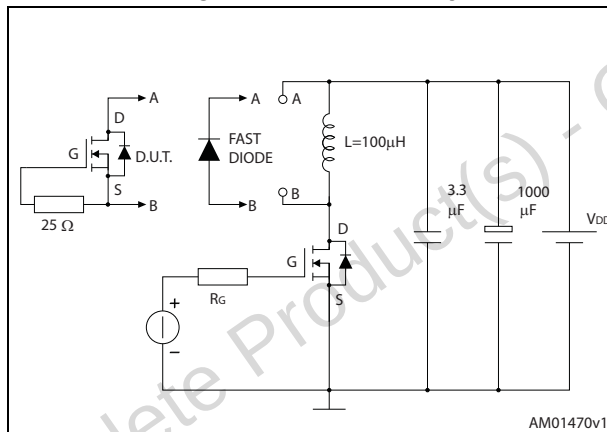


Figure 27. Unclamped inductive load test circuit

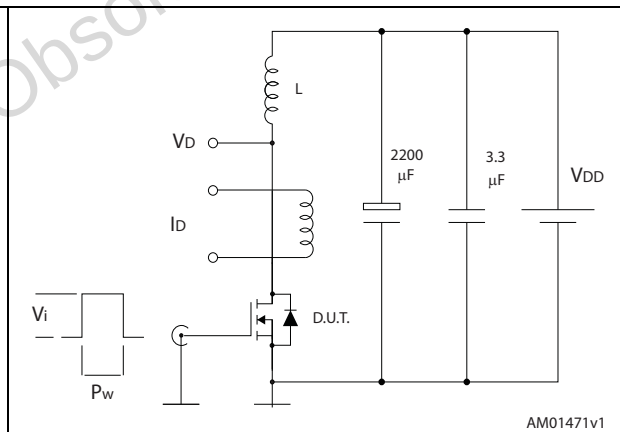


Figure 28. Unclamped inductive waveform

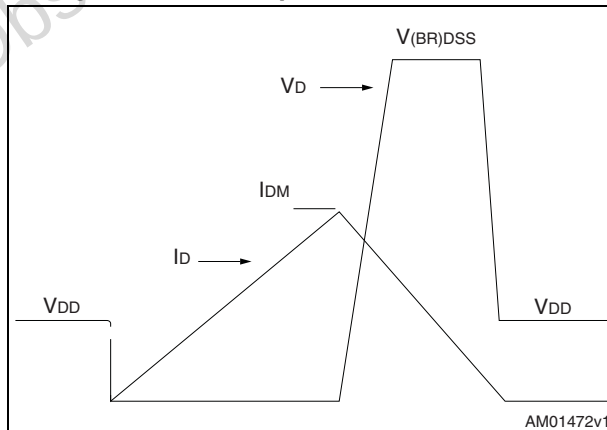
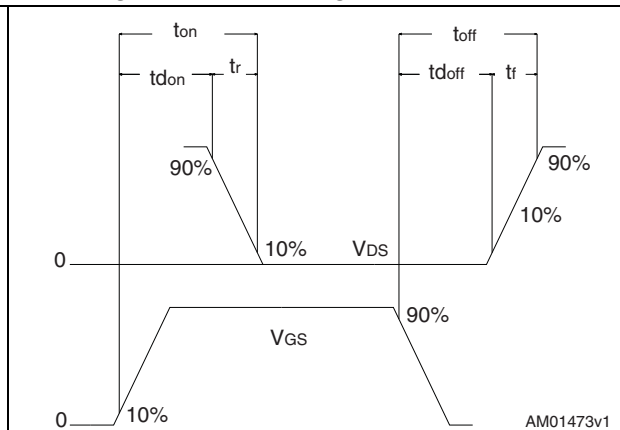


Figure 29. Switching time waveform



4 Test circuits for P-channel

Figure 30. Switching times test circuit for resistive load

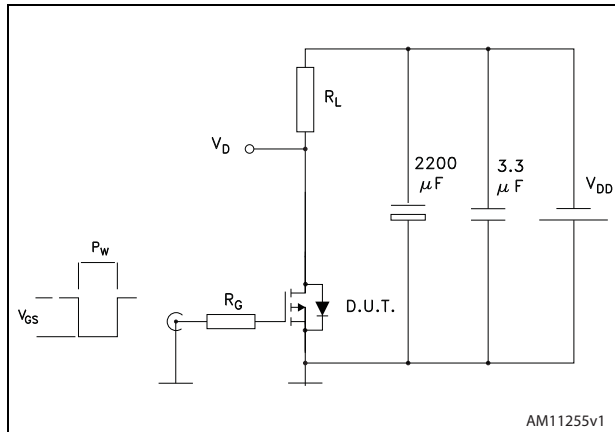


Figure 31. Gate charge test circuit

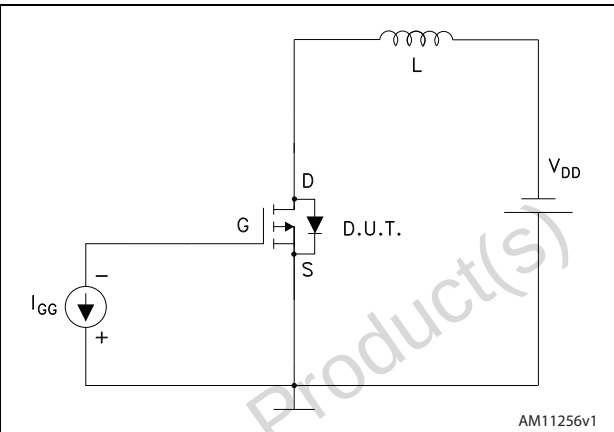
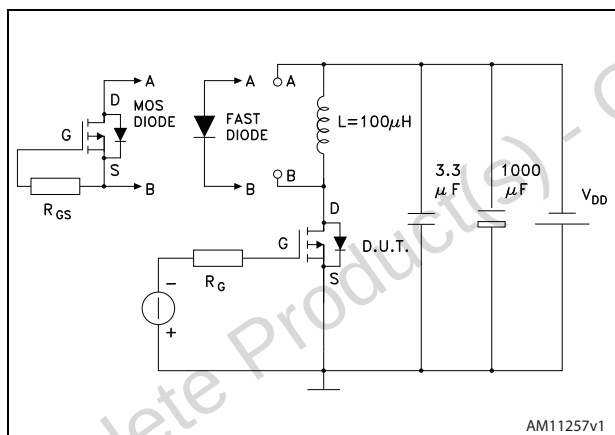


Figure 32. Test circuit for diode recovery behavior



5 Package mechanical data

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Obsolete Product(s) - Obsolete Product(s)

Figure 33. SO-8 drawing

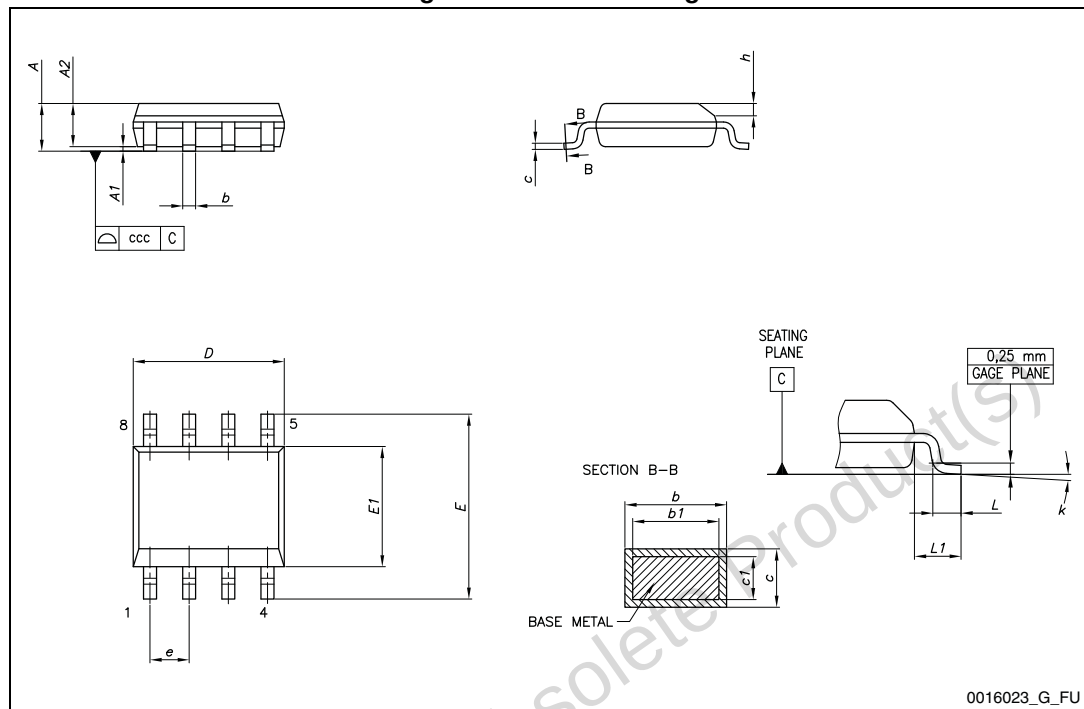
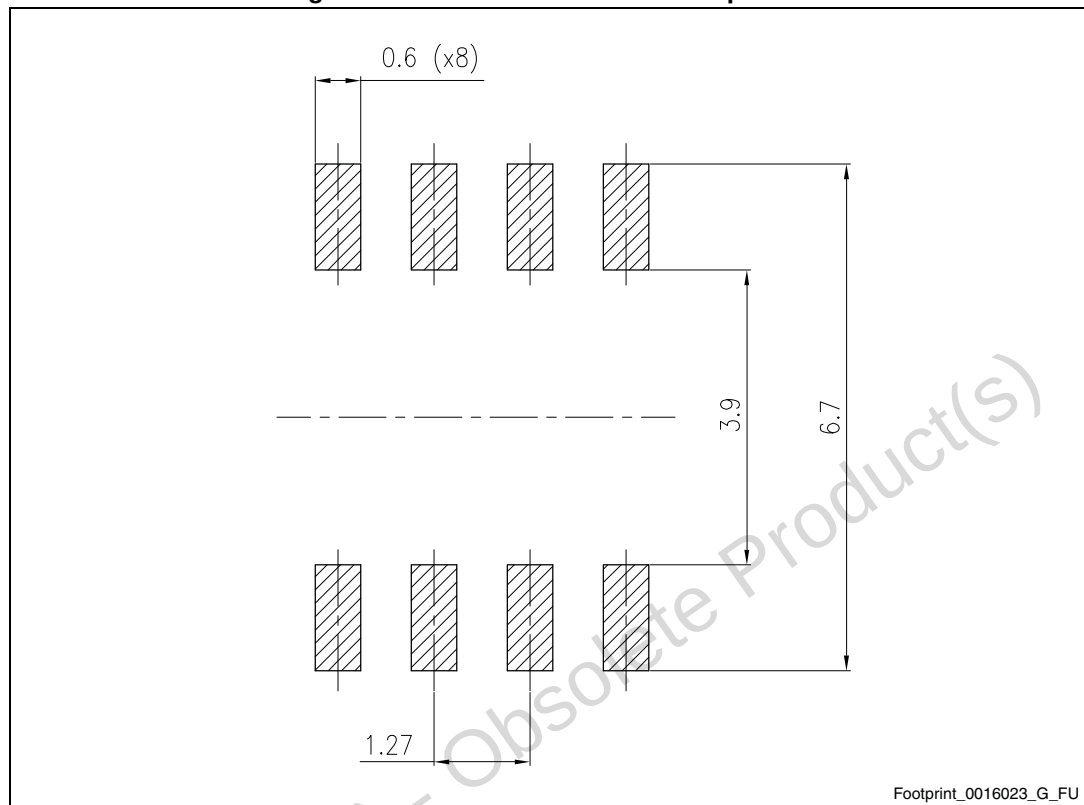


Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 34. SO-8 recommended footprint^(a)

a. All dimensions are in millimeters.

6 Packaging mechanical data

Figure 35. SO-8 tape and reel dimensions

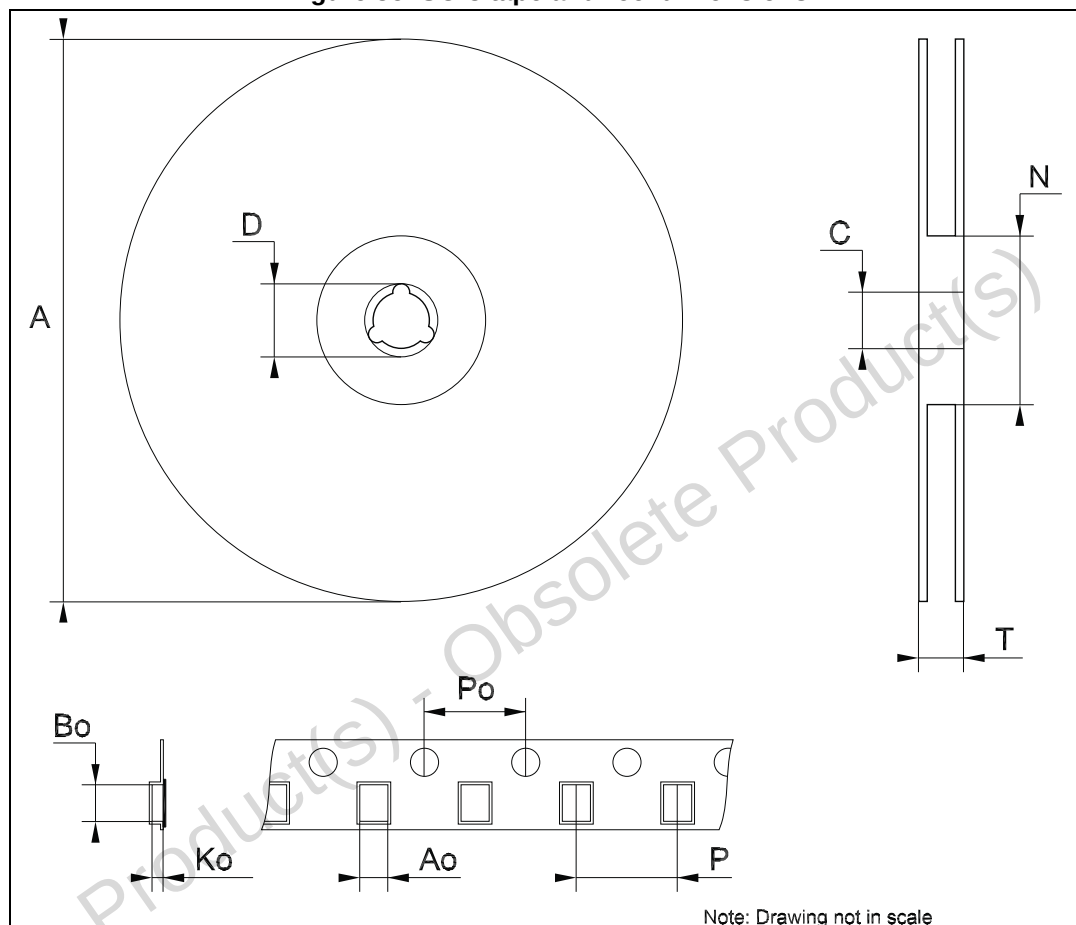


Table 9. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

7 Revision history

Table 10. Revision history

Date	Revision	Changes
01-Feb-2013	1	First revision.
03-Apr-2014	2	– Modified: V_{GS} (for P-channel) value in Table 2 – Modified: P_{TOT} value in Table 2 – Modified: $R_{thj-pcb}$ value in Table 3 – Modified: Q_g typical value in Table 5 – Added: Section 2.1: Electrical characteristics (curves) for N-channel and Section 2.2: Electrical characteristics (curves) for P-channel – Minor text changes
11-Apr-2014	3	– Modified: marking in Table 1 – Minor text changes

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