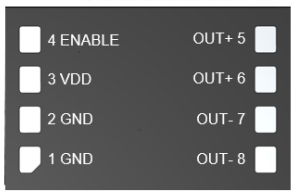
STSID140-12

Datasheet

Surface-mount isolated thyristor driver

DFN 5.35 X 3.45 mm



Bottom view

Product status link
STSID140-12

Product summary	
Order code	STSID140-12
Package	DFN
I_{OUT}	40 mA
V_{ISO}	1.25 kV_{RMS}

Features

- Gate driver for thyristor control
- Triac AC switch and SCR control compliant
- 40 mA current output
- Single 3.3V supply for direct MCU drive
- Maximum junction temperature: 125 °C
- Low quiescent standby current: 5 uA
- Input-output functional isolation:
  - Isolation level tested at 2121 V_{PK}
  - High creepage distance: 3.92 mm compliant with *IEC 60335-1* standard for 250 V_{RMS} application with material group I and overvoltage category II
- EMC performances:
  - High static immunity: *IEC 61000-4-4* EFT at ±4 kV
  - *IEC 61000-4-5* overvoltage: ±4 kV
  - Compliant with *EN 55016-2-1*, CISPR 16-2-1 for conducted noise
  - Compliant with *EN 55016-2-3*, CISPR 16-2-3 for radiated noise
  - Compliant with *ESD IEC 61000-4-2* up to ±2 kV contact
- Package:
  - DFN SMD compact package: 5.35 x 3.45 mm
  - Halogen-free molding, lead-free plating
  - ECOPACK2 compliant

Application

- General-purpose AC line load switching
- Inrush current limiting circuits for industrial SMPS and UPS
- Heating resistor control, solid-state relays
- Motor control circuits and starters

Description

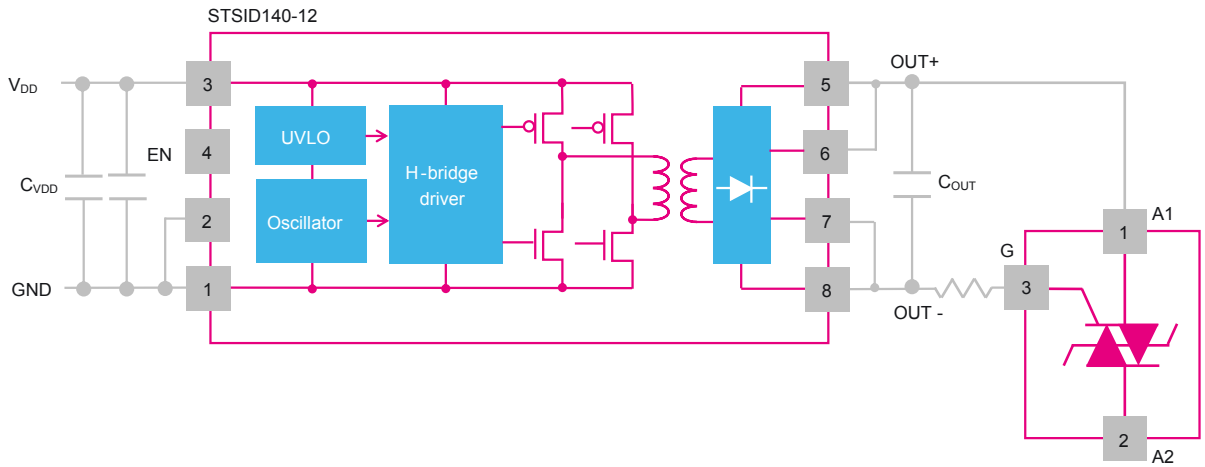
Integrated insulated gate driver for AC switch SCRs or Triacs. Its insulated voltage up to 1.25 kV_{RMS} gives functional insulation to drive any thyristor in industrial application.

The STSID140-12 is a 40 mA output gate driver, allowing to design large range of thyristors for industrial AC motor control, or suitable for inrush current management in AC/DC application.

A high reliability solution, the AC switch-insulated driver is able to ensure high load current switching making the plug and play interface between MCU and SCR/Triac.

1 Application and pins description

Figure 1. Application diagram



Note: Refer to Section 3: Application schematics and test circuit for all thyristor configurations: 3-quadrants Triac, 4-quadrants Triac, Q2/Q3 ACS, and SCR.

C_{VDD} and COUT are mandatory and low ESR capacitors. Typical recommended values are respectively 1 µF // 100 nF and 33 nF. These capacitors must be placed as close as possible from the STSID140-12 for maximum electrical performance.

Table 1. Pins description

Pin #	Type	Description
1	GND	Ground, refer to V_{DD}.
2	GND	Pin 1 and 2 must be connected together on the PCB.
3	V_{DD}	Power supply
4	EN	Enable pin at high level, and output is active. Low level is disabling the circuit.
5	OUT+	Insulated power output. Sourcing current.
6	OUT+	Pin 5 and 6 must be connected together on the PCB.
7	OUT-	Insulated power output reference. Sinking current.
8	OUT-	Pin 7 and 8 must be connected together on the PCB.

2 Electrical characteristics

Stresses beyond the absolute ratings range in Table 2 can cause permanent damage to the device.

These are stress ratings only. The functional operation of the device under these conditions is not ensured.

Exposure to operating conditions outside the recommended operating conditions into Table 3, and up to absolute maximum ratings into Table 2 for extended periods, may affect device reliability.

This driver is suitable for functional electrical insulation only within the maximum operating ratings. Ensure compliance with the safety ratings by using suitable protective circuits.

Table 2. Absolute maximum ratings (limiting values), T_{amb} = 25 °C unless otherwise specified

Symbol	Test conditions	Value	Unit
I_{OUTM}	Maximum output current, at V_{DD} = 3.47 V	55	mA
V_{DD}	Maximum voltage range (T_j = -30 °C to 125 °C)	-0.5 to +4.5	V
T_{STG}	Storage temperature range	-40 to +150	°C
T_J	Operating junction temperature range	-30 to +125	°C
T_l	Maximum lead temperature soldering during 10 s	245	°C
V_{WRM}	OUT+ to OUT-, DC voltage	6	V
V_{HBM}	ESD – HBM	±2	kV
V_{IEC}	According to *IEC 61000-4-2* conditions – Contact surge applied between 6/7/8 shorted versus 1/2/3/4 shorted	±4	kV
V_{OUTSM}	Maximum non-repetitive surge voltage between OUT+ and OUT-	30	V_{KP}
V_{OUTRM}	Maximum repetitive surge voltage between OUT+ and OUT-	30	V_{KP}

Table 3. Recommended operating conditions

Symbol	Test conditions		Value	Unit
I_{OUT}	Output current range,with V_{DD} = 3.14 V, T_{OP} = -30 °C to 85 °C, and V_{OUT} = 1.5 V, and C_{OUT} = 33 nF	Max.	40	mA
		Min.	10	mA
V_{DD}	Supply voltage range	Min.	3.14	V
		Max.	3.47	V
t_{ON}	Output enable delay, to reach 90 % of steady-state V_{OUT}, R_{OUT} = 82 Ω (1), V_{DD} = 3.3 V, T_{amb} = 25 °C, C_{OUT} = 33 nF	Typ.	5	µs
T_J	Operating junction temperature range		-30 to +125	°C

1. *Resistor between out+ and out- for test purpose.*

Table 4. Isolation parameters according to *IEC 60747-17* (T_{amb} = 25 °C)

Symbol	Test conditions		Value	Unit
CLR	External clearance distance, minimum value		3.92	mm
CPG	External creepage distance, minimum value		3.92	mm
CTI	Comparative tracking index		600	V
MG	Material group			1
OC	Overvoltage category			2
MSL	Moisture sensitive level		1	
CMTI	Common-mode transient isolation (1), according to *IEC 60747-17*, V_{CM} = V_{ISO} = 1250 V	Typ.	70	kV/µs
Q_{PD}	Apparent charge, method b2: 100 % final production test for 1 s, V_{PD} = V_{INI} = 1.2 x V_{IOTM} = 2121 V_{PK}, t_{INI} = 1 s	Max.	5	pC
	Method a: After I/O safety test subgroup 2/3,V_{INI} = V_{IOTM}, t_{INI} = 60 s, V_{PD} = 1.2 × V_{IORM} = 741 V_{PK}, t_m = 10 s			
	Method a: After environmental tests subgroup 1, V_{INI} = V_{IOTM}, t_{INI} = 60 s, V_{PD} = 1.3 × V_{IORM} = 803 V_{PK}, t_m = 10 s			
R_{IO}	Minimum input to output isolation (2) resistance, $V_{I/O}$ = 500 V	T_J = 25 °C	>10^{12}	Ω
		T_J = 125 °C	>10^9	Ω
V_{ISO}	Input to output (2), insulation RMS voltage (100 % final production test at 1500 V_{RMS} for 1 s)	60 s	1250	V_{RMS}
V_{IOTM}	Input to output (2), maximum transient isolation AC peak voltage (100 % final production test at 2121 V_{PK} for 1 s)	60 s	1767	V_{PK}
V_{IORM}	Input to output (2), maximum rated repetitive peak isolation voltage	AC	618	V_{PK}
		DC	450	V_{DC}
V_{IOWM}	Input to output (2), maximum RMS working voltage		437	V_{RMS}
V_{IMP}	Impulse voltage, peak value of 1.2/50 µs waveform without flashover, input to output (2), according to *IEC 61000-4-5*		±2.5	kV
V_{IOSM}	Internal isolation barrier breakdown peak voltage, input to output (2), according to *IEC 61000-4-5* conditions, 1.2/50 µs waveform (3)		±4	kV
C_{IO}	Barrier capacitance, input to output (2), V_{AC} = 30 mV, and f = 1 MHz	Typ.	3	pF

1. *Not tested in production.*
2. *Input pins short-circuited together (V_{DD}, GND, and EN) versus output pins short-circuited together (OUT+ and OUT-).*
3. *Tested in nonconductive liquid environment.*

Table 5. Input characteristics (T_{amb} = 25 °C unless otherwise specified)

Symbol	Test conditions		Value	Unit
R_{IN}	Input pull-down resistor	Typ.	100	kΩ
$I_{Q\text{-}OFF}$	Maximum quiescent current, EN= 0 and V_{DD} = 3.3 V	Max.	5	µA
I_{DD}	V_{DD} pin consumption with I_{OUT} = 40 mA and V_{DD} = 3.3 V	Max.	90	mA
V_{IH}	EN input high-level threshold voltage	Max.	70 % of V_{DD}	V
V_{IL} (1)	EN input low-level threshold voltage	Min.	30 % of V_{DD}	V
UVLO	Undervoltage-lockout disabling operation	Max.	2.96	V

1. *Value guaranteed by design and characterization data.*

Table 6. Thermal characteristics

Symbol	Test conditions		Value	Unit
$R_{th\ j\text{-}a}$	Junction to ambient thermal characteristics, according to JEDEC JESD51-x	Typ.	220	°C/W

2.1 Typical characteristics curves

Typical performance

Figure 2. Typical performance curve versus V_{DD}

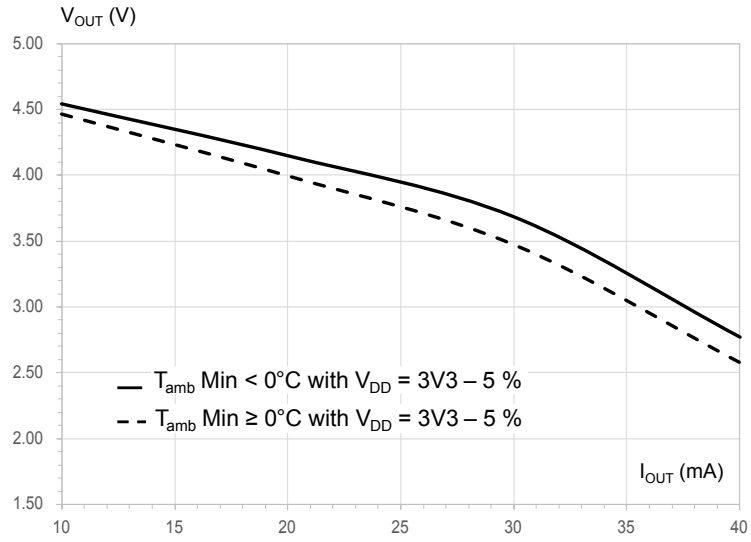
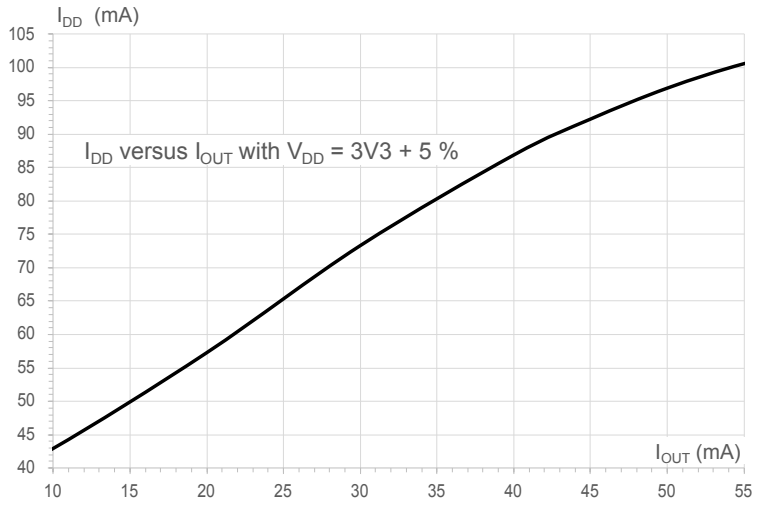


Figure 3. Typical performance curve versus T_{amb}



In order to define the gate resistor (R_G) we have to consider the thyristor gate current (I_{GT}) and gate voltage (V_{GT}).

Thyristor datasheet provide these worst case data at T_{amb} min.

In order to calculate the minimum resistor value you can refer to the V_{OUT} curve of STSID140 at T_{amb} min. and V_{DD} min. according to the formula below :

$$R_G \geq \frac{V_{OUT}(I_G(T_{amb\,min.}),\ T_{amb\,min.}) - V_G(T_{amb\,min.})}{I_G(T_{amb\,min.})}$$

RG must not be lower than 60 Ω.

3 Application schematics and test circuit

Figure 4. **Application schematics to drive Triac**

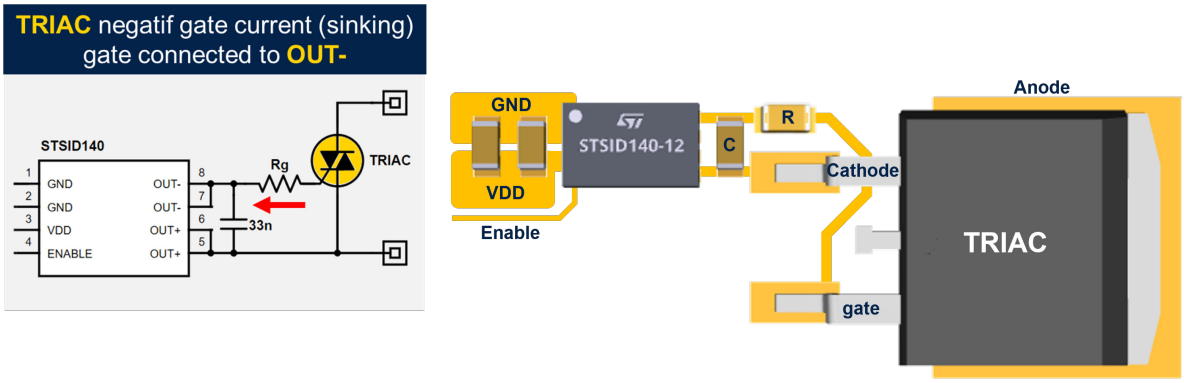


Figure 5. **Application schematics to drive SCR**

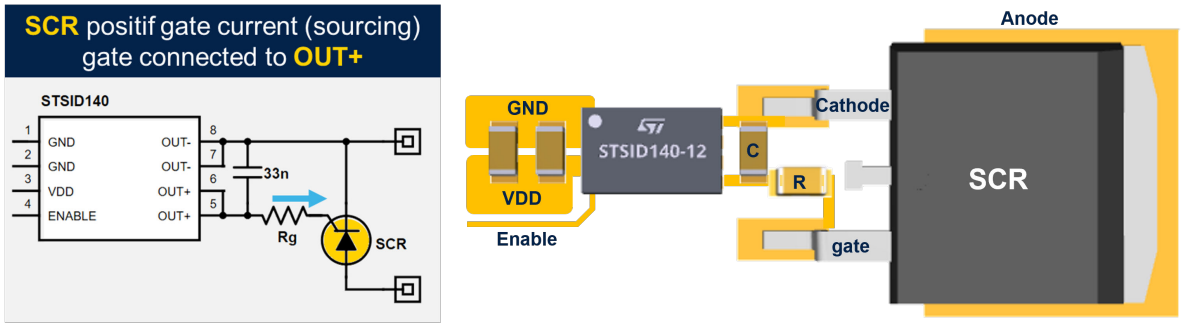
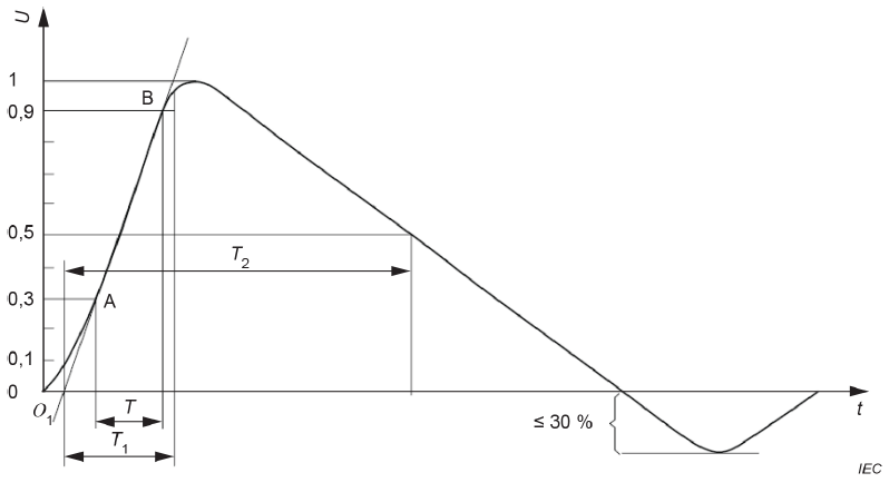


Figure 6. ***IEC 61000-4-5* test circuit**



Front time: $T_1 = 1{,}67 \times T = 1{,}2\ \mu s \pm 30\ \%$
Time to half-value: $T_2 = 50\ \mu s \pm 20\ \%$

4 Ordering information

Figure 7. **Ordering information scheme**

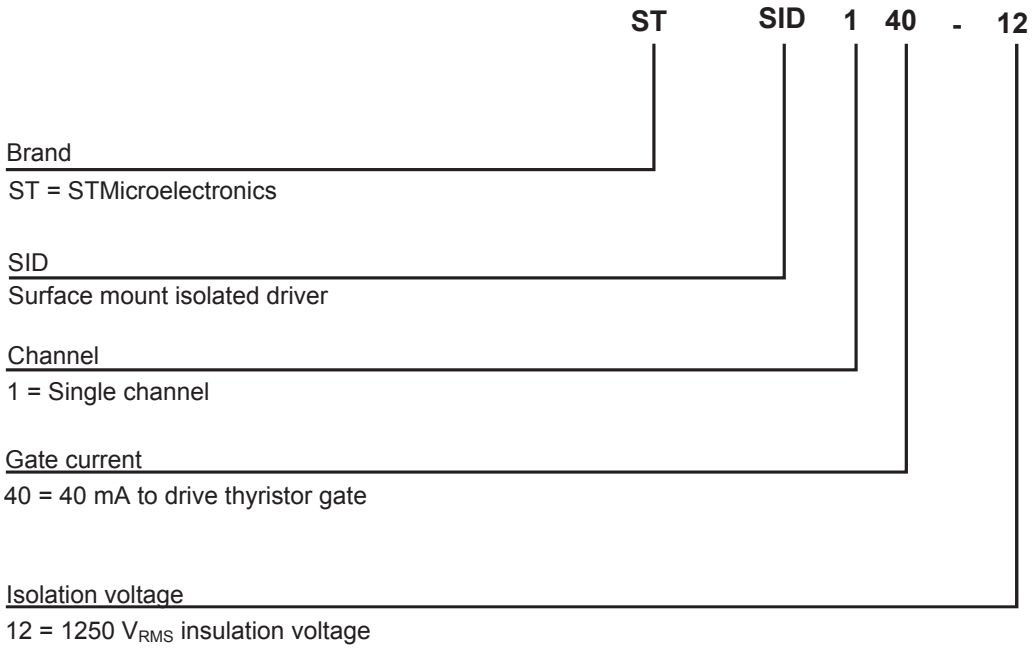


Table 7. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
STSID140-12	STSID140-12	DFN 5.35 x 3.45	47 mg	3000	Tape and reel

5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 Package information

- Halogen-free molding, lead-free plating

Figure 8. DFN 5.35 x 3.45 mm package outline

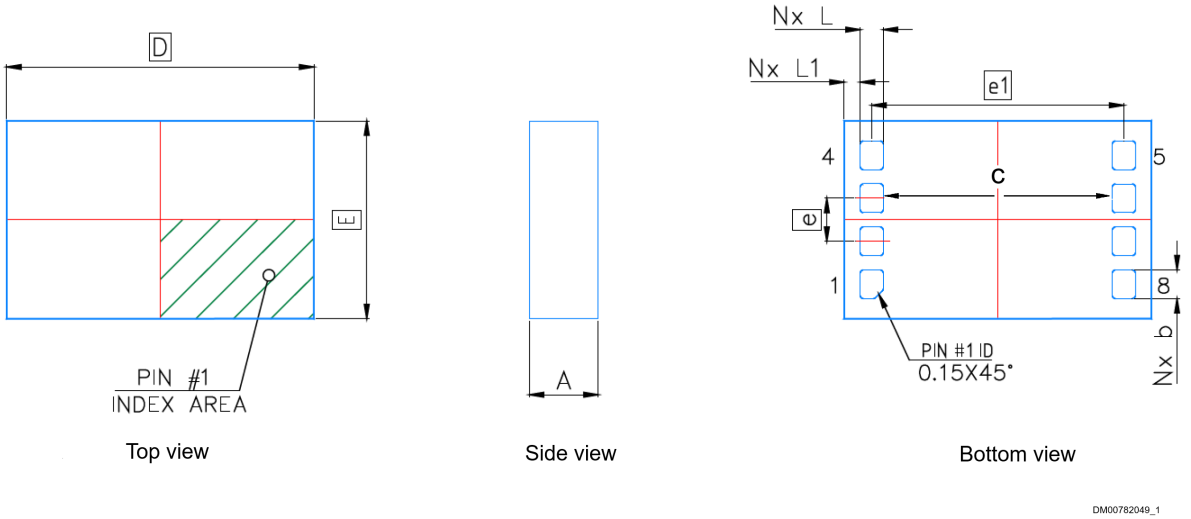
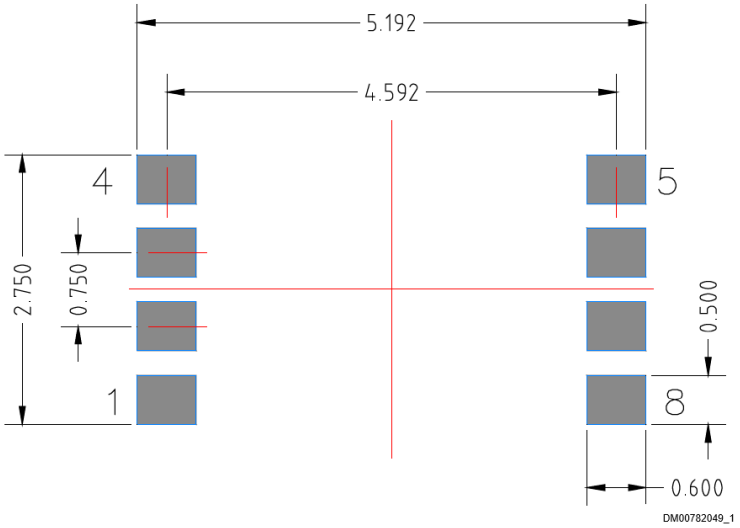


Table 8. DFN 5.35 x 3.45 mm mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	1.10	1.20	1.30
b	0.45	0.50	0.55
C	3.92		
D	5.25	5.35	5.45
E	3.35	3.45	3.55
e		0.75	
e1		4.392	
L	0.35	0.40	0.45
L1	0.229	0.279	0.329
N		8	

Figure 9. **Recommended footprint (dimensions in mm)**



- Recommended pad stencil: 450 µm x 540 µm
- Recommended stencil thickness: 150 µm

Figure 10. **Recommended layout**

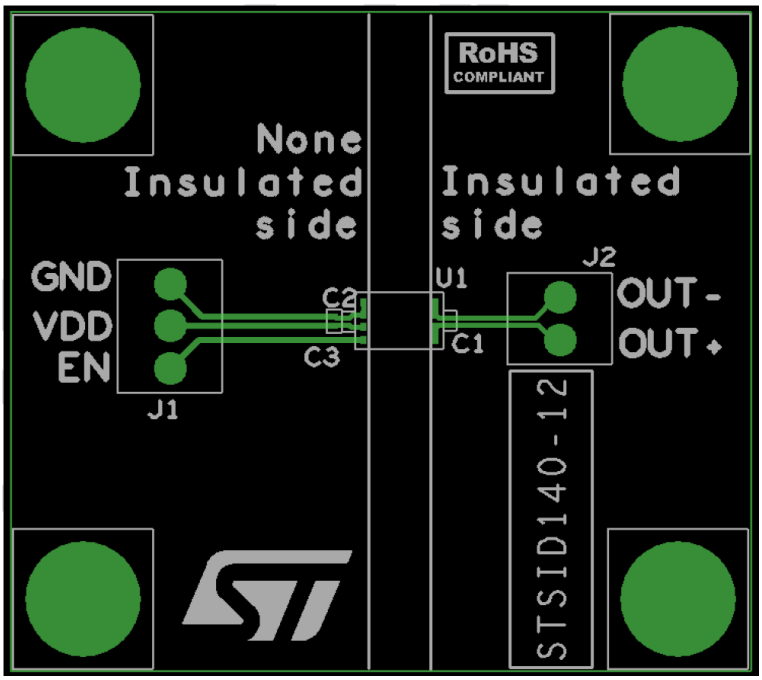


Figure 11. **Marking**

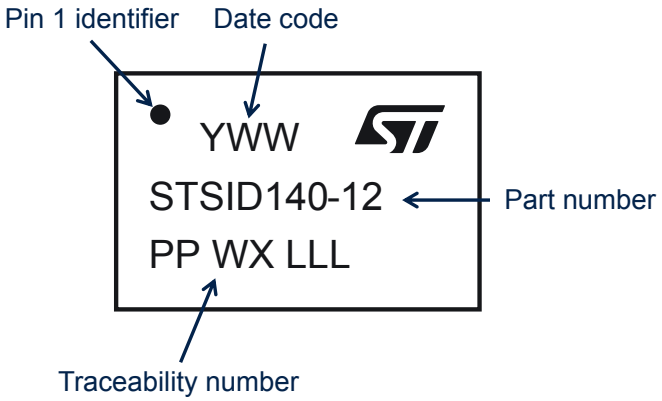
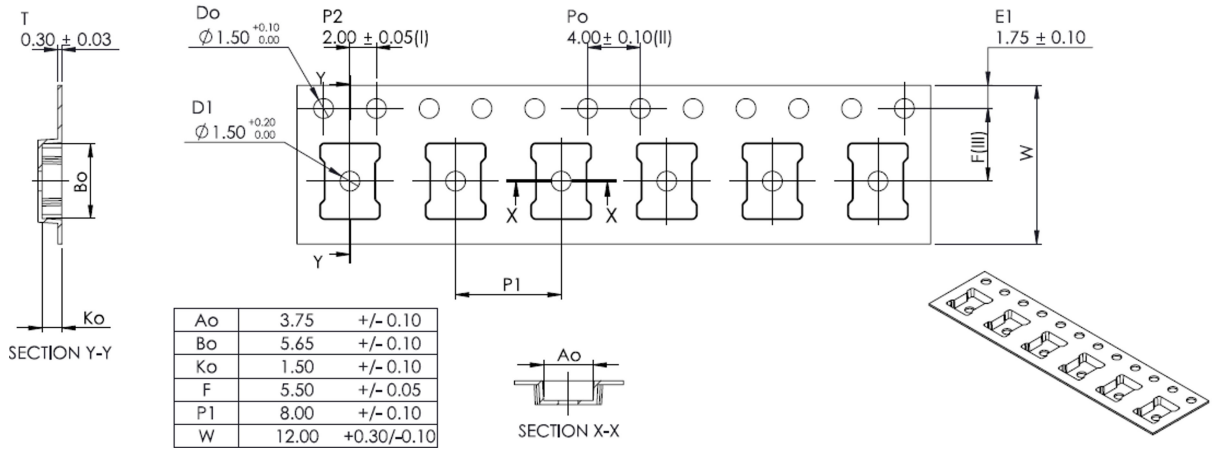


Figure 12. **Carrier tape information**

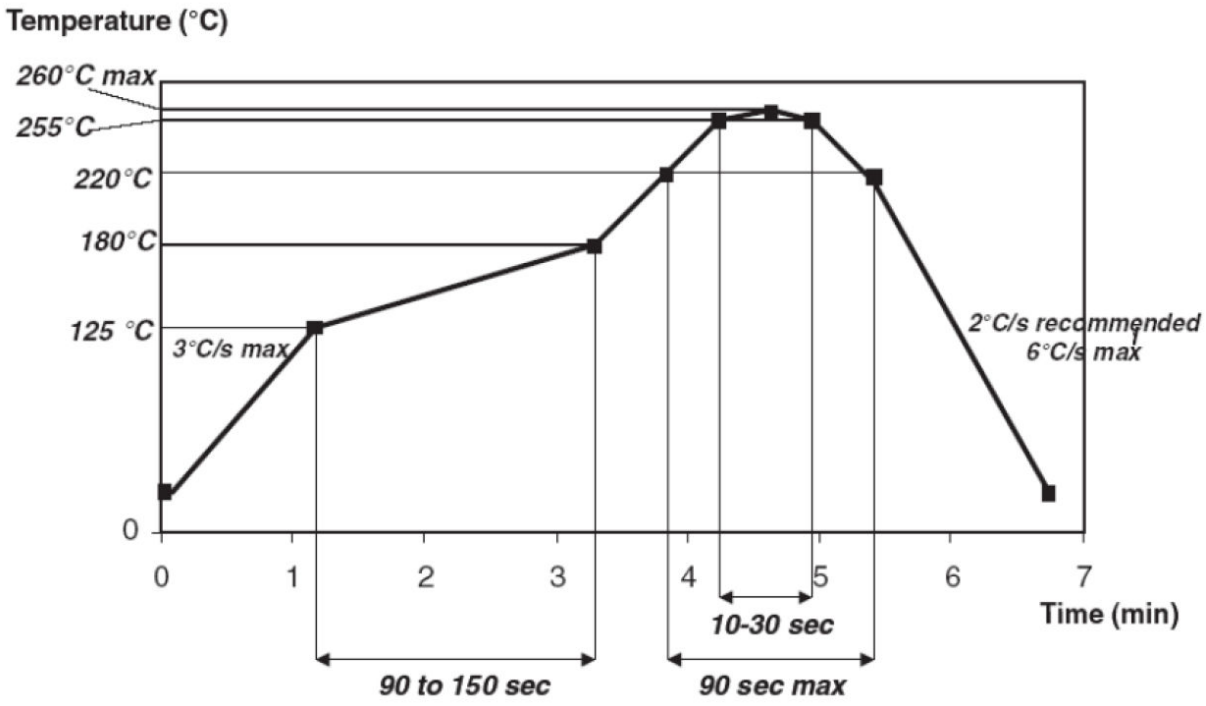


Ao	3.75	+/- 0.10
Bo	5.65	+/- 0.10
Ko	1.50	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+0.30/-0.10

5.1.1 Recommended soldering reflow profile

The package is following IPC/JEDEC J-STD-020E requirements, and thus can be exposed to a maximum temperature of 245 °C for 10 seconds. Overheating during the reflow-soldering process may damage the device, therefore any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical leadfree solder heating profiles (ST ECOPACK) are given here below for mounting on an FR4 PCB.

Figure 13. Recommended soldering profile



Revision history

Table 9. **Document revision history**

Date	Revision	Changes
18-Sep-2025	1	Initial release.

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.