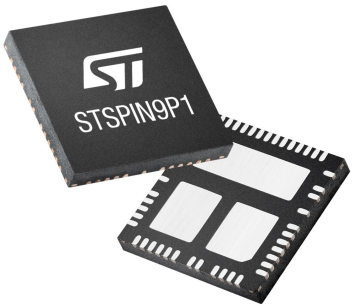
STSPIN9P1

Datasheet

75 V high-current half-bridge advanced motor driver series



Features

- Supply voltage from 7 V to 75 V
- Embedded power MOSFETs with scalable current ratings:
  - 10 A_{rms}, $R_{DS(ON)}$ = 16 mΩ typ
  - 6 A_{rms}, $R_{DS(ON)}$ = 27 mΩ typ
- Current sensing amplifier
- Current limiter implementing PWM trimming or fixed OFF time control
- Adjustable slew rate for improved EMI/efficiency trade-off
- Full set of protections: overtemperature, overcurrent and UVLO
- Open-load detection

Applications

- Stage lighting
- Factory automation
- ATM and money handling machines
- Textile machines
- Home appliances
- Robotics

Product status link
STSPIN9P11
STSPIN9P12
STSPIN9P13
STSPIN9P14
STSPIN9P15
STSPIN9P16
STSPIN9P17
STSPIN9P18

Product label
SUSTAINABLE TECHNOLOGY

Description

The STSPIN9P series is an extremely flexible platform that supports a wide range of low-voltage motors with power ratings up to 500 W, including stepper, brushed, and brushless DC motors.

Thanks to the integration of low $R_{DS(ON)}$ MOSFETs (16 mΩ or 27 mΩ depending on the model), the BOM space saving compared to discrete solutions is significant.

The supply voltage is wide, ranging from 7 to 75 V. The series offers a set of pin-to-pin compatible half-bridge and full-bridge topologies, enabling coverage of a broad variety of applications.

The STSPIN9P1 sub-series includes pin-to-pin compatible half-bridge devices. Components in the STSPIN9P1 series differ in $R_{DS(ON)}$, driving mode, and control features to enable the adoption of a tailored solution for each specific application.

Despite their topological simplicity, the devices integrate a wide set of functional blocks and advanced features.

All versions integrate regulators making the device fully self-supplied. A charge pump allows unlimited high-side on time.

The integrated AFE, composed of a differential amplifier and a comparator, is designed to amplify the signal from a shunt resistor and compare it to a reference.

In case of versions with integrated current limiter, the comparator output is used to implement a fixed off time or a PWM trimming control strategy, otherwise it is only available for the application on the COUT open-drain output.

All devices in the STSPIN9P series feature the adjustable slew rate, enabling optimization of the EMI/efficiency trade-off. This capability improves overall performance and accelerates customer design qualification.

The devices are also fully protected thanks to UVLO (overcurrent protection and thermal shutdown). Additionally, open-load detection verifies proper motor connection when the power stage is disabled, providing dedicated signaling on the nOL output.

The STSPIN9P1 products come in a compact 7x7 QFN package.

1 Overview

The STSPIN9P1 platform targets high-current motor-driving solutions with particular focus on brushed-DC motors.

The family encompasses several systems-in-package composed of one control die and two MOSFET dies implementing a half-bridge topology.

For each topology, different power-MOSFET die sizes are available, as listed in Table 1.

Products also differentiate according to the features provided by the control die:

Table 1. Half-bridge ordering codes

Order code	R_{DSON} (mΩ)	I_{RMS} (A)	Input logic	Curr. limiter
STSPIN9P11	16	10	IN, EN	Yes
STSPIN9P12	16	10	IN, EN	No
STSPIN9P13	16	10	INH, INL	Yes
STSPIN9P14	16	10	INH, INL	No
STSPIN9P15	27	6	IN, EN	Yes
STSPIN9P16	27	6	IN, EN	No
STSPIN9P17	27	6	INH, INL	Yes
STSPIN9P18	27	6	INH, INL	No

2 Block diagrams

Figure 1. **STSPIN9P11 / STSPIN9P15 half-bridge with current limiter, EN/IN driving**

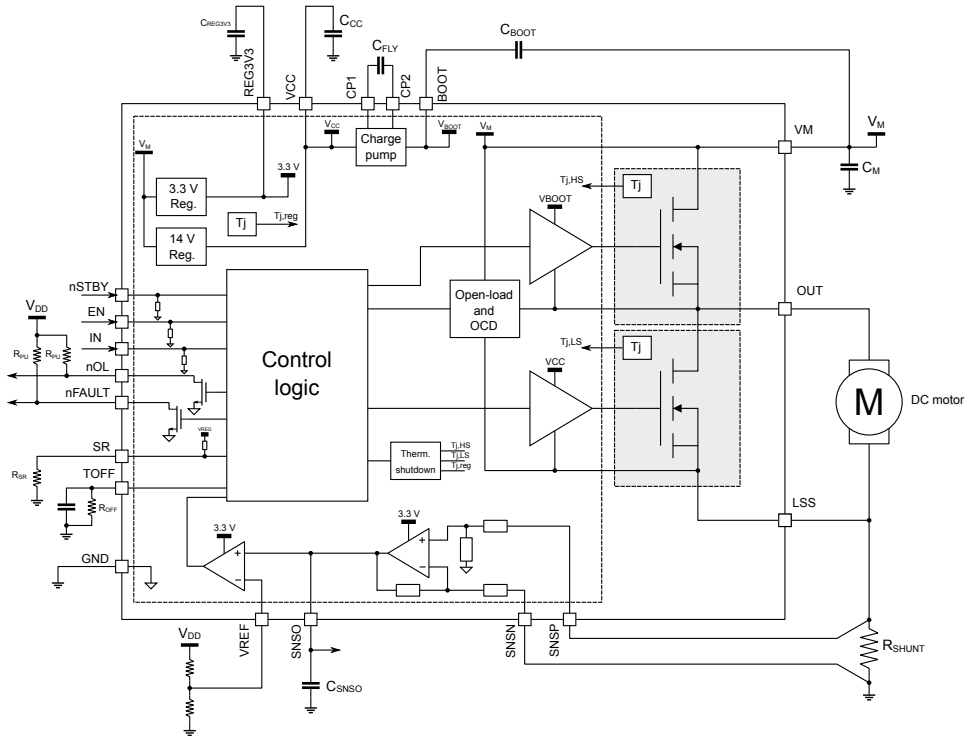


Figure 2. **STSPIN9P13 / STSPIN9P17 half-bridge with current limiter, INH/INL driving**

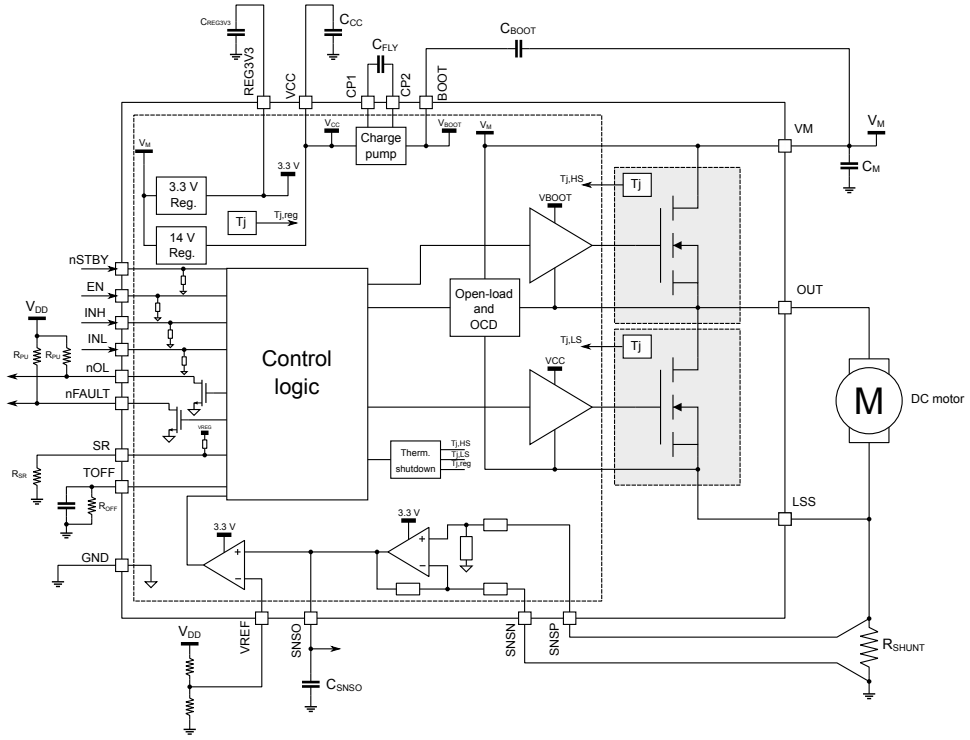


Figure 3. **STSPIN9P12 / STSPIN9P16 half-bridge with uncommitted AFE, EN/IN driving**

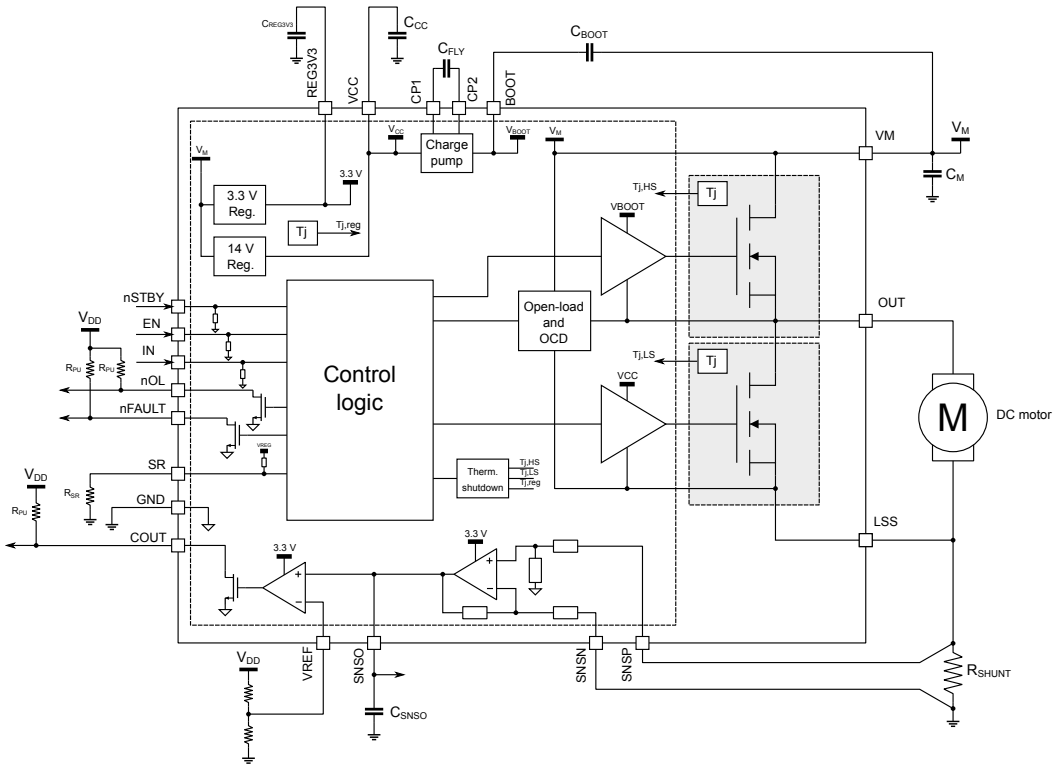
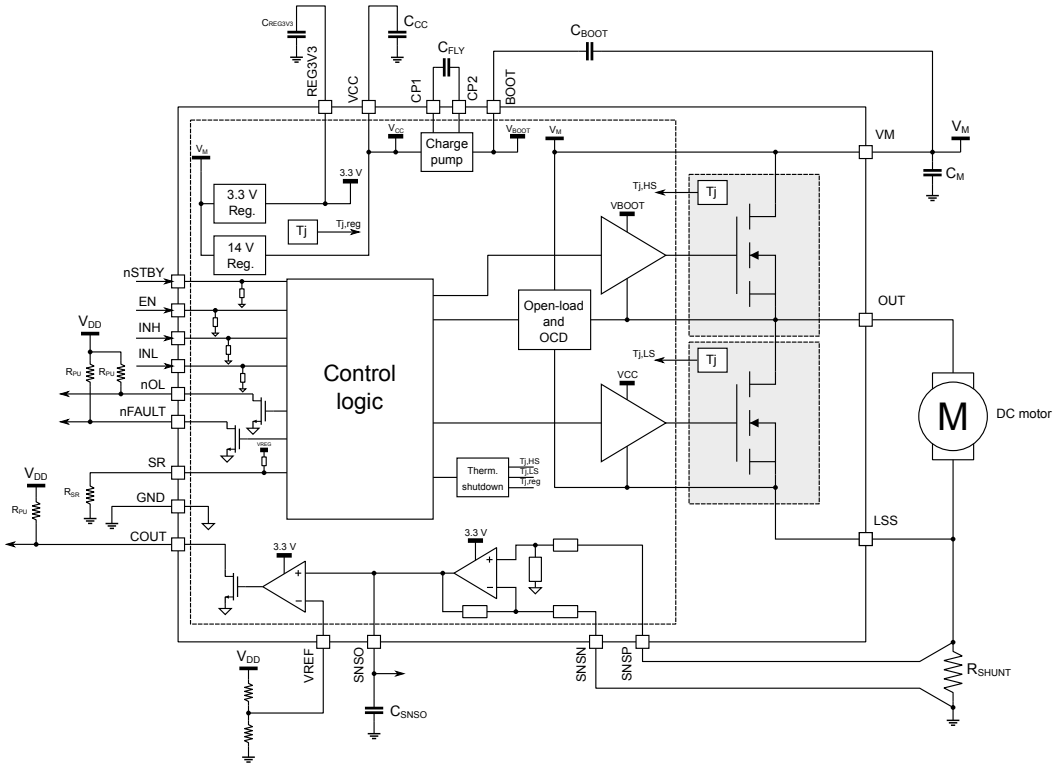


Figure 4. **STSPIN9P14 / STSPIN9P18 half-bridge with uncommitted AFE, INH/INL driving**



3 Pin description

Figure 5. **STSPIN9P1 half-bridge - pinout**

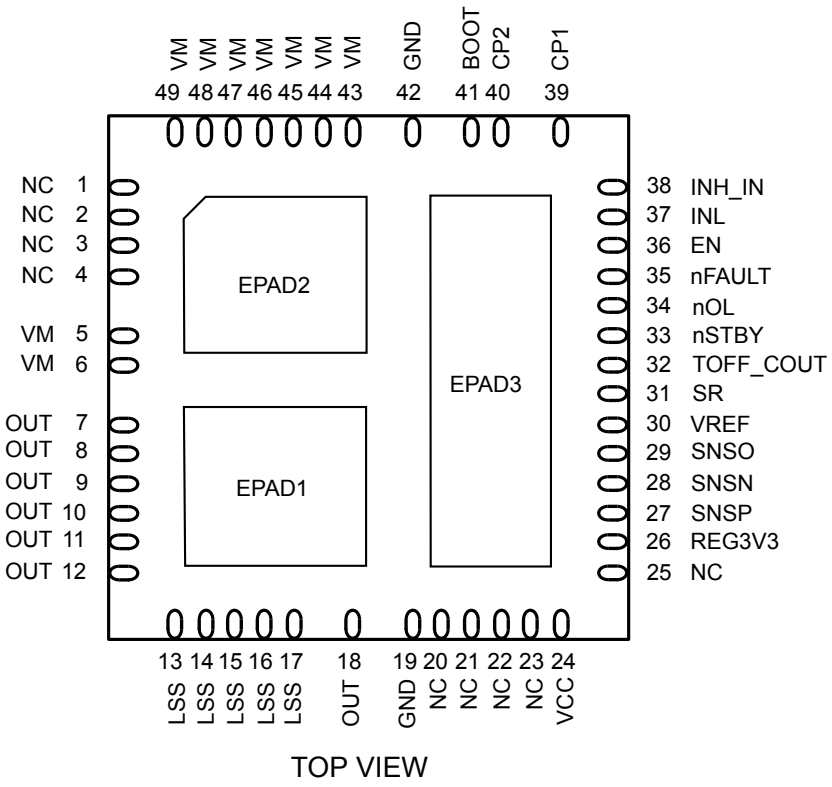


Table 2. **STSPIN9P1 half-bridge - pin assignment**

Pin n.	Name	Type	Function
1, 2, 3, 4, 20, 21, 22, 23, 25	NC	-	Not connected
5, 6, 43, 44, 45, 46, 47, 48, 49, EPAD2	VM	Supply	Main supply voltage (HS MOSFET drain)
7, 8, 9, 10, 11, 12, 18, EPAD1	OUT	Analog out	Half-bridge output (LS MOSFET drain, HS MOSFET source)
13, 14, 15, 16, 17	LSS	Analog out	Half-bridge reference voltage (LS MOSFET source)
19, 42, EPAD3	GND	Ground	Ground
24	VCC	Supply	14 V regulator output
26	REG3V3	Supply	3.3 V regulator output
27	SNSP	Analog input	Sense amplifier non inverting input
28	SNSN	Analog input	Sense amplifier inverting input
29	SNSO	Analog output	Sense amplifier output/Comparator non inverting input
30	VREF	Analog input	Current limiter reference/Comparator inverting input
31	SR	Analog input	Slew-rate setting
32	COUT	Open-drain output	Comparator open-drain output

Pin n.	Name	Type	Function
32	TOFF	Analog input	Current limiter off-time setting Short to ground for PWM trimming mode
33	nSTBY	Digital input	Active low standby
34	nOL	Open-drain output	Open load detection drain output
35	nFAULT	Open-drain output	Fault open drain output
36	EN	Digital input	Enable input
37	INL	Digital input	Driving input
38	INH IN	Digital input	Driving input
39	CP1	Analog out	Fly capacitor pin 1
40	CP2	Analog out	Fly capacitor pin 2
41	BOOT	Supply	Bootstrap voltage

4 Device ratings

4.1 Absolute maximum ratings (AMR)

Stresses above the absolute maximum ratings listed in Table 3 may cause permanent damage to the device. Prolonged exposure to conditions at or above the maximum ratings may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_M	Main supply voltage		-0.3 to 80 (1)	V
V_{CC}	Gate driver supply voltage		-0.3 to 18	V
V_{REG3V3}	3.3 V regulator supply voltage		-0.3 to 4	V
I_{OUT}	Output current (each output) DC current	10 A option	10	A
		6 A option	6	
CP1	Charge pump capacitor pin 1 voltage		-0.3 to V_M+0.3	V
CP2	Charge pump capacitor pin 2 voltage		-0.3 to BOOT+0.3	V
V_{BOOT}	Bootstrap voltage		-0.3 to V_M+18	V
V_{OUTx}	OUTx pin voltage	DC	-0.6 to V_M+0.4	V
V_{SLS}	Low-side source voltage	DC	-0.6 to +0.6	V
V_{IO}	Logic input/output voltage		-0.3 to 5.5	V
V_{SR}	Slew rate pin voltage		-0.3 to V_{REG3V3}+0.3	V
I_{OD}	Open-drain sink current		Up to 10	mA
V_{SNSO}	Current-sensing amplifier output voltage		-0.3 to V_{REG3V3}+0.3	V
I_{SNSO}	Current-sensing amplifier output current		Up to 35	mA
V_{SNSP}	Current sensing amplifier non-inverting input voltage	DC	-0.6 to +0.6	V
V_{SNSN}	Current sensing amplifier inverting input voltage	DC	-0.6 to +0.6	V
V_{REF}	Reference voltage		-0.3 to V_{REG3V3}+0.3	V
T_{stg}	Storage temperature		-55 to 150	°C
T_J	Junction temperature		-40 to 150	°C

1. *MOSFETs are based on 100 V technology, the actual supply voltage could be limited by gate driver ratings.*

4.2 ESD characteristics

Table 4. ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2000	V
CDM	Charge Device Model	All pins Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2a	500	V
		Corner pins only Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V

4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_M	Motor supply voltage		7		75	V
V_{CC}	Gate driver supply voltage			14		V
		VM and VCC pin shorted	7		15	V
C_{CC}	VCC regulator output capacitor			4.7		µF
V_{BOOT}	Bootstrap voltage			V_M+V_{CC}		V
C_{BOOT}	Bootstrap capacitor			1		µF
C_{FLY}	Charge pump fly capacitor			220		nF
C_{REG3V3}	REG3V3 capacitor			4.7		µF
C_{SNSO}	Differential amplifier output capacitor				100	pF
V_{IO}	Logic input/output voltage		0		5	V
I_{OD}	Open-drain sink current				4	mA
V_{SNSO}	Current-sensing amplifier output voltage		0		3.3	V
V_{SNSP}	Current-sensing amplifier non-inverting input voltage		0		0.5	V
V_{SNSN}	Current-sensing amplifier inverting input voltage			0		V
V_{REF}	Reference voltage		0		3.3	V
f_{PWM}	PWM frequency	$V_M \geq 15$ V			100	kHz
		$V_M < 15$ V			25	kHz
T_{amb}	Operative ambient temperature		-40		125 (1)	°C

1. *The actual operative range depends on power dissipation and actual junction-ambient thermal resistance of the device in the final application.*

4.4 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(J-CT)}$	Thermal resistance, junction-to-case top	23	°C/W
$R_{th(J-CB)}$	Thermal resistance, junction-to-case bottom	1.4	°C/W

5 Electrical characteristics

Testing conditions: V_M = 48 V, unless otherwise specified.

Typical values are tested at T_J = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the range of -40 to 125 °C, unless otherwise specified

Table 7. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply						
$V_{CC,on}$	VCC supply UVLO turn-on threshold		6.45		7	V
$V_{CC,hyst}$	VCC supply UVLO hysteresis ($V_{CC,on}$ - $V_{CC,off}$)			240		mV
$V_{BO,on}$	Bootstrap supply UVLO turn-on threshold	V_{BO} = V_{BOOT} - V_M	5.8		7	V
$V_{BO,hyst}$	Bootstrap supply UVLO hysteresis ($V_{BO,on}$ - $V_{BO,off}$)			240		mV
V_{REG3V3}	Internal 3.3 V regulator output voltage	I_{SHORT} = 41 mA		3.3		V
I_{Mq}	Overall quiescent consumption from VM	All MOSFETs off No external load on user regulator No load on SNSO R_{OFF} = 12 kΩ, fixed t_{OFF}		4.2		mA
I_{STBY}	Standby current consumption	nSTBY = low, T_J = 25 °C			0.5	µA
		nSTBY = low, full temperature range			1	
$t_{STBY,off}$	Standby to MOSFETs turn-off	See Figure 9		22.5		µs
$t_{STBY,dis}$	MOSFETs turn-off to circuitry disabling	See Figure 9		5		µs
$t_{STBY,on}$	Standby wake-up time	See Figure 9 (1) nSTBY low pulse 1 ms		32		µs
14 V LDO linear regulator						
V_{CC}	14 V linear regulator output			14.2		V
$I_{CC,lim}$	Maximum regulator current			40		mA
Power stage						
$R_{DS(ON),LS}$	Low-side turn-on resistance	10 A version, T_J = 25 °C		16		mΩ
		6 A version, T_J = 25 °C		27		mΩ
		10 A version, full temperature range			36	mΩ
		6 A version, full temperature range			59	mΩ
$R_{DS(ON),HS}$	High-side turn-on resistance	10 A version, T_J = 25 °C		16		mΩ
		6 A version, T_J = 25 °C		27		mΩ
		10 A version, full temperature range			36	mΩ
		6 A version, full temperature range			59	mΩ
t_{dINH}	Input-high to high-side turn-on propagation delay (including DT)	Maximum slew rate 50% IN to 20% OUT		1.6		µs
t_{dINL}	Input-low to low-side turn-on propagation delay (including DT)	Maximum slew rate 50% IN to 80% OUT		1.6		µs

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{on_MOS}	High-side MOSFET turn-on propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 0V, V_M = 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		270		ns
	Low-side MOSFET turn-on propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		280		
	High-side MOSFET turn-on propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 0V, V_M = 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		250		
	Low-side MOSFET turn-on propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		270		
t_{off_MOS}	High-side MOSFET turn-on propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 0V, V_M = 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		850		ns
	Low-side MOSFET turn-on propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		500		
	High-side MOSFET turn-on propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 0V, V_M = 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		850		

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{off_MOS}	Low-side MOSFET turn-on propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ V_{in} = 0 - 3.3 V OUT 500 Ω to 48 V 50% V_{in} to 10 or 90% OUT Max slew rate		480		ns
t_{DT}	Deadtime			1.3		µs
MT	Propagation delay matching	Maximum Slew Rate MT = $\lvert t_{dINH} - t_{dINL} \rvert$			150	ns
t_{dENH}	High-side MOSFET enable propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 0 V, V_M = 48 V 50% EN to 10 or 90% OUT Max slew rate		240		ns
	Low-side MOSFET enable propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 48 V 50% EN to 10 or 90% OUT Max slew rate		260		
	High-side MOSFET enable propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 0 V, V_M = 48 V 50% EN to 10 or 90% OUT Max slew rate		250		
	Low-side MOSFET enable propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 48 V 50% EN to 10 or 90% OUT Max slew rate		270		
t_{dENL}	High-side MOSFET disable propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 0 V, V_M = 48 V 50% EN to 10 or 90% OUT Max slew rate		740		ns
	Low-side MOSFET disable propagation delay	10 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 48 V		425		

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{dENL}		50% EN to 10 or 90% OUT Max slew rate				ns
	High-side MOSFET disable propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 0 V, V_M = 48 V 50% EN to 10 or 90% OUT Max slew rate		760		
	Low-side MOSFET disable propagation delay	6 A version $V_{BOOT} = V_M + V_{CC}$ EN = 0 - 3.3 V OUT 500 Ω to 48 V 50% EN to 10 or 90% OUT Max slew rate		450		
SR_{rise}	Rising slew rate (20% - 80%)	R_{SR} = short to 3.3 V		1		V/ns
		R_{SR} = 44 kΩ		0.5		
		R_{SR} = 22 kΩ		0.3		
		R_{SR} = short to 0 V		0.2		
SR_{fall}	Falling slew rate (80% - 20%)	R_{SR} = short to 3.3 V		1		V/ns
		R_{SR} = 44 kΩ		0.5		
		R_{SR} = 22 kΩ		0.3		
		R_{SR} = short to 0 V		0.2		
Logic input and outputs						
$V_{IL(EN)}$	Low logic input voltage	EN input			0.4	V
$V_{IH(EN)}$	High logic input voltage	EN input	2.55			V
V_{IL}	Low logic input voltage	IN, INH, INL, nSTBY inputs			0.8	V
V_{IH}	High logic input voltage	IN, INH, INL, nSTBY inputs	2.1			V
R_{PDin}	Input pull-down resistor			500		kΩ
V_{OL}	Open drain outputs low logic voltage	I_{SINK} = 4 mA			0.35	V
$I_{H,SR}$	SR current generator			50		µA
Integrated comparator						
$V_{COMP,offset}$	Comparator offset	V_{REF} = 1 V			10	mV
$t_{COMP,delay}$	Propagation delay	V_{REF} = 1 V		240		ns
$t_{COMP,deglitch}$	Deglitch filter			130		ns
Integrated amplifier						
$V_{AMPoffset}$	Amplifier offset	T_J = 25 °C			6	mV
		Full temperature range			7	mV
A_{CL}	Amplifier gain		9.5	10	10.5	V/V
$R_{in,AMP}$	Equivalent input resistance			90		kΩ
V_{SNSOH}	High-level output voltage	V_{SNSP} = 0.36 V		14		mV

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
	(V_{REG3V3} - V_{SNSO})	V_{SNSN} = 0 V I_L = 500 µA				
V_{SNSOL}	Low-level output voltage	I_L = 500 µA		20		mV
$t_{settling}$	Output voltage settling time	V_{in} 150 mV step R_L = 3 kΩ, C_L= 100 pF		150		ns
Current limiter						
$V_{toffDIS}$	PWM trimming mode voltage on TOFF pin				0.2	V
t_{OFF}	Current limiter off time	R_{OFF} = 10 kΩ, C_{OFF} = 0.1 nF		1		µs
		R_{OFF} = 23 kΩ, C_{OFF} = 0.5 nF		10		µs
		R_{OFF} = 630 kΩ, C_{OFF} = 1 nF		550		µs
t_{BLANK}	Blanking time	10 A version, SR short to 3.3 V		1.5		µs
		10 A version, R_{SR} = 44 kΩ		1.9		
		10 A version, R_{SR} = 22 kΩ		2.6		
		10 A version, SR short to 0 V		3.4		
		6 A version, SR short to 3.3 V		1.3		
		6 A version, R_{SR} = 44 kΩ		2.1		
		6 A version, R_{SR} = 22 kΩ		3.2		
		6 A version, SR short to 0 V		4.5		
Open-load detection						
$t_{OLD,refresh}$	Open-load detection refresh time			100		µs
$t_{OLD,check}$	Open-load detection check time			100		µs
$I_{OLD,PD}$	Open-load detection pull-down			2.5	3	mA
V_{OLDL}	Open-load detection low threshold			2.3		V
V_{OLDH}	Open-load detection high threshold			V_M + 2		V
Overcurrent protection						
I_{OC}	Overcurrent threshold	10 A version, T_J = 25 °C	14	22		A
		6 A version, T_J = 25 °C	8	13		
		10 A version, full temperature range	12			A
		6 A version, full temperature range	6			
$V_{RELEASE}$	OC release ENABLE threshold		0.4			V
Thermal shutdown						
T_{SD}	Thermal shutdown threshold (regulator protection)			150		°C
$T_{SD,release}$	Thermal shutdown release threshold (regulator protection)			120		°C
$T_{SD(MOS)}$	Thermal shutdown threshold (MOSFETs protection)		120	130		°C
$T_{SD(MOS),release}$	Thermal shutdown release threshold (MOSFETs protection)		100			°C

1. *The actual time to return to operative condition may depend on settling time of supply voltages (V_{REG3V3}, V_{CC} and V_{BOOT}).*

5.1 Timing diagrams

Figure 6. Propagation delay definition, IN/EN, OUT

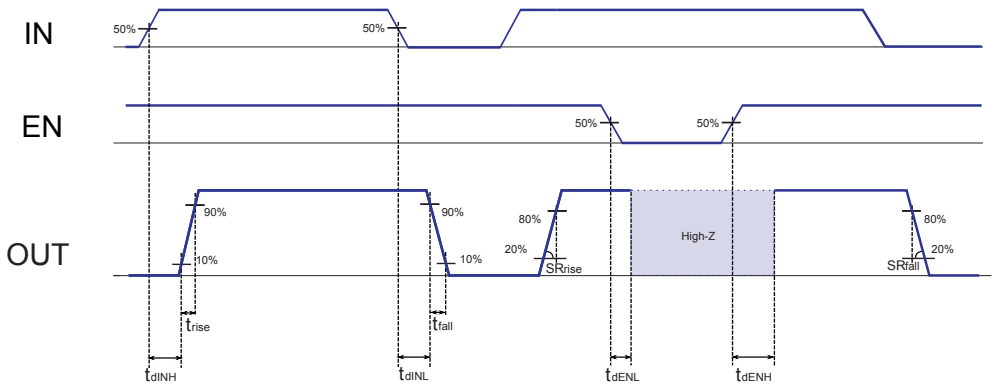


Figure 7. Propagation delay definition, INH/INL, EN, OUT, high-side hard switching

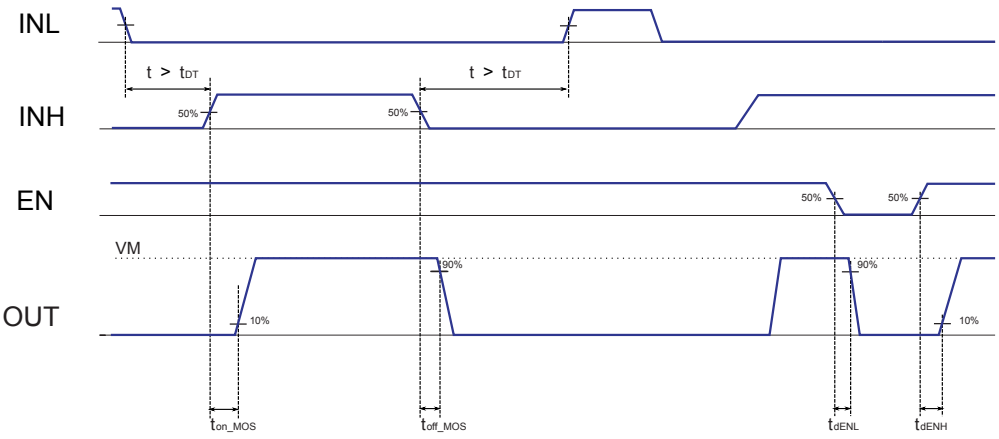
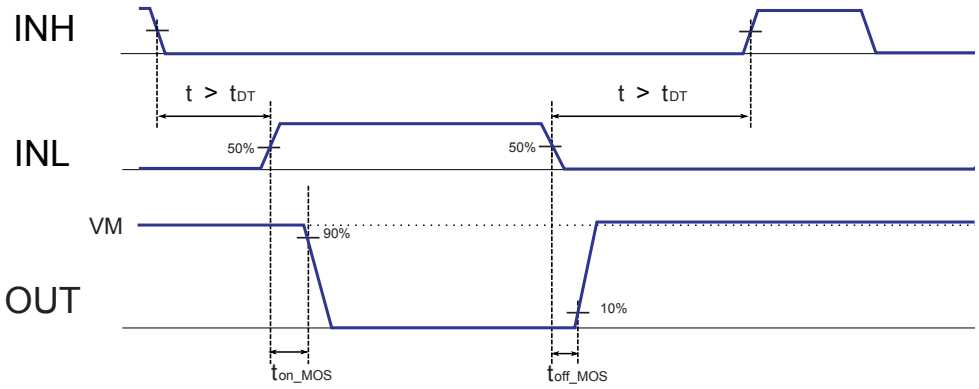


Figure 8. **Propagation delay definition, INH/INL, OUT, low-side hard switching**



6 Control die description

The following sections describe in detail the control-die architecture and the function of its sub-blocks.

6.1 Supply and regulators

The control die integrates three linear regulators generating different supply voltages, starting from the main supply input (VM).

6.1.1 Power-up and power-down

During power-up, all the MOSFETs are kept off, with maximum allowed sink current, until:

- Low-side (V_{CC}) and high-side (V_{BOOT}) gate driver supplies are asserted above respective ULVO thresholds.
- Internal control blocks are properly supplied and operative.

6.1.2 3.3 V regulator (REG3V3)

The control circuitry requires a 3.3 V supply voltage for proper operation. This voltage is internally generated by a linear regulator requiring an external capacitor on the output line.

Note: This regulator cannot be used for supplying external components.

6.1.3 14 V regulator (VCC)

The device integrates a 14 V linear regulator, which generates the gate driver supply (V_{CC}). The regulator has a maximum overall current availability $I_{CC,lim,}$protecting the regulator against short circuit and overload.

Note: This regulator cannot be used for supplying external components.

6.1.4 Charge pump

A charge pump supplies the high-side gate drivers and guarantees 100% duty-cycle operation.

6.1.5 Standby

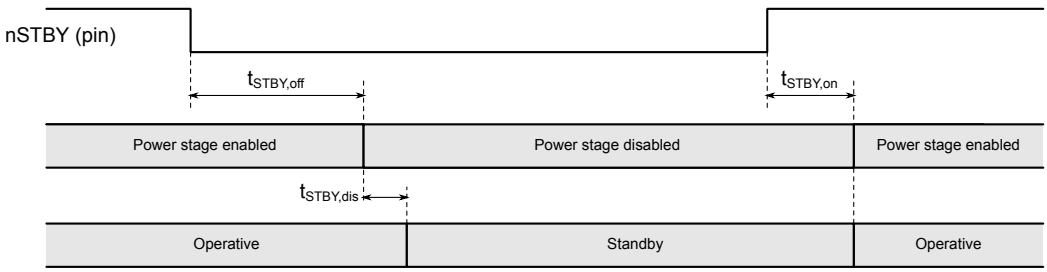
Setting the nSTBY input low disables the power stage and forces the device in low consumption mode (current consumption: I_{STBY}).

In this condition, the following circuits are disabled:

- All internal regulators
- Charge pump
- Gate drivers
- Analog front-end (differential amplifier and comparator)
- All protections

The embedded MOSFETs are kept off by the 100 kΩ pull-down resistor on the gate driver outputs.

Figure 9. Standby



6.2 Control logic

The power stage is controlled using different driving strategies according to the device product code.

Table 8. Half-bridge with EN/IN driving strategy, inputs to output

EN	IN	DECAY (1)	OUT
0	X	X	High impedance
1	0	0	LS on
1	1	0	HS on
1	X	1	LS on

1. *Decay status forced by the current limiter circuit, if enabled. See Section 6.4.1.*

Table 9. Half-bridge with INH/INL driving strategy, inputs to output

EN	INL	INH	DECAY (1)	OUT
0	X	X	X	High impedance
1	0	0	X	High impedance
1	1	0	X	LS on
1	0	1	0	HS on
1	0	1	1	LS on
1	1	1	X	High impedance/Interlocking

1. *Decay status forced by the current limiter circuit, if enabled. See Section 6.4.1.*

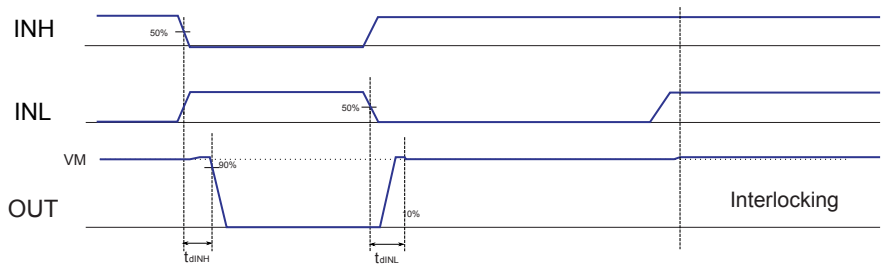
All control inputs of the device have pull-down resistors to avoid unpredictable behaviour in case of pin disconnection.

6.2.1 Dead time

The dead time feature, in companion with interlocking function, ensures that the high-side and low-side MOSFETs of the same channel are not turned ON simultaneously. A minimum dead time is enforced between the turn-off of one gate driver output and the turn-on of its complementary output.

The INH/INL driving mode (see Table 9) allows the user to apply a custom dead time. If the applied dead time is shorter than the internal one, the internal value takes precedence.

Figure 10. Dead time and interlocking, low-side hard switching



6.3 Gate driver

The high-side (HS) and low-side (LS) gate drivers have a similar block diagram:

- A reference pin for the low level (OUT for HS and LSS for LS).
- The output pad (GHS or GLS), directly connected to the gate of the embedded MOSFET.
- The supply pin (BOOT or VCC), fixed and independent of the reference node.

When the control die is disabled (e.g. in standby mode or not supplied), an equivalent 100 kΩ resistor ensures that the MOSFETs remain off.

The driver source current and turn-on timing are set to change the output slew rate among four values: for each slew rate, a pair of current and timing is selected based on the characteristics of the embedded MOSFET.

The sink current and turn-off timing are set only according to the integrated power MOSFETs targeting a fast turn-off. Turning off the MOSFETs with the maximum current allows for minimizing the dead time duration.

The voltage on the SR pin is set through an external pull-down resistor combined with an integrated pull-up.

Figure 11. Slew rate (SR) selection circuit

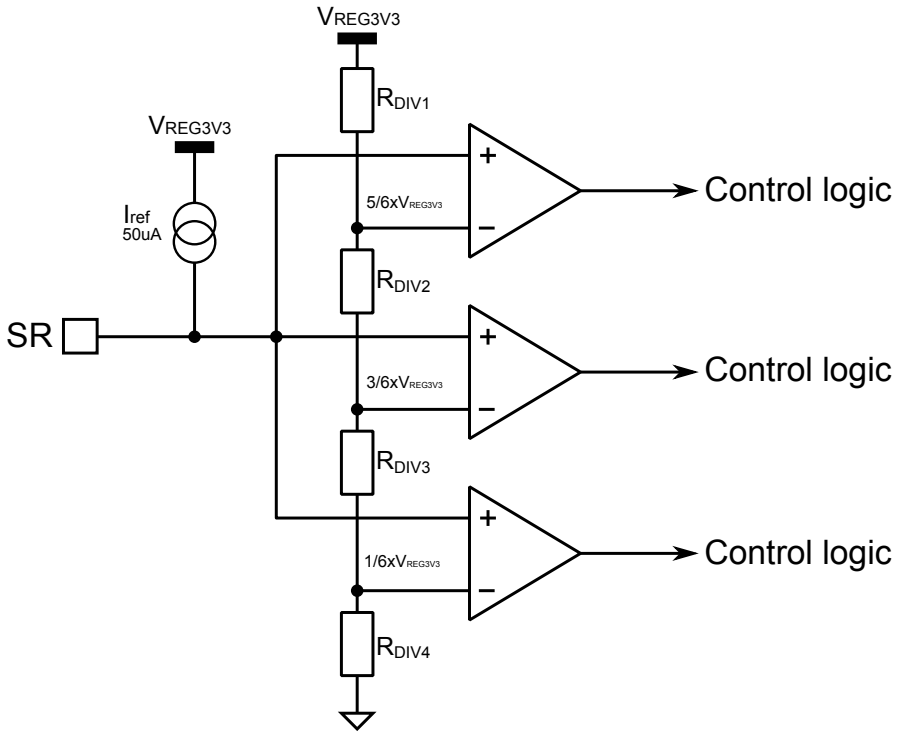


Table 10. Slew rate selection

V_{SR}	R_{SR} (± 5%)	Output slew rate (typ) at V_M = 48 V	t_{rise} / t_{fall}
$V_{SR} > 5/6 \times V_{REG3V3}$	Short REG3V3	1 V/ns	50 ns
$3/6 \times V_{REG3V3} < V_{SR} < 5/6 \times V_{REG3V3}$	44 kΩ	0.5 V/ns	100 ns
$1/6 \times V_{REG3V3} < V_{SR} < 3/6 \times V_{REG3V3}$	22 kΩ	0.3 V/ns	150 ns
$V_{SR} < 1/6 \times V_{REG3V3}$	Short GND	0.2 V/ns	200 ns

6.4 Current sensing amplifier and comparator

The control die integrates one differential amplifier with a fixed gain factor of A_{CL} designed to amplify the signal from an external shunt resistor.

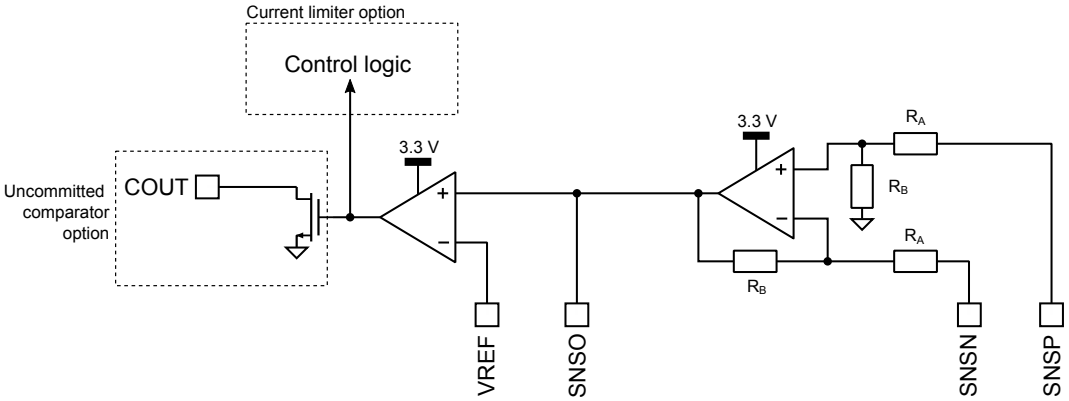
The differential voltage between SNSP (non-inverting input) and SNSN (inverting input) is amplified and available on the SNSO output.

The same signal is internally connected to the non-inverting input of a comparator, which according to the ordering code, is at user disposal or dedicated to a current limiting feature (see Section 6.4.1).

In the first case (uncommitted comparator), the result of the comparison is available on the COUT open-drain output with an inverted logic: when amplifier output is greater than VREF voltage, COUT is forced low.

In both cases, the inverting input of the comparator is available on the VREF input pin.

Figure 12. Embedded amplifier and comparator



It is possible to filter the amplifier output connecting to a small capacitor on the SNSO pin. This affects the comparator input as well.

6.4.1 Current limiter

When the amplifier and the comparator are dedicated to the current limiter feature, the voltage drop of an external shunt resistor connected between SNSP and SNSN is amplified by A_{CL} and compared with the reference voltage (V_{REF}).

When $V_{SNSO} > V_{REF}$, the comparator triggers, and the device operates according to the selected decay strategy.

Two current limiter modes are available:

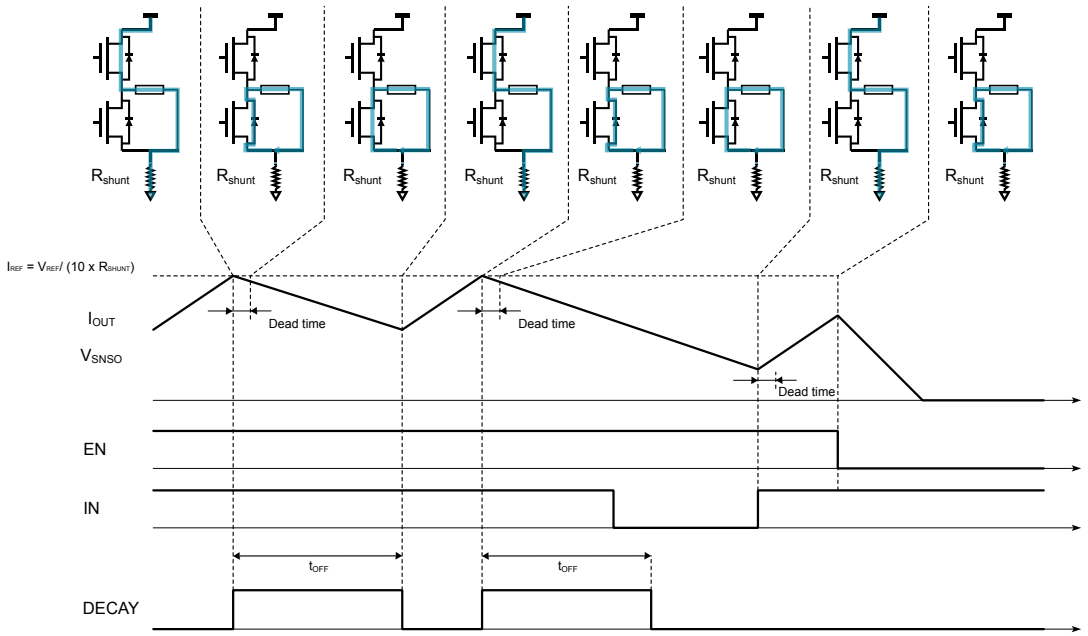
- Fixed OFF time (RC network on the TOFF pin)
- PWM trimming (TOFF pin shorted to ground)

To avoid spurious triggering of the current limiter, a blanking signal is applied to the comparator output during each power-stage commutation.

6.4.1.1 *Fixed OFF time*

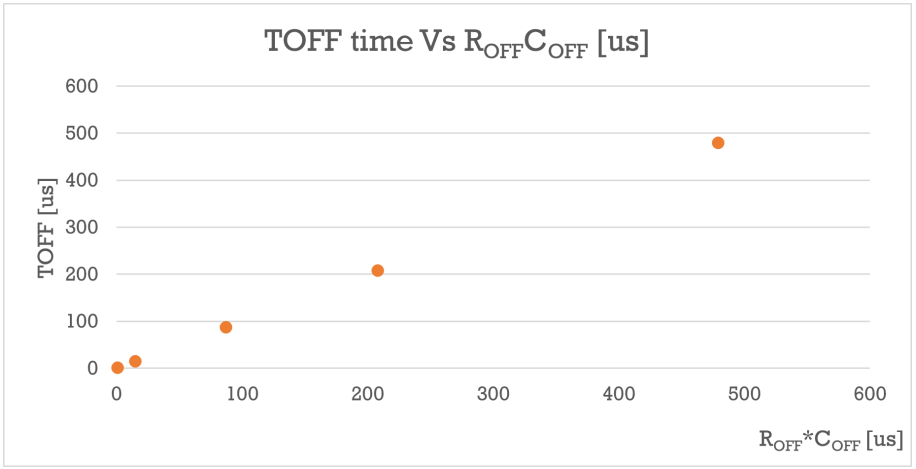
In fixed off time mode, when the comparator is triggered, the control circuitry sets the device in decay status for a t_{off} time.

Figure 13. Fixed OFF time current limiter



This timing is adjusted through an RC network connected to the TOFF pin as shown in Figure 14.

Figure 14. t_{OFF} vs. R_{OFF}- C_{OFF} network

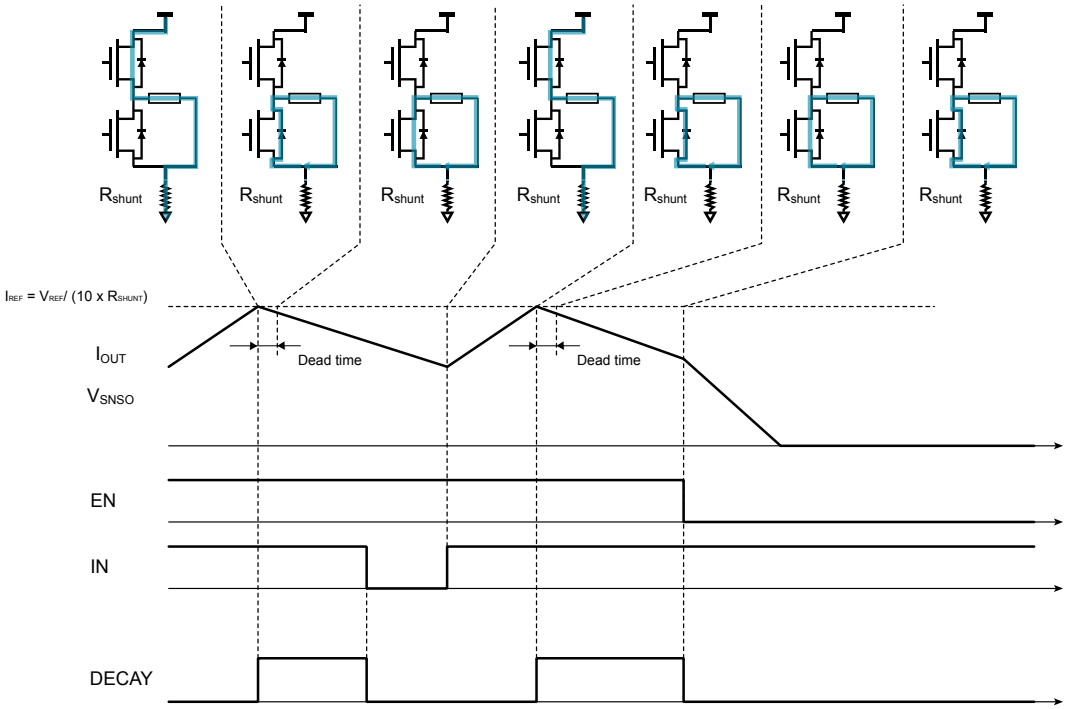


6.4.1.2 *PWM trimming mode*

PWM trimming mode is activated by shorting the TOFF pin to ground. When the comparator is triggered, the control circuitry sets the device in decay status until one of the following conditions occurs:

- Half-bridge device with EN/IN driving strategy: EN is forced low or IN is forced low.
- Half-bridge device with INH/INL driving strategy: EN is forced low, INH is forced low or INL is forced high.

Figure 15. PWM trimming current limiter



6.5 Open-load detection

The control die integrates open-load detection circuitry.

If an open-load failure condition is asserted, the nOL pin is forced low until one of the following conditions is met:

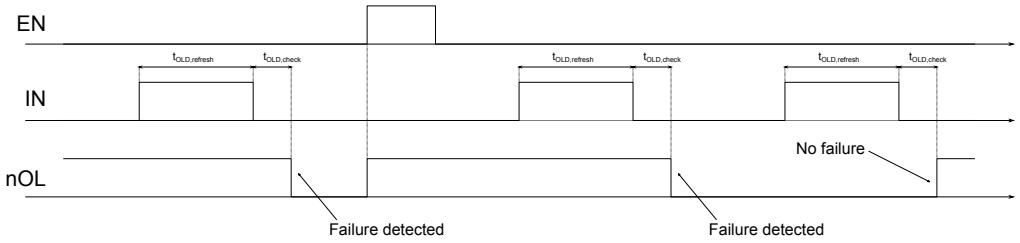
- The bridge is enabled (i.e. leaving high impedance condition).
- The bridge successfully passes the next open-load check.

Note: The open-load failure does not interfere with normal operation.

In the device, an open-load test is performed when:

- EN/IN case: the EN signal is low and a positive pulse of $t_{OLD,refresh}$ is applied on the IN input (see Figure 16).
- INH/INL case: the EN signal is low and a positive pulse of $t_{OLD,refresh}$ is applied on the INH input.

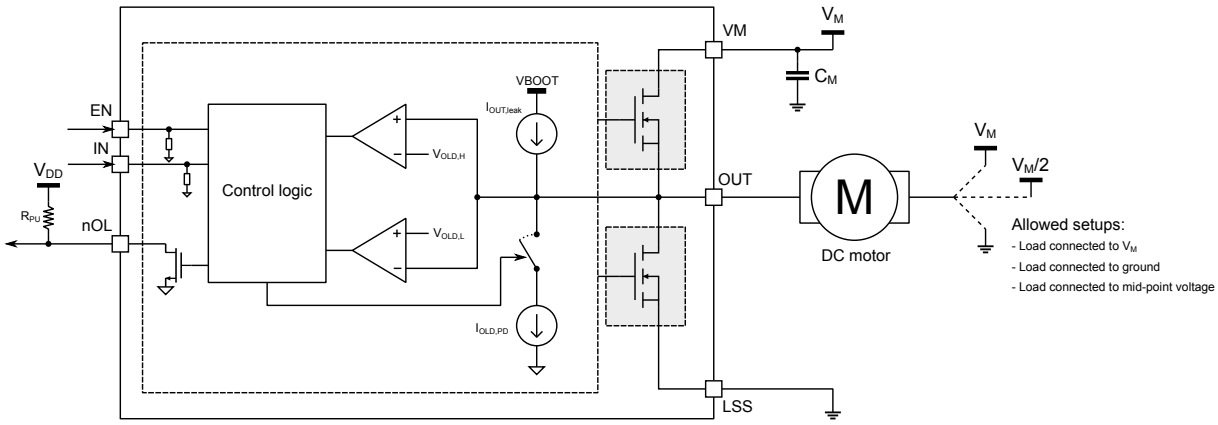
Figure 16. Open-load test triggering - EN/IN version



The test is performed as follows:

1. The output voltage is checked in accordance with the following cases:
   a. The voltage is above $V_{OLD,H}$.
   b. The voltage is below $V_{OLD,L}$.
   c. The voltage is neither above $V_{OLD,H}$ nor below $V_{OLD,L}$.
2. A pull-down current $I_{OLD,PD}$ is applied to the output and the output voltage is checked again.

Figure 17. Open-load detection



The result of the two checks, which is available after $t_{OLD,check}$, defines the open-load condition assortment.

Table 11. Open-load detection test result

	Check 1 (pull-up)		
Check 2 (pull-down)	$V_{OUT} > V_{OLD,H}$	$V_{OLD,L} < V_{OUT} < V_{OLD,H}$	$V_{OUT} < V_{OLD,L}$
$V_{OUT} > V_{OLD,H}$	**OK** (load shorted to VM)	FAIL (Anomalous)	FAIL (Anomalous)
$V_{OLD,L} < V_{OUT} < V_{OLD,H}$	**OK** (weak pull-up)	**OK** (unipolar driving)	FAIL (Anomalous)
$V_{OUT} < V_{OLD,L}$	FAIL (open-load)	**OK** (weak pull-down)	**OK** (load shorted to GND)

6.6 Protections

The device integrates several protections as listed in Table 12.
All protections force the nFAULT output low until they are released.

Table 12. Protection summary table

Protection	Triggering condition	Effect	Release condition
V_{CC} UVLO	$V_{CC} < V_{CC,off}$	Power stage disabled	$V_{CC} \geq V_{CC,on}$
Control die overtemperature	$T_{J,control} > T_{SD}$	Power stage disabled VCC regulator and charge pump off	$T_{J,control} \leq T_{SD,release}$
V_{BOOT} UVLO	$V_{BOOT} - V_M < V_{BO,off}$	HS MOSFET off LS MOSFET driven according to inputs	$V_{BOOT} - V_M \geq V_{BO,on}$
V_{DS} monitoring	V_{DS} of one MOSFET > $V_{DS,th}$	Power stage disabled	EN input forced low ($V_{EN} < V_{RELEASE}$)
MOSFETs' overtemperature	$T_{J,MOS} > T_{SD}$	Power stage disabled	$T_{J,MOS} \leq T_{SD,release}$

6.6.1 Overcurrent protection (V_{DS} monitoring)

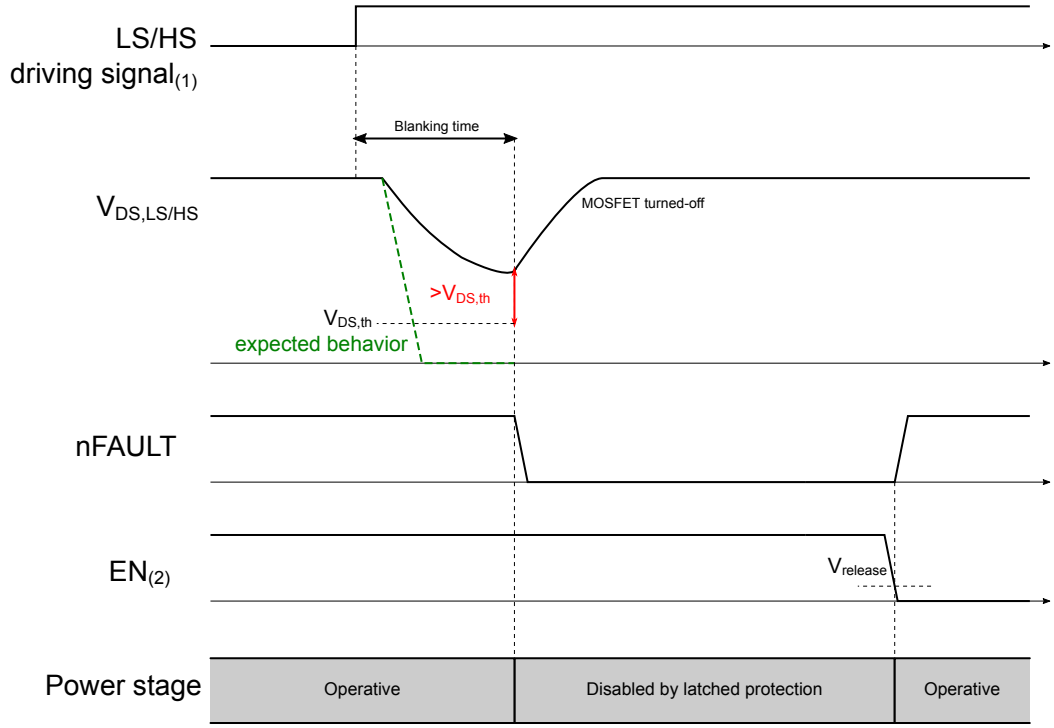
The control die constantly monitors the drain-source drop of each power MOSFET: $V_M - V_{OUT}$ for the high-side, and $V_{OUT} - V_{SLS}$ for the low-side.

When a power MOSFET is expected to be on (i.e. at the end of the turn-on phase), and its drain-source drop exceeds the $V_{DS,th}$ threshold, an overcurrent condition is triggered. This forces the power stage into a safe state and pulls the nFAULT output low.

The safe condition is achieved by turning off all MOSFETs using a reduced turn-off current to limit the dI/dt and avoid critical overshoots or undershoots below ground on the switching node.

The control die keeps the MOSFETs off until normal operation is restored by forcing the EN input low ($V_{EN} < V_{RELEASE}$).

Figure 18. Overcurrent protection



(1) According to specific driving option
(2) In ENx/INx option, both the EN1 and EN2 must be forced low.

6.6.2 Undervoltage lockout protection (UVLO)

Undervoltage lockout protection (UVLO) is present on the following supplies:

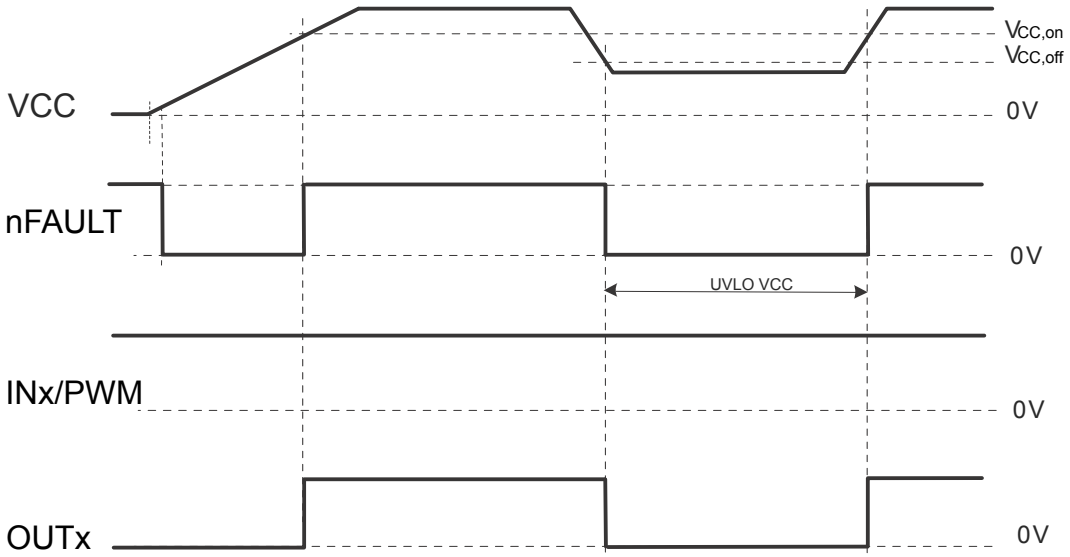
- Low-side gate driver supply (V_{CC})
- High-side gate driver supply (V_{BOOT}– V_M)

During power-up, UVLO is released when the supply exceeds its respective “on” threshold. After power-up, the UVLO is triggered when the supply falls below its respective “off” threshold and is released again once the supply rises above the “on” threshold.

Deglitch filtering on the protection comparators prevents spurious triggering due to internally generated or externally coupled noises.

When at least one of the supplies is in UVLO condition, the power stage is forced into a safe state (i.e. all MOSFETs turned off), and the nFAULT output is forced low.

Figure 19. UVLO protection on VCC power supply



6.6.3 Thermal shutdown

Each MOSFET in the system-in-package is protected against overtemperature by a dedicated temperature sensor located in the driver die (one sensor per MOSFET). When the measured temperature of any MOSFET is above the safe threshold $T_{SD(MOS)}$, the control die turns off the power stage until the temperature of all MOSFETs is below $T_{SD(MOS),release}$.

A temperature monitoring circuit is also present in the control die. If the measured temperature is above the safe threshold T_{SD}, the VCC regulator and the charge pump are turned off until the temperature returns below $T_{SD,release}$.

In both cases, the nFAULT output is forced low.

7 Package information

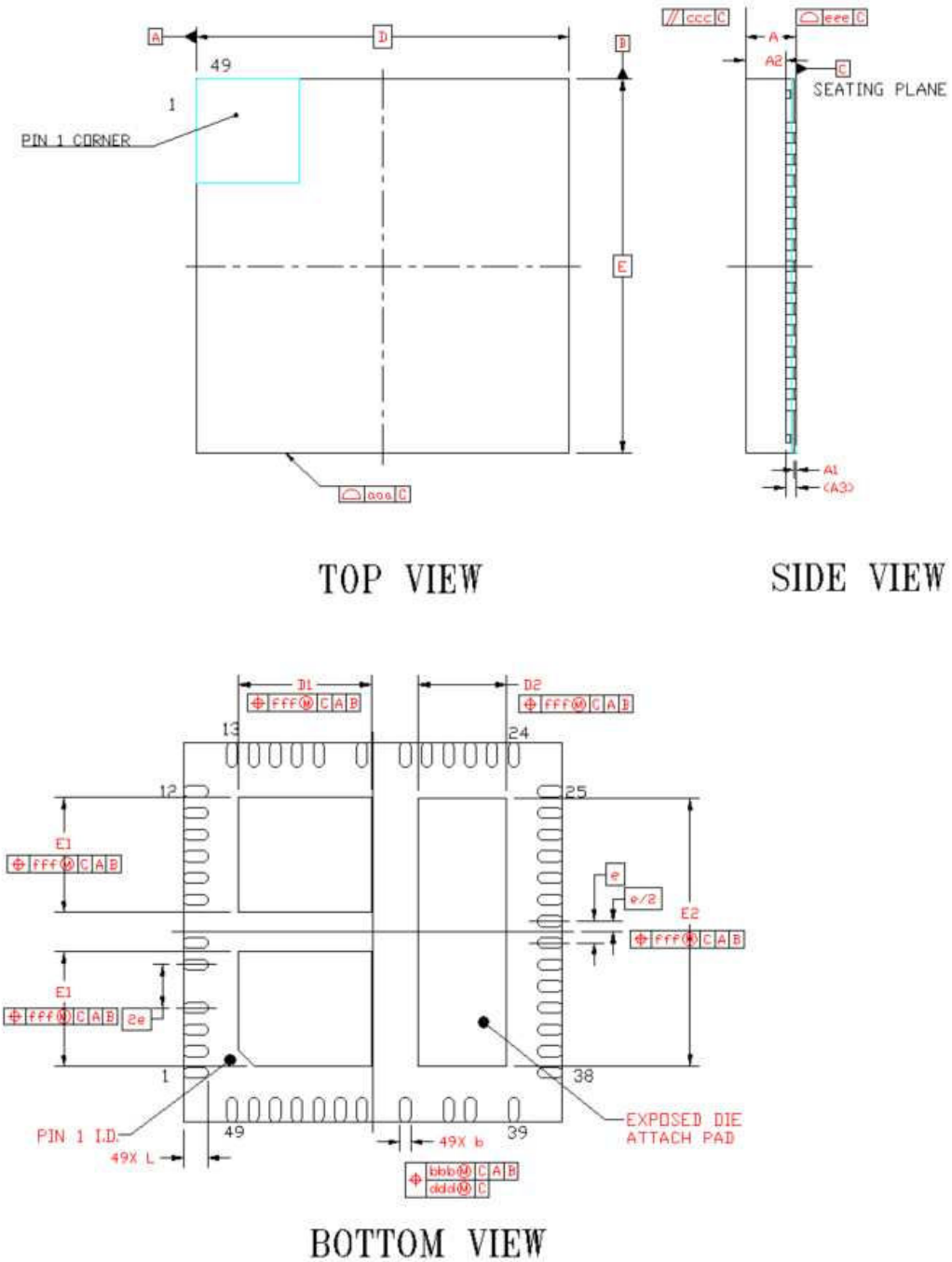
To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 VFQFPN 7x7x1.0 mm 49L pitch 0.4 package information

Table 13. Package mechanical data

Symbol	Min.	Nom.	Max.
	[mm]		
A	0.90	0.95	1.00
A1	0.00	0.035	0.05
A2	-	0.75	-
A3	0.203 REF.		
b	0.15	0.2	0.25
D	7.00 BSC		
D1	2.36	2.46	2.56
D2	1.54	1.64	1.74
E	7.00 BSC		
E1	2.02	2.12	2.22
E2	4.84	4.94	5.04
L	0.35	0.45	0.55
e	0.4 BSC		
Tolerance			
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.1		

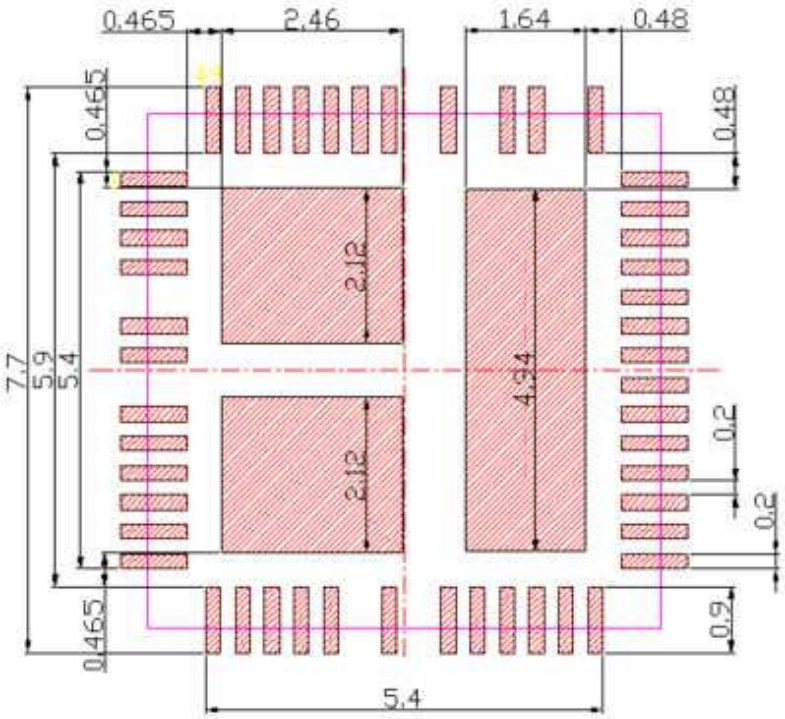
Figure 20. **Package outline**



7.2 Suggested footprint

The STSPIN9P1 footprint for the PCB layout is typically defined based on multiple design factors, such as assembly plant technology capabilities and board component density. For easy device usage and evaluation, ST provides the following footprint design, which is suitable for a wide range of PCBs.

Figure 21. Suggested footprint



8 Ordering information

Table 14. **Order code**

Order code	Package	Package marking	Packing
STSPIN9P11	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P11	Tape and reel
STSPIN9P12	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P12	Tape and reel
STSPIN9P13	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P13	Tape and reel
STSPIN9P14	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P14	Tape and reel
STSPIN9P15	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P15	Tape and reel
STSPIN9P16	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P16	Tape and reel
STSPIN9P17	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P17	Tape and reel
STSPIN9P18	VFQFPN 7x7x1.0 mm 49L pitch 0.4	SPIN9P18	Tape and reel

Revision history

Table 15. **Document revision history**

Date	Version	Changes
12-Sep-2025	1	Initial release.

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