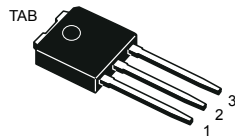
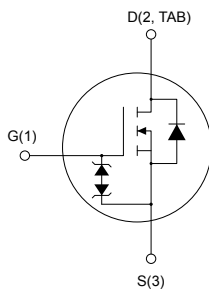


N-channel 800 V, 3.5 Ω typ., 2 A MDmesh K5 Power MOSFET in an IPAK package


IPAK


AM01476v1_tab


Product status link
[STU2N80K5](#)
Product summary

Order code	STU2N80K5
Marking	2N80K5
Package	IPAK
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STU2N80K5	800 V	4.5 Ω	2 A

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	8	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$.
3. $V_{DS} \leq 640\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.78	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	100	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	0.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	60.5	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 800\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 800\text{ V}$, $V_{GS} = 0\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			50	
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$		3.5	4.5	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	105	-	pF
C_{oss}	Output capacitance		-	8	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }640\text{ V}$	-	16	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	7	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	18	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}$, $I_D = 2\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	5	-	nC
Q_{gs}	Gate-source charge		-	1	-	nC
Q_{gd}	Gate-drain charge		-	3.7	-	nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 1\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	8	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	19	-	ns
t_f	Fall time		-	32	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	255		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	1		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	8		A
t_{rr}	Reverse recovery time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	285		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	1.45		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	7.5		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

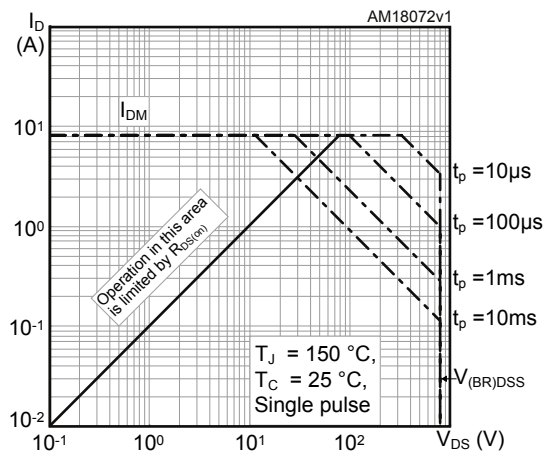


Figure 2. Thermal impedance

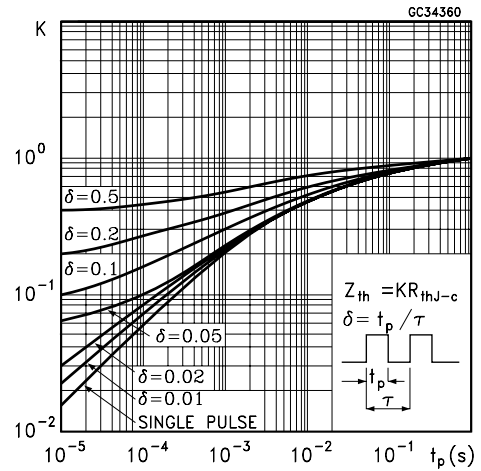


Figure 3. Output characteristics

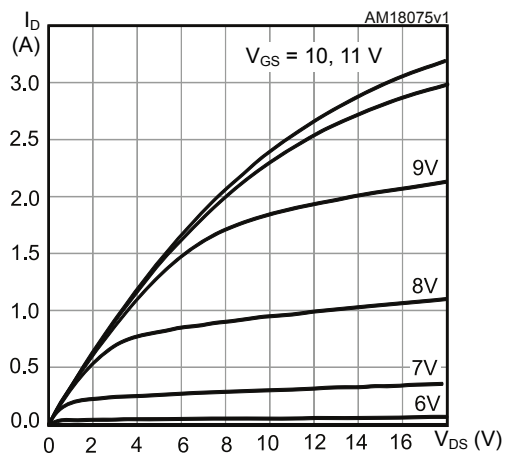


Figure 4. Transfer characteristics

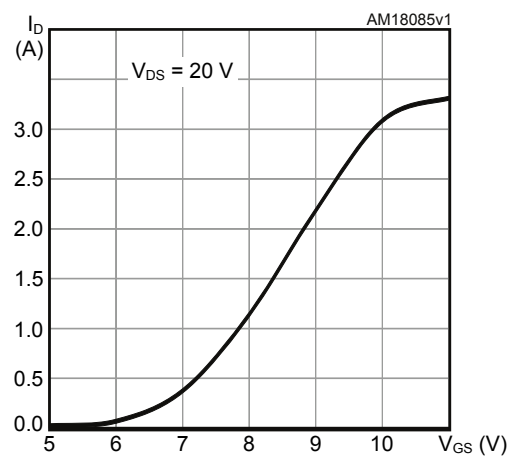


Figure 5. Gate charge vs gate-source voltage

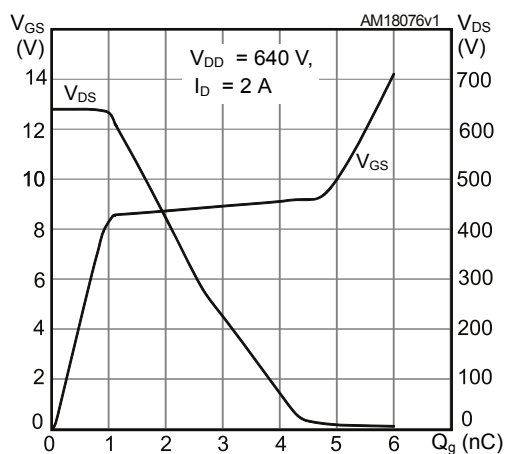


Figure 6. Static drain-source on-resistance

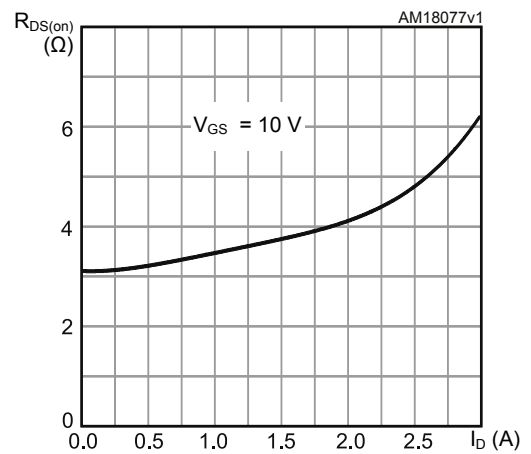


Figure 7. Capacitance variations

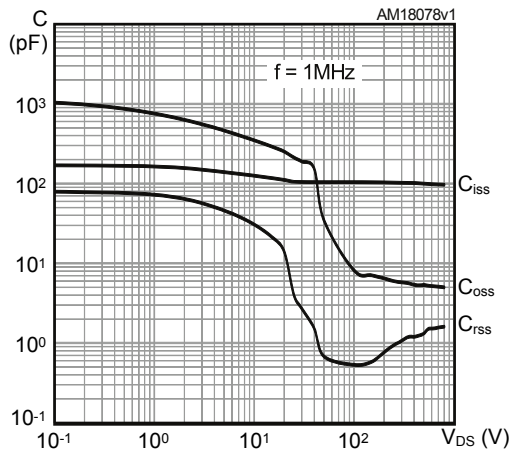


Figure 8. Output capacitance stored energy

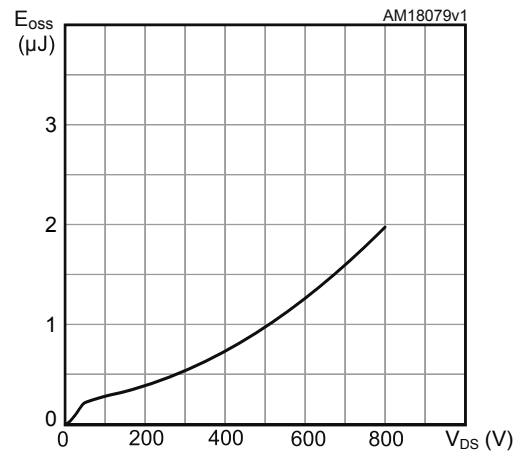


Figure 9. Normalized gate threshold voltage vs temperature

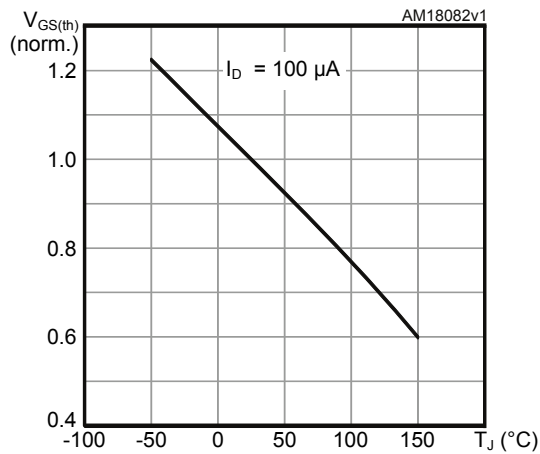


Figure 10. Normalized on-resistance vs temperature

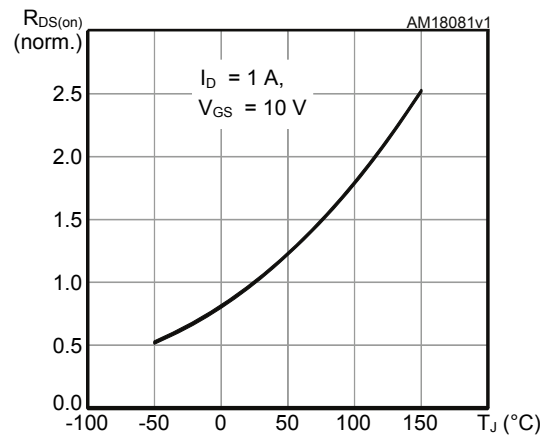


Figure 11. Normalized V_{(BR)DSS} vs temperature

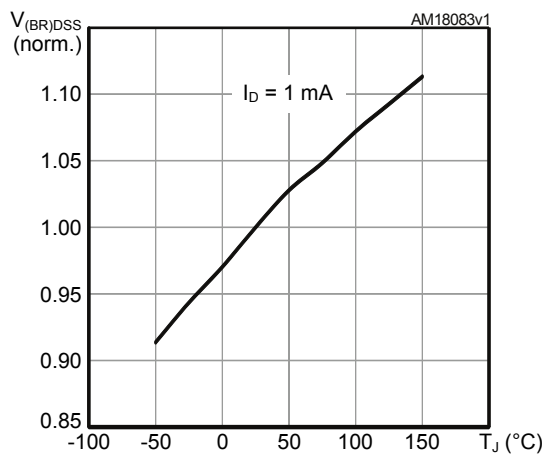


Figure 12. Source-drain diode forward characteristics

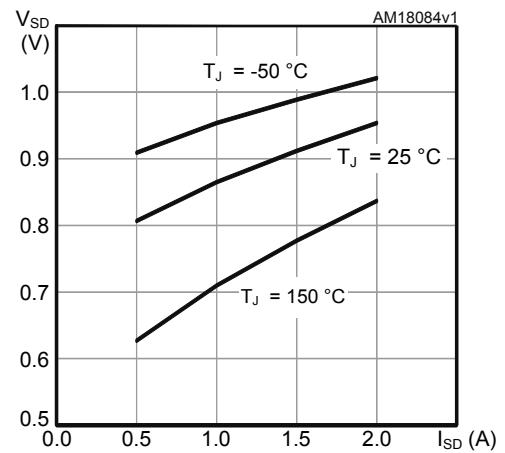
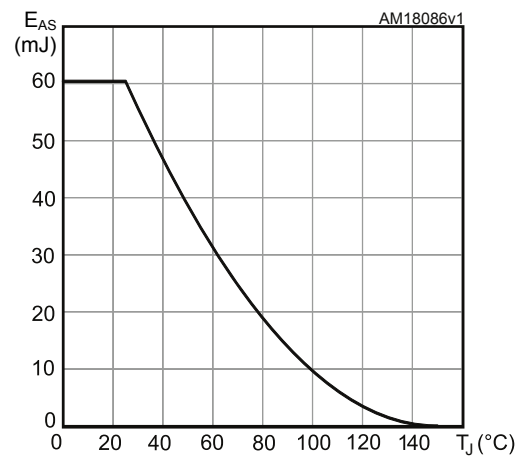
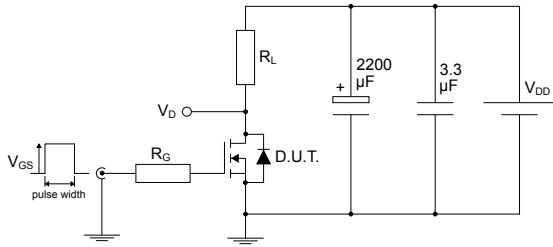


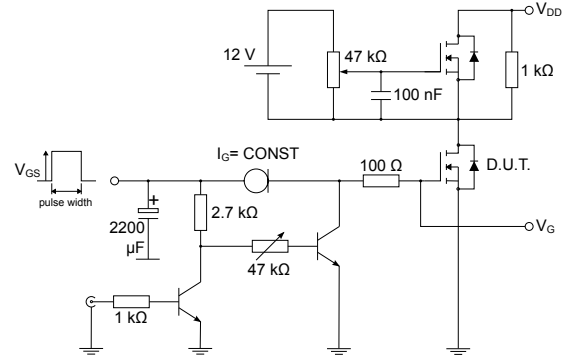
Figure 13. Maximum avalanche energy vs starting T_J



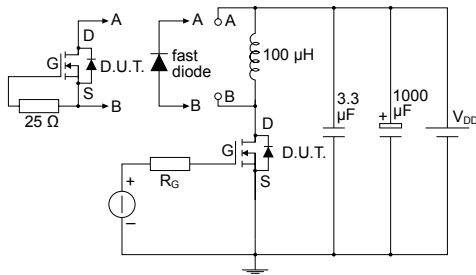
3 Test circuits

Figure 14. Test circuit for resistive load switching times


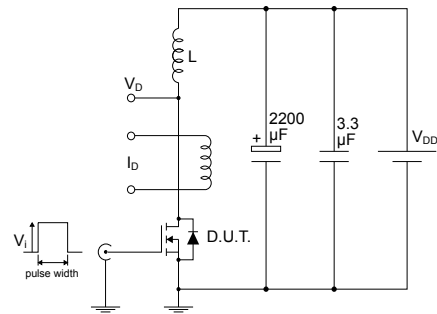
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Figure 15. Test circuit for gate charge behavior


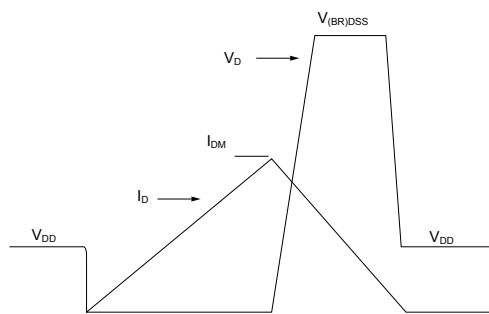
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Figure 16. Test circuit for inductive load switching and diode recovery times


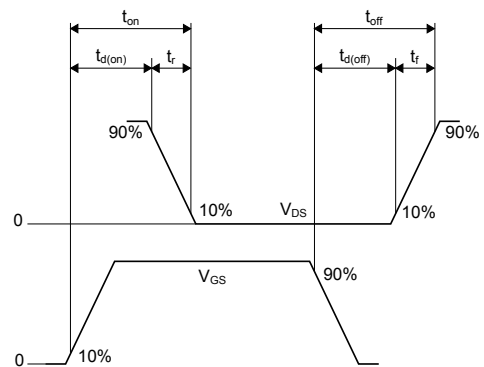
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


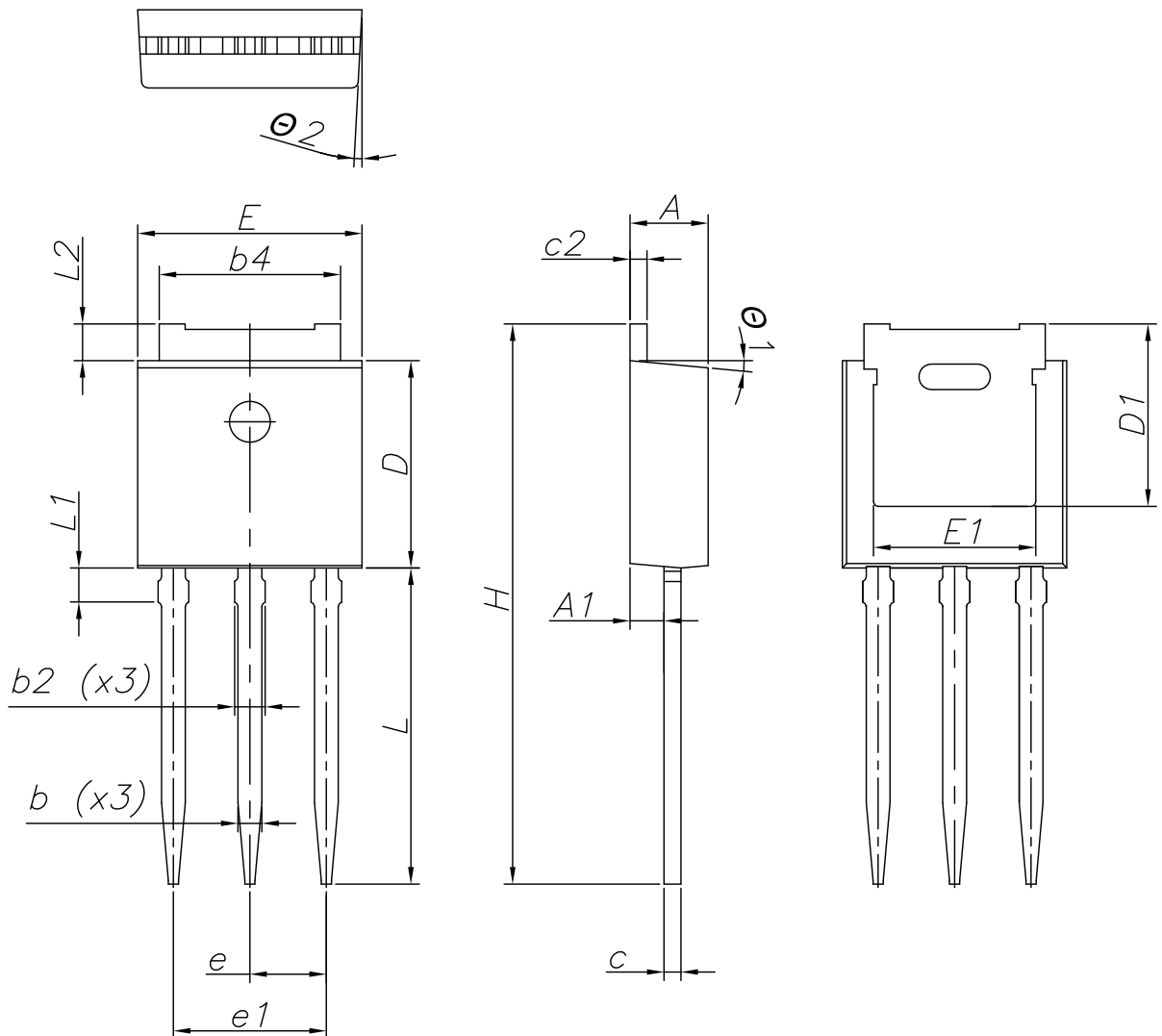
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type C package information

Figure 20. IPAK (TO-251) type C package outline



0068771_IK_typeC_rev16

Table 8. IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Jul-2013	1	First release.
18-Feb-2014	2	<ul style="list-style-type: none"> – Added: IPAK package – Modified: EAS value in <i>Table 2</i> – Modified: Rthj-case in <i>Table 3</i> – Modified: typical values in <i>Table 5, 6 and 7</i> – Added: <i>Section 2.1: Electrical characteristics (curves)</i> – Updated: <i>Figure 25, 26 and Table 9</i> – Added: <i>Table 12 and Figure 29</i> – Minor text changes
25-Sep-2015	3	<ul style="list-style-type: none"> – Updated title, features and description in cover page. – Updated <i>Figure 10, Figure 11 and Section 4: Package information.</i> – Minor text changes.
24-Nov-2023	4	<p>The part numbers STP2N80K5, STF2N80K5 and STD2N80K5 have been moved to a separate datasheet and the document has been updated accordingly.</p> <p>Removed "<i>Table 8. Gate-source Zener diode</i>".</p> <p>Replaced "<i>Section 4.4 IPAK (TO-251) type A package information</i>" with Section 4.1 IPAK (TO-251) type C package information.</p> <p>Minor text changes.</p>

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