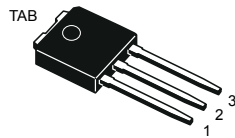
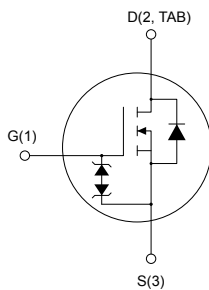


## N-channel 950 V, 4.2 $\Omega$ typ., 2 A MDmesh K5 Power MOSFET in an IPAK package


**IPAK**


AM01476v1\_tab


**Product status link**
[STU2N95K5](#)
**Product summary**

|                   |           |
|-------------------|-----------|
| <b>Order code</b> | STU2N95K5 |
| <b>Marking</b>    | 2N95K5    |
| <b>Package</b>    | IPAK      |
| <b>Packing</b>    | Tube      |

### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|------------|----------|-------------------|-------|
| STU2N95K5  | 950 V    | 5 $\Omega$        | 2 A   |

- Industry's lowest  $R_{DS(on)}$  x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter   | Value      | Unit             |
|----------------|---|------------|------------------|
| $V_{GS}$       | Gate-source voltage   | $\pm 30$   | V                |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 2          | A                |
|                | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 1.3        |                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)  | 8          | A                |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$     | 45         | W                |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                               | 4.5        | V/ns             |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                       | 50         | V/ns             |
| $T_{stg}$      | Storage temperature range                                       | -55 to 150 | $^\circ\text{C}$ |
| $T_J$          | Operating junction temperature range                            |            | $^\circ\text{C}$ |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 2\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ .
3.  $V_{DS} \leq 760\text{ V}$ .

**Table 2. Thermal data**

| Symbol     | Parameter                               | Value | Unit                      |
|------------|---|-------|---------------------------|
| $R_{thJC}$ | Thermal resistance, junction-to-case    | 2.78  | $^\circ\text{C}/\text{W}$ |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | 100   | $^\circ\text{C}/\text{W}$ |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter  | Value | Unit |
|----------|--|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)                                  | 1     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 50    | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off-state**

| Symbol        | Parameter                         | Test conditions   | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|---|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                   | 950  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{DS} = 950\text{ V}$ , $V_{GS} = 0\text{ V}$                               |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{DS} = 950\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$ |      |      | 50       |               |
| $I_{GSS}$     | Gate body leakage current         | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$                            |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                            | 3    | 4    | 5        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 1\text{ A}$                                   |      | 4.2  | 5        | $\Omega$      |

1. Specified by design, not tested in production.

**Table 5. Dynamic**

| Symbol            | Parameter                             | Test conditions   | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|---|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$  | -    | 105  | -    | pF       |
| $C_{oss}$         | Output capacitance                    |   | -    | 9    | -    | pF       |
| $C_{rss}$         | Reverse transfer capacitance          |   | -    | 0.5  | -    | pF       |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }760\text{ V}$   | -    | 16   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related |   | -    | 6    | -    | pF       |
| $R_g$             | Intrinsic gate resistance             | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$   | -    | 16   | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 760\text{ V}$ , $I_D = 2\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 10   | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    |   | -    | 1.5  | -    | nC       |
| $Q_{gd}$          | Gate-drain charge                     |   | -    | 8    | -    | nC       |

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 475\text{ V}$ , $I_D = 1\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$    | -    | 8.5  | -    | ns   |
| $t_r$        | Rise time           |   | -    | 13.5 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 20.5 | -    | ns   |
| $t_f$        | Fall time           |   | -    | 32.5 | -    | ns   |

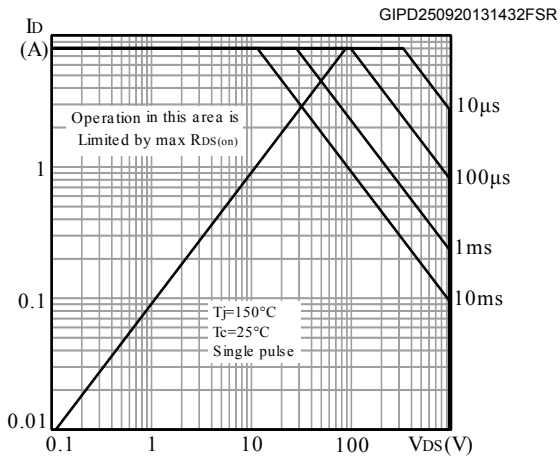
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions   | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|---|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |   | -    |      | 2    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |   | -    |      | 8    | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 2\text{ A}$ , $V_{GS} = 0\text{ V}$                                       | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,                        | -    | 300  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       | $V_{DD} = 60\text{ V}$  | -    | 1.15 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 7.6  |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,                        | -    | 525  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       | $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$                          | -    | 1.90 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 7.2  |      | A             |

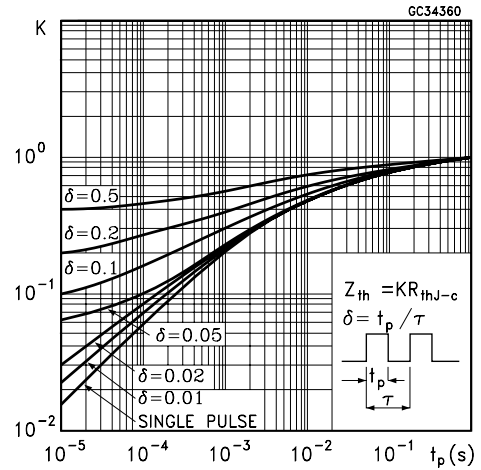
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

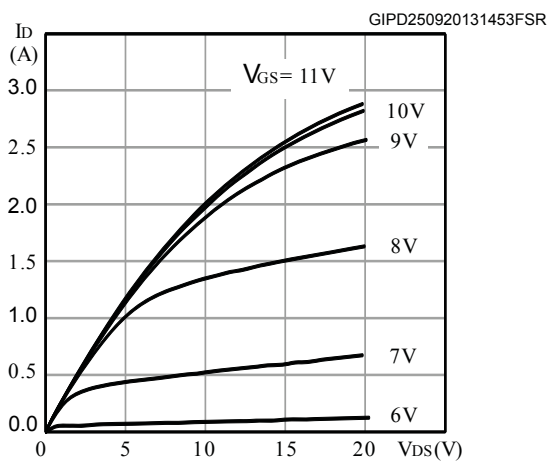
**Figure 1. Safe operating area**



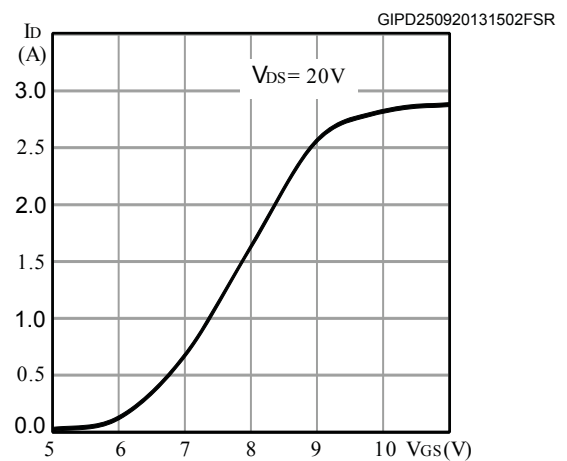
**Figure 2. Normalized transient thermal impedance**



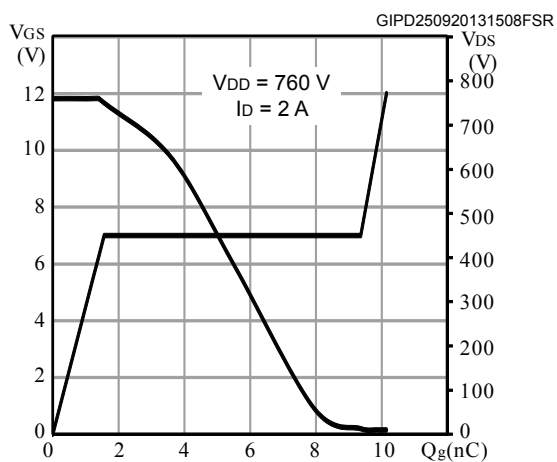
**Figure 3. Typical output characteristics**



**Figure 4. Typical transfer characteristics**



**Figure 5. Typical gate charge characteristics**



**Figure 6. Typical drain-source on-resistance**

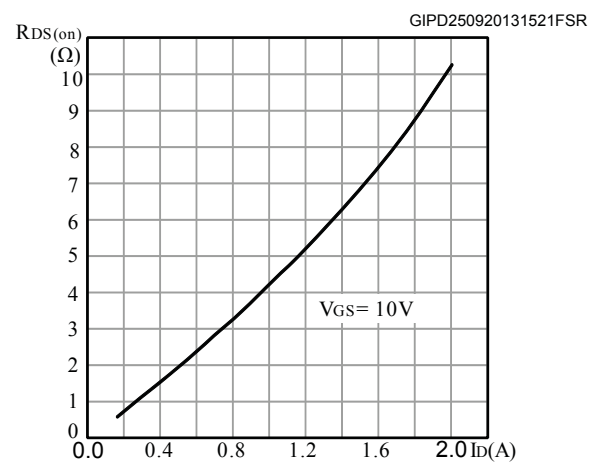


Figure 7. Typical capacitance characteristics

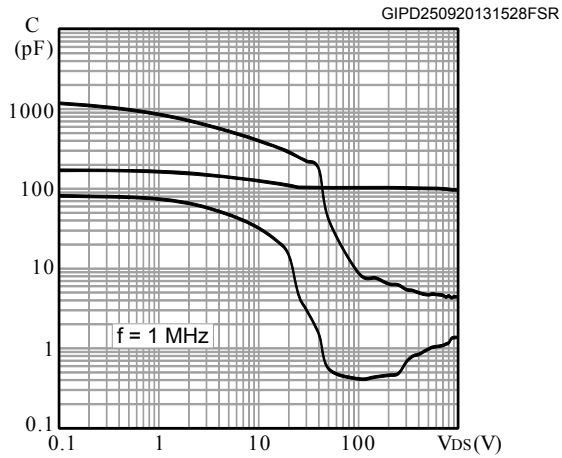


Figure 8. Output capacitance stored energy

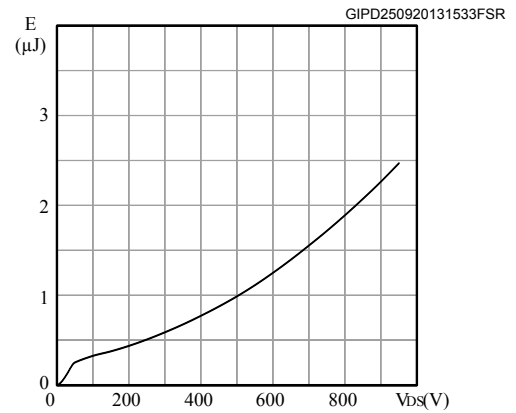


Figure 9. Normalized gate threshold vs temperature

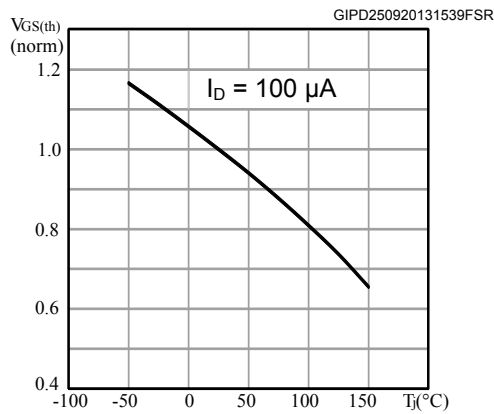


Figure 10. Normalized on-resistance vs temperature

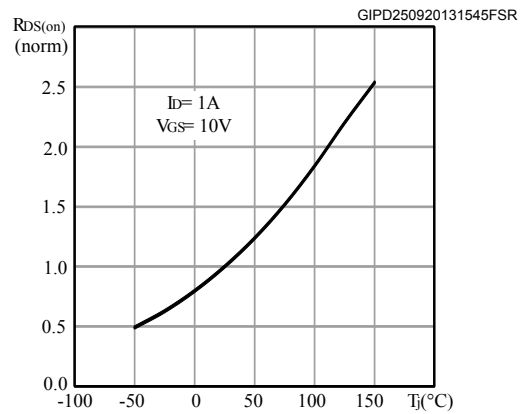


Figure 11. Normalized breakdown voltage vs temperature

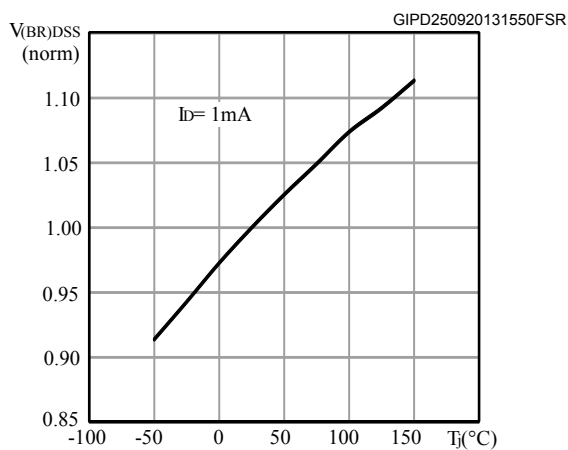
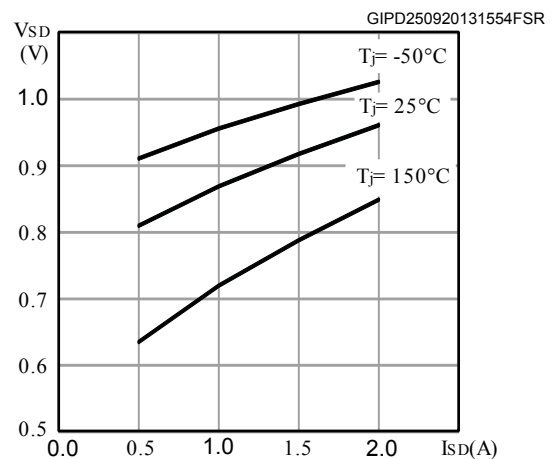


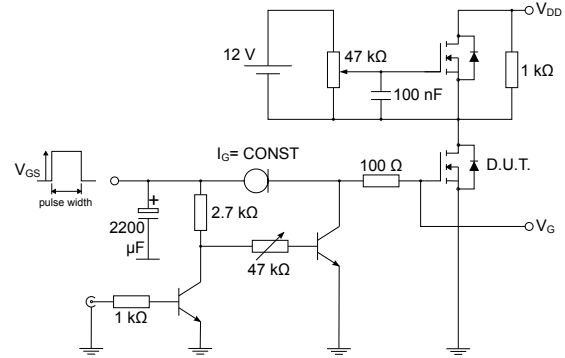
Figure 12. Typical reverse diode forward characteristics



### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


AM01468v1

**Figure 14. Test circuit for gate charge behavior**


AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**

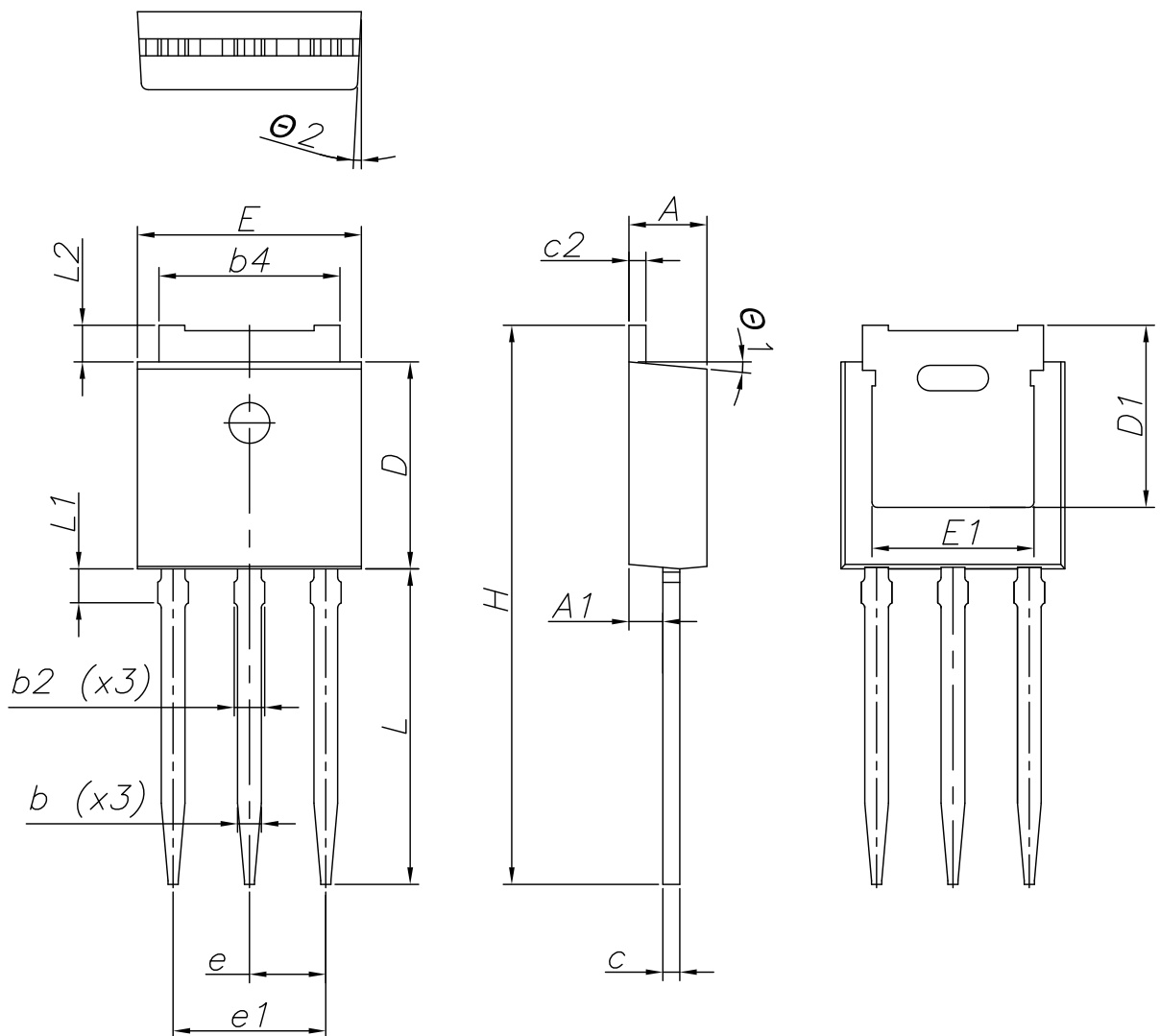

AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 IPAK (TO-251) type C package information

Figure 19. IPAK (TO-251) type C package outline



0068771\_IK\_typeC\_rev16



**Table 8. IPAK (TO-251) type C package mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 2.20  | 2.30  | 2.35  |
| A1   | 0.90  | 1.00  | 1.10  |
| b    | 0.66  |       | 0.79  |
| b2   |       |       | 0.90  |
| b4   | 5.23  | 5.33  | 5.43  |
| c    | 0.46  |       | 0.59  |
| c2   | 0.46  |       | 0.59  |
| D    | 6.00  | 6.10  | 6.20  |
| D1   | 5.20  | 5.37  | 5.55  |
| E    | 6.50  | 6.60  | 6.70  |
| E1   | 4.60  | 4.78  | 4.95  |
| e    | 2.20  | 2.25  | 2.30  |
| e1   | 4.40  | 4.50  | 4.60  |
| H    | 16.18 | 16.48 | 16.78 |
| L    | 9.00  | 9.30  | 9.60  |
| L1   | 0.80  | 1.00  | 1.20  |
| L2   | 0.90  | 1.08  | 1.25  |
| θ1   | 3°    | 5°    | 7°    |
| θ2   | 1°    | 3°    | 5°    |

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 25-Sep-2013 | 1        | First release.   |
| 23-Nov-2023 | 2        | The part numbers STD2N95K5, STF2N95K5 and STP2N95K5 have been moved to separate datasheets and the document has been updated accordingly.<br>Removed Gate-source Zener diode table<br>Updated <a href="#">Section 4 Package information</a> .<br>Minor text changes. |

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