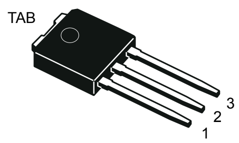
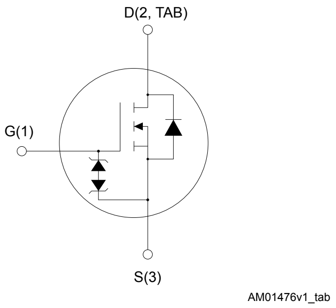
STU3N45K3

Datasheet

N-channel 450 V, 3.3 Ω typ., 1.8 A MDmesh K3 Power MOSFET in an IPAK package



IPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STU3N45K3	450 V	4 Ω	1.8 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status link
STU3N45K3

Product summary	
Order code	STU3N45K3
Marking	3N45K3
Package	IPAK
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	450	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	1.8	A
	Drain current (continuous) at T_C = 100 °C	1	
I_{DM} (1)	Drain current (pulsed)	7.2	A
P_{TOT}	Total power dissipation at T_C = 25 °C	27	W
ESD	Gate-source human body model (R=1.5 kΩ, C=100 pF)	1	kV
dv/dt (2)	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 1.8 A, di/dt ≤ 400 A/μs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	4.63	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	100	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	0.9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	60	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	450			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 450 V			1	µA
		V_{GS} = 0 V, V_{DS} = 450 V, T_C = 125 °C (1)			50	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.6 A		3.3	4	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	164	-	pF
C_{oss}	Output capacitance		-	17	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss(er)}$ (1)	Equivalent output capacitance energy related	V_{DS} = 0 to 360 V, V_{GS} = 0 V	-	18	-	pF
$C_{oss(tr)}$ (2)	Equivalent output capacitance time related		-	13	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	8	-	Ω
Q_g	Total gate charge	V_{DD} = 360 V, I_D = 1.8 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	9.4	-	nC
Q_{gs}	Gate-source charge		-	1.8	-	nC
Q_{gd}	Gate-drain charge		-	6.1	-	nC

1. *$C_{oss(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{oss(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 225 V, I_D = 0.9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	6.5	-	ns
t_r	Rise time		-	5.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	17	-	ns
t_f	Fall time		-	22	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.6	A
I_{SDM} (1)	Source-drain current (pulsed)		-		2.4	A
V_{SD} (2)	Forward on voltage	I_{SD} = 0.6 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 1.8 A, di/dt = 100 A/µs V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	175		ns
Q_{rr}	Reverse recovery charge		-	550		nC
I_{RRM}	Reverse recovery current		-	6		A
t_{rr}	Reverse recovery time	I_{SD} = 1.8 A, di/dt = 100 A/µs V_{DD} = 60 V, T_J = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	185		ns
Q_{rr}	Reverse recovery charge		-	600		nC
I_{RRM}	Reverse recovery current		-	6.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

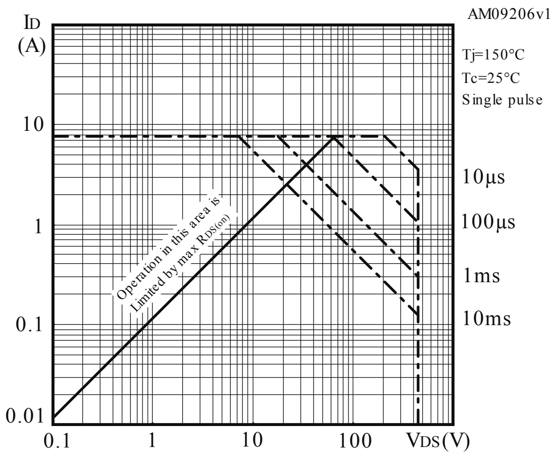


Figure 2. Normalized transient thermal impedance

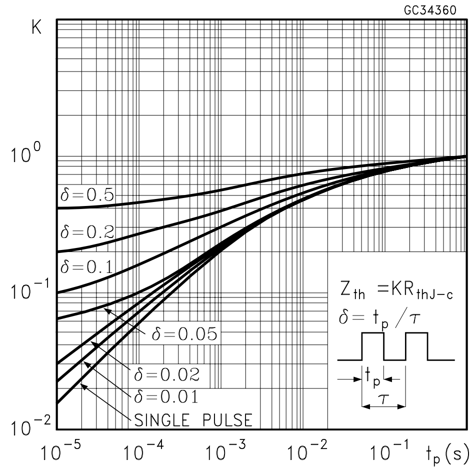


Figure 3. Typical output characteristics

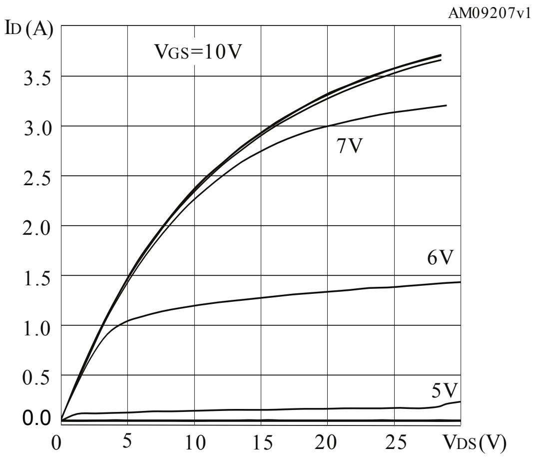


Figure 4. Typical transfer characteristics

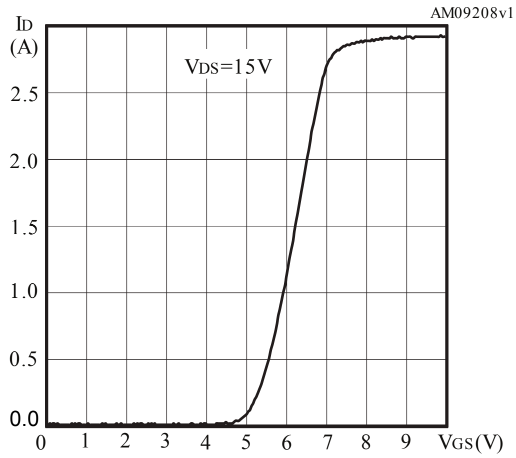


Figure 5. Typical gate charge characteristics

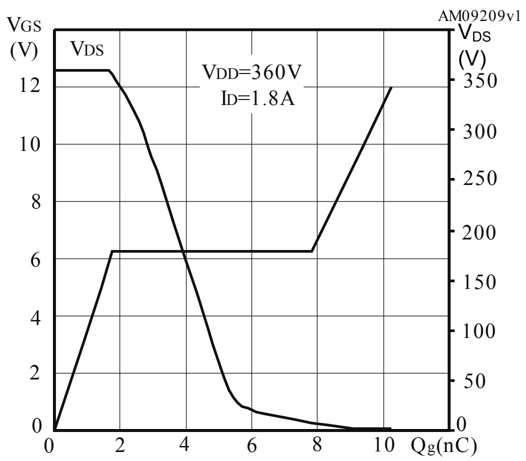


Figure 6. Typical drain-source on-resistance

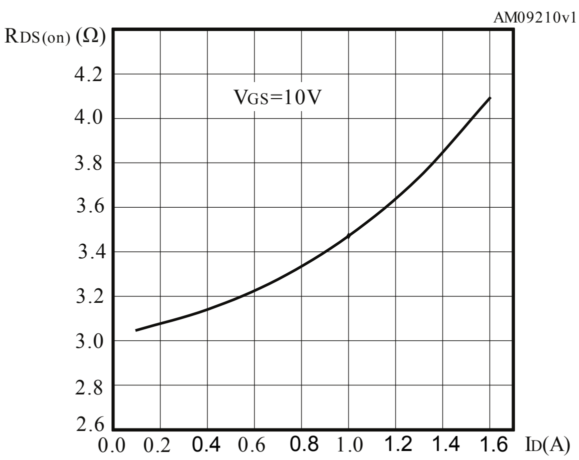


Figure 7. Typical capacitance characteristics

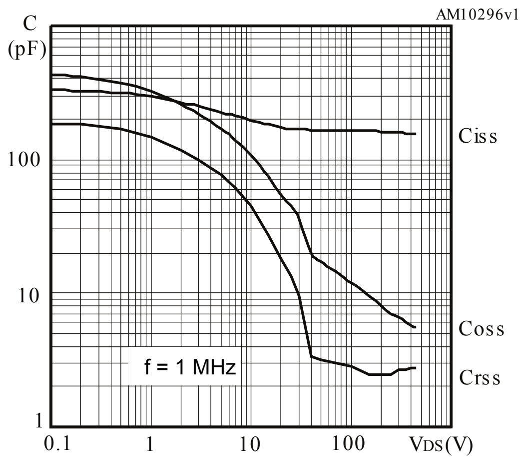


Figure 8. Typical output capacitance stored energy

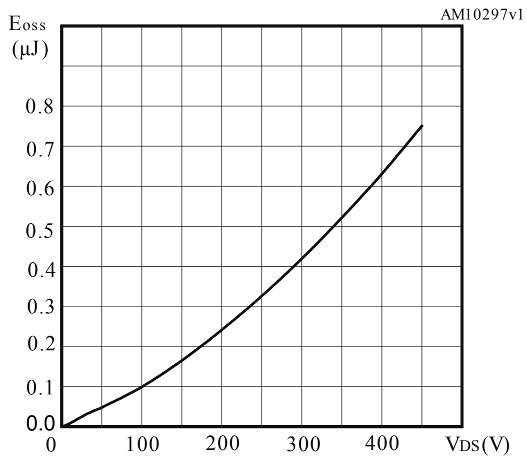


Figure 9. Normalized gate threshold vs temperature

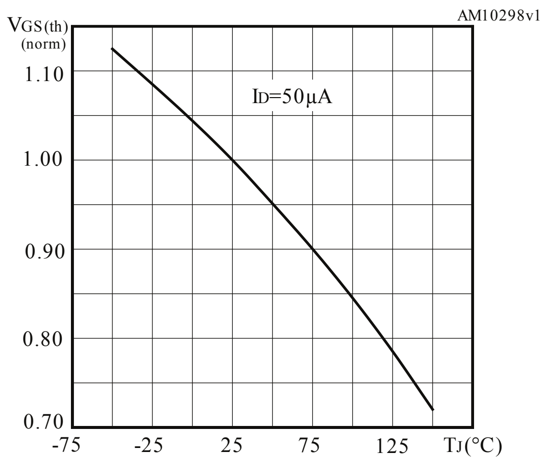


Figure 10. Normalized on-resistance vs temperature

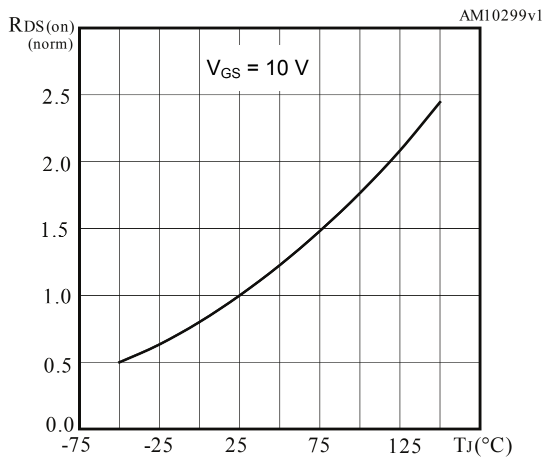


Figure 11. Normalized breakdown voltage vs temperature

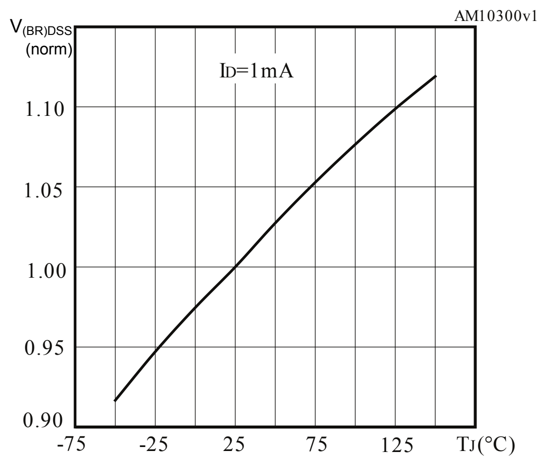


Figure 12. Typical reverse diode forward characteristics

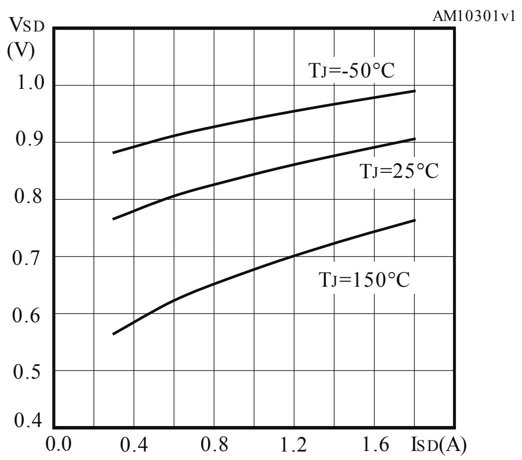
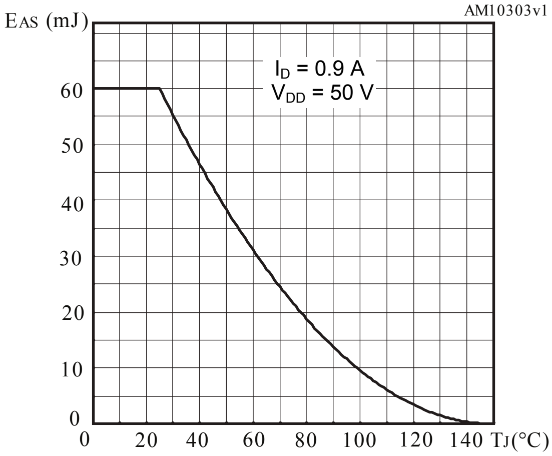


Figure 13. **Maximum avalanche energy vs temperature**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

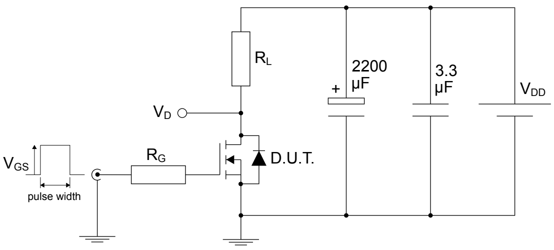


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Figure 15. Test circuit for gate charge behavior

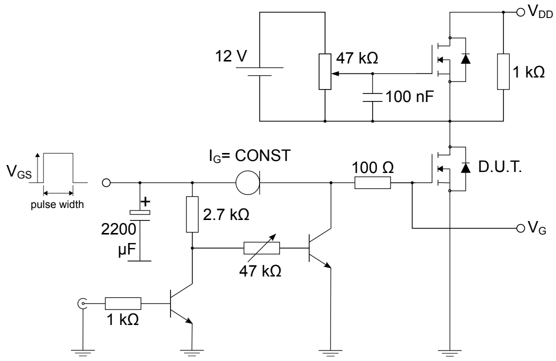

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Figure 16. Test circuit for inductive load switching and diode recovery times

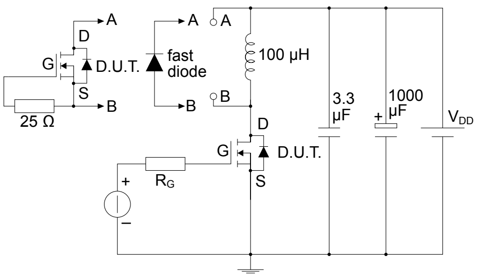

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Figure 17. Unclamped inductive load test circuit

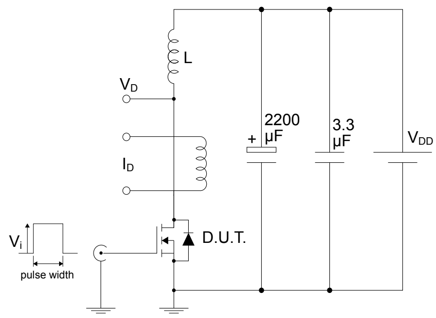

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Figure 18. Unclamped inductive waveform

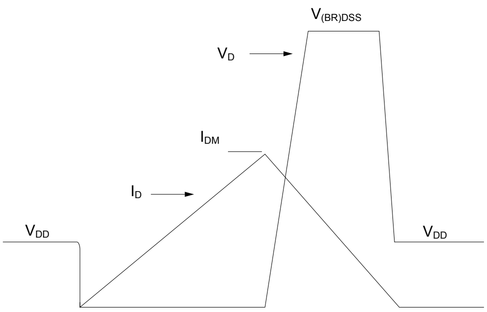

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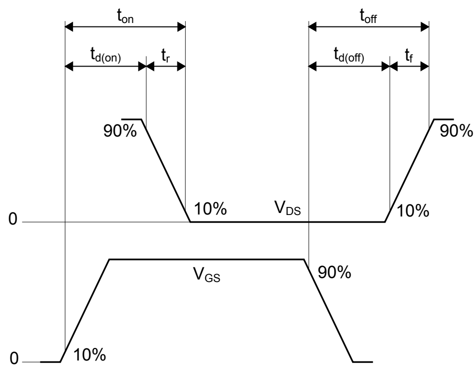
Figure 19. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type C package information

Figure 20. **IPAK (TO-251) type C package outline**

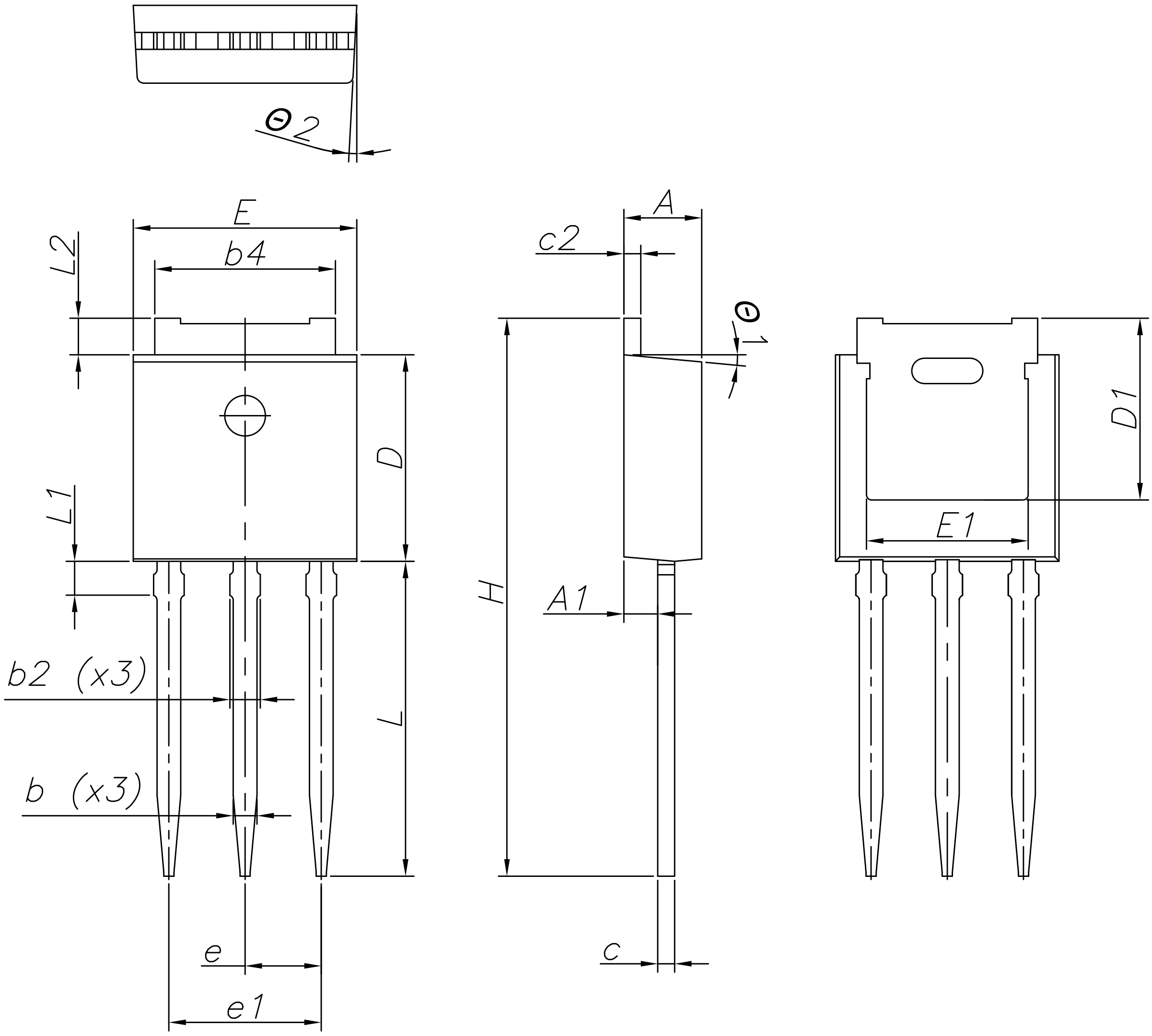

Table 8. IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
02-Mar-2010	1	First release.
23-Apr-2010	2	Changed root part number.
24-Jun-2013	3	– Part numbers STN3N45K3 and STQ3N45K3-AP have been moved to two separate datasheets – Modified: *Description* and *Figure 1* in cover page – Modified: Vesd(g-s) value – Updated: *Section 4: Package mechanical data*
27-Nov-2023	4	Updated Table 5. Dynamic. Updated Section 4 Package information. Minor text changes.

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