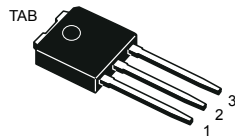
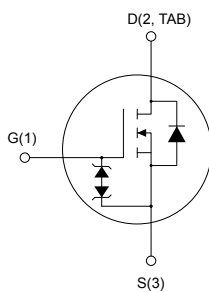


## N-channel 620 V, 1.28 $\Omega$ typ., 4.2 A MDmesh K3 Power MOSFET in an IPAK package


**IPAK**


AM01476v1\_tab


**Product status link**
[STU5N62K3](#)
**Product summary**

<b>Order code</b>	STU5N62K3
<b>Marking</b>	5N62K3
<b>Package</b>	IPAK
<b>Packing</b>	Tube

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STU5N62K3	620 V	1.6 $\Omega$	4.2 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	620	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4.2	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	
$I_{DM}^{(1)}$	Drain current (pulsed)	16.8	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12	V/ns
$di/dt^{(2)}$	Diode reverse recovery current slope	400	A/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 4.2\text{ A}$ ,  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.79	$^\circ\text{C/W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	100	$^\circ\text{C/W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width is limited by $T_J$ max.)	4.2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	120	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	620			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 620\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 620\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2.1\text{ A}$		1.28	1.6	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	680	-	pF
$C_{oss}$	Output capacitance		-	50	-	pF
$C_{rss}$	Reverse transfer capacitance		-	8	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }496\text{ V}$ , $V_{GS} = 0\text{ V}$	-	16.6	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 496\text{ V}$ , $I_D = 4.2\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	26	-	nC
$Q_{gs}$	Gate-source charge		-	4	-	nC
$Q_{gd}$	Gate-drain charge		-	16	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$ , $I_D = 4.2\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	12	-	ns
$t_r$	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	40	-	ns
$t_f$	Fall time		-	21	-	ns

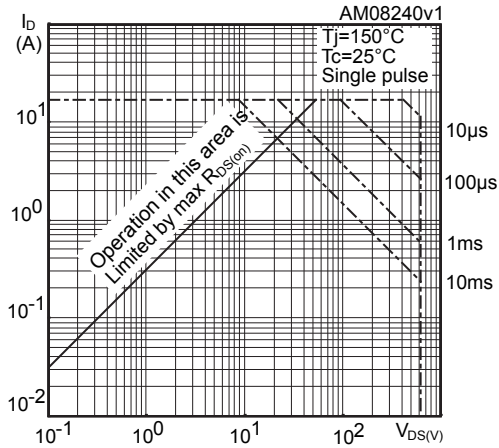
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.2 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.2 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	290		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	1.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.2 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	320		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$	-	2.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	14		A

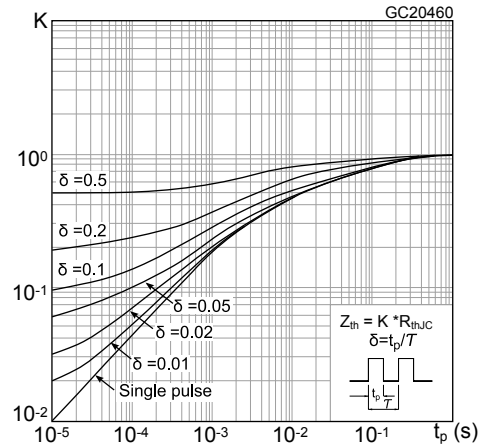
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

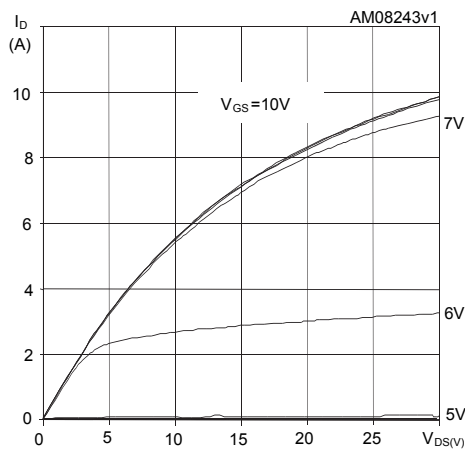
**Figure 1. Safe operating area**



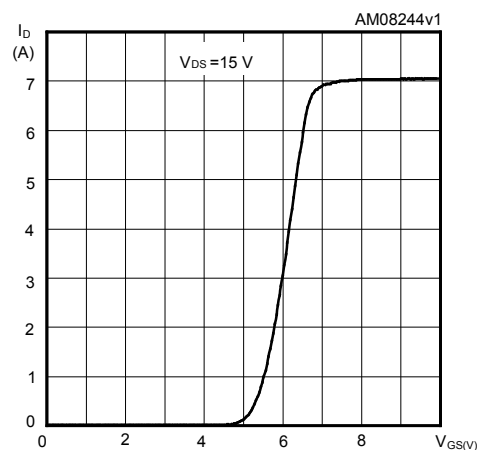
**Figure 2. Thermal impedance**



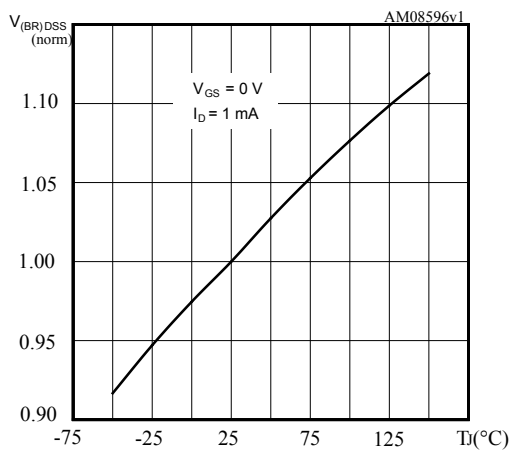
**Figure 3. Output characteristics**



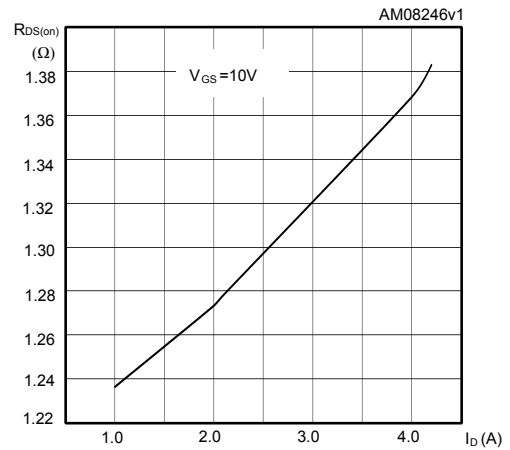
**Figure 4. Transfer characteristics**



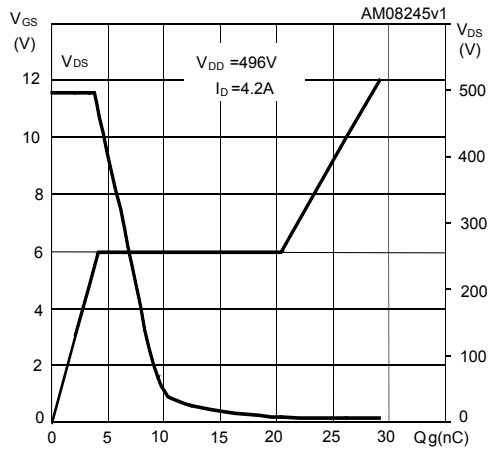
**Figure 5. Normalized  $V_{(BR)DSS}$  vs temperature**



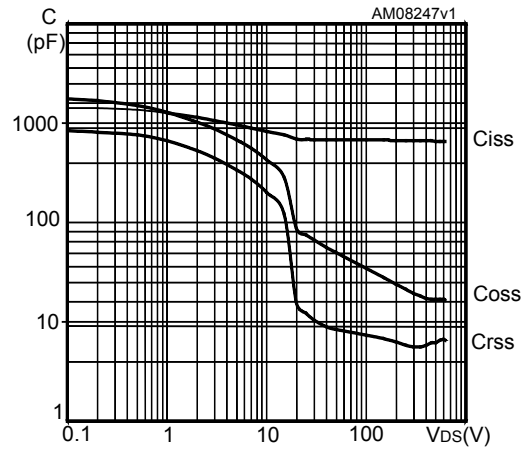
**Figure 6. Static drain-source on-resistance**



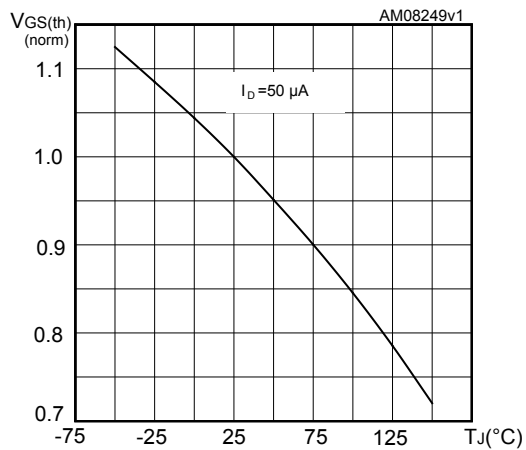
**Figure 7. Gate charge vs gate-source voltage**



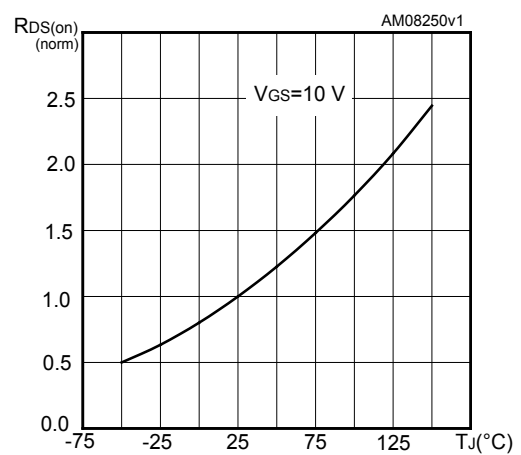
**Figure 8. Capacitance variations**



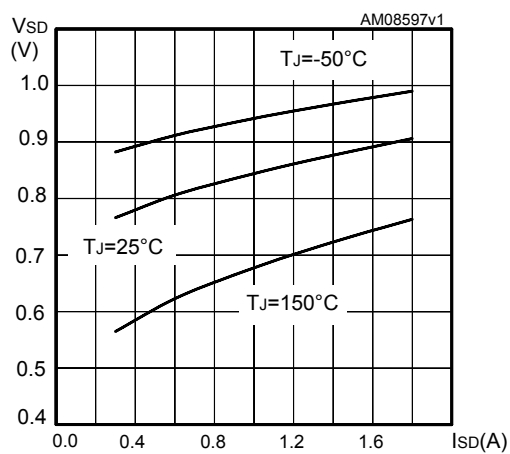
**Figure 9. Normalized gate threshold voltage vs temperature**



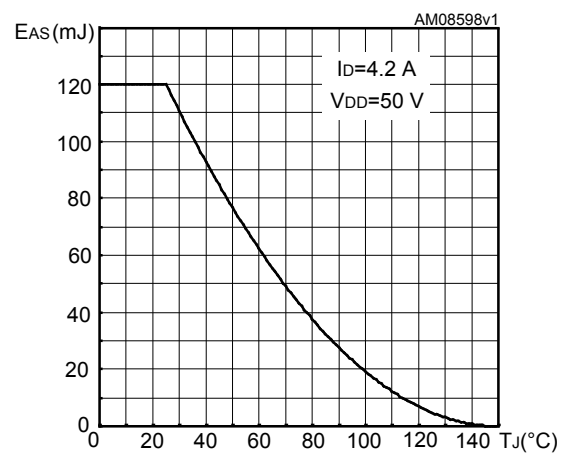
**Figure 10. Normalized on-resistance vs temperature**



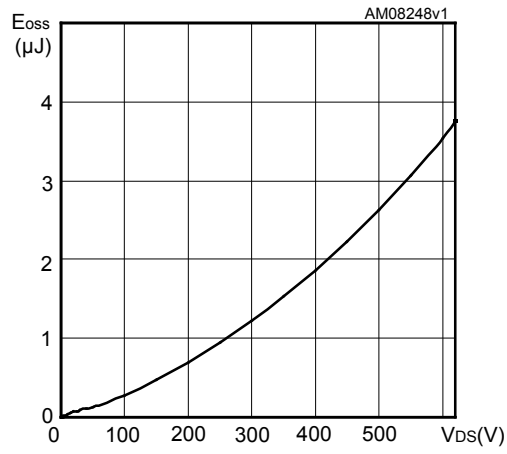
**Figure 11. Source-drain diode forward characteristics**



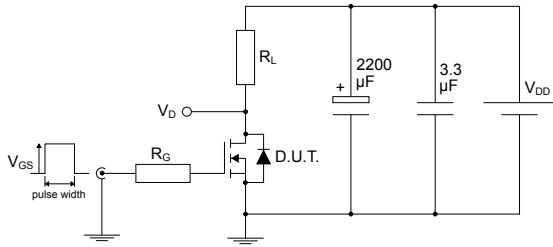
**Figure 12. Maximum avalanche energy vs temperature**



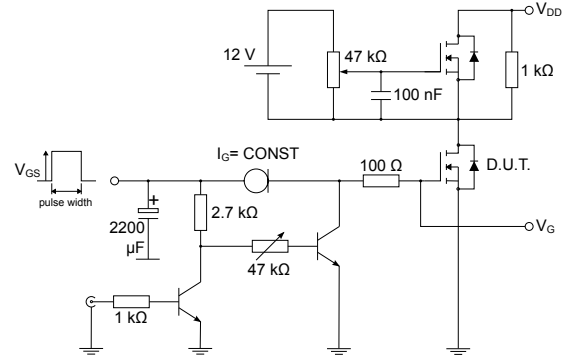
**Figure 13. Output capacitance stored energy**



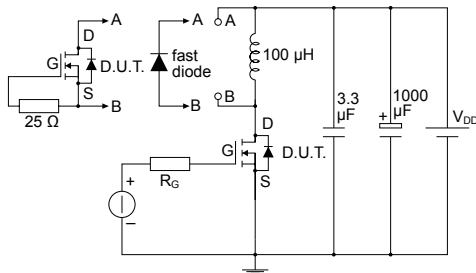
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


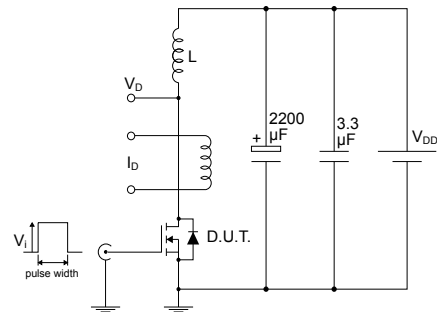
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**Figure 15. Test circuit for gate charge behavior**


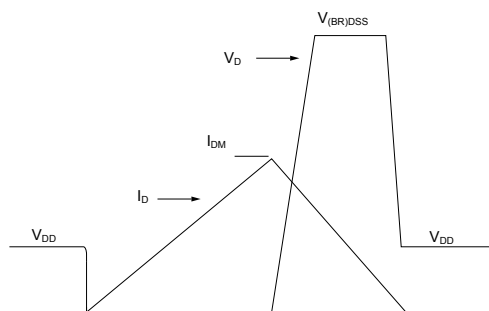
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


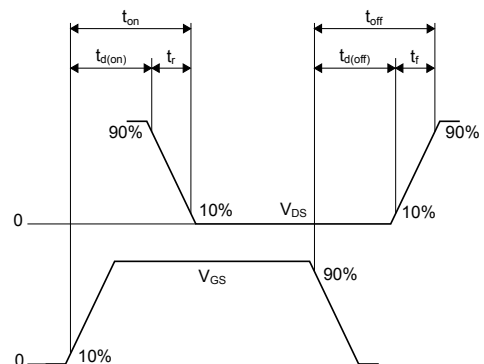
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


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**Figure 19. Switching time waveform**


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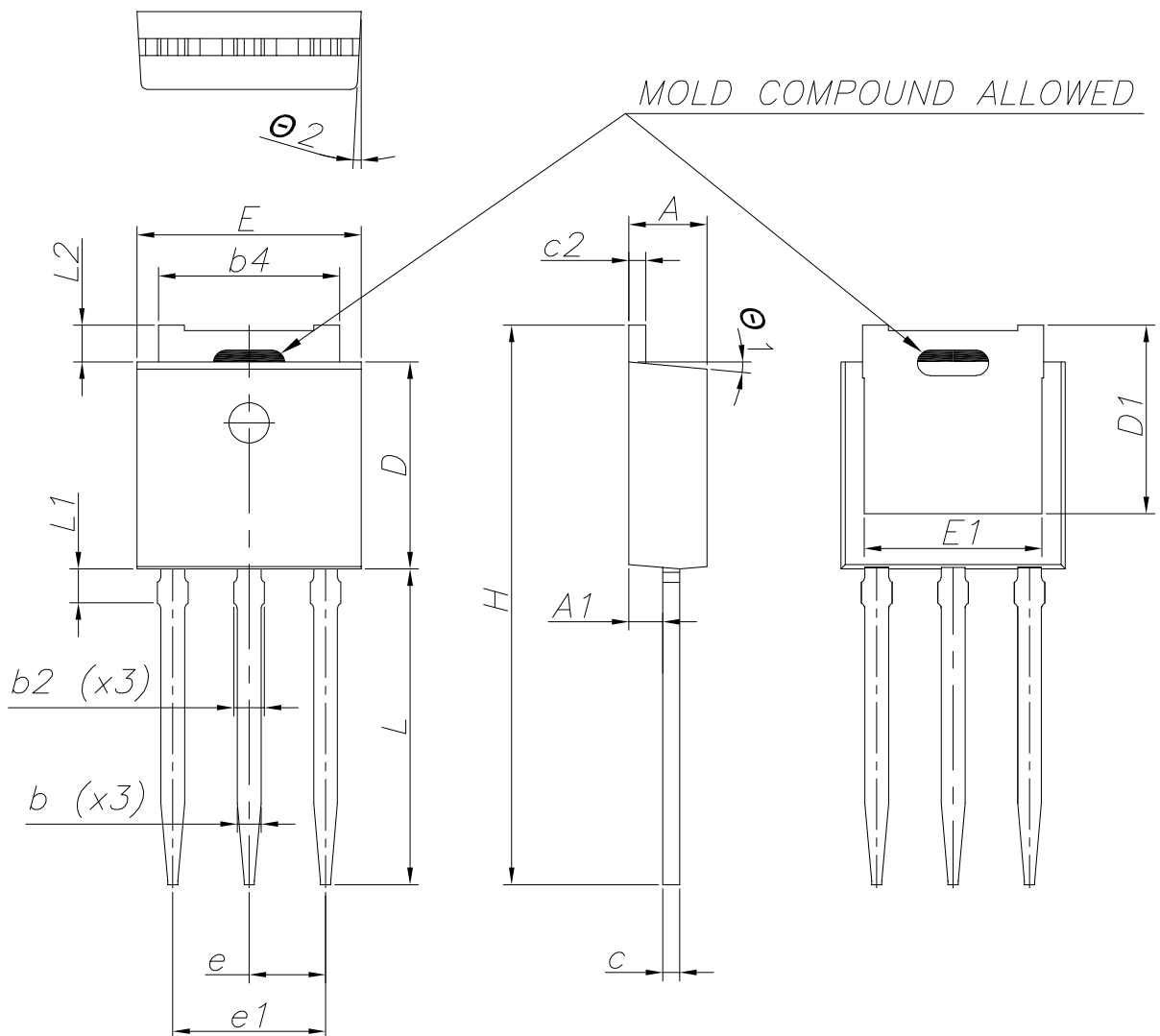


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 IPAK (TO-251) type E package information

Figure 20. IPAK (TO-251) type E package outline



0068771\_E\_rev.16

**Table 8. IPAK (TO-251) type E package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.30	5.53	5.75
E	6.50	6.60	6.70
E1	5.05	5.23	5.40
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
Ø1	3°	5°	7°
Ø2	1°	3°	5°

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
01-Sep-2023	1	First release. Part number STU5N62K3 previously included in datasheet DS6792.

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