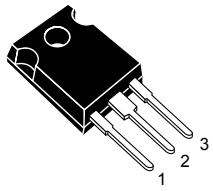
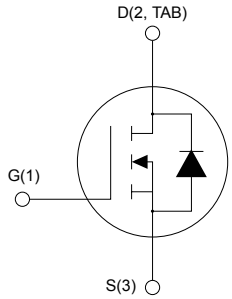
N-channel 1700 V, 7 Ω typ., 2.6 A PowerMESH Power MOSFET in a TO-247 package



TO-247



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW3N170	1700 V	13 Ω	2.6 A

- High speed switching
- Intrinsic capacitances and Q_g minimized
- 100% avalanche tested

Applications

- Switching applications

Description

This Power MOSFET is designed using the STMicroelectronics consolidated strip-layout-based MESH OVERLAY process. The result is a product that matches or improves on the performance of comparable standard parts from other manufacturers.

Product status link
STW3N170

Product summary	
Order code	STW3N170
Marking	3N170
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1700	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.6	A
	Drain current (continuous) at T_C = 100 °C	1.6	
I_{DM} (1)	Drain current (pulsed)	10.4	A
P_{TOT}	Total power dissipation at T_C = 25 °C	160	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.78	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	0.8	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	2	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1700			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1700 V, V_{GS} = 0 V			10	µA
		V_{DS} = 1700 V, V_{GS} = 0 V, T_C = 125 °C(1)			500	
I_{GSS}	Gate body leakage current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.3 A		7	13	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1100	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	7	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3.6	-	Ω
Q_g	Total gate charge	V_{DD} = 1360 V, I_D = 2.6 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	44	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 850 V, I_D = 1.3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	25	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	51	-	ns
t_f	Fall time		-	53	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.6	A
I_{SDM} (1)	Source-drain current (pulsed)		-		10.4	A
V_{SD}(2)	Forward on voltage	I_{SD} = 2.6 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 2.6 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	1.58		µs
Q_{rr}	Reverse recovery charge		-	6		µC
I_{RRM}	Reverse recovery current		-	7.9		A
t_{rr}	Reverse recovery time	I_{SD} = 2.6 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J= 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	2.12		µs
Q_{rr}	Reverse recovery charge		-	8.8		µC
I_{RRM}	Reverse recovery current		-	8.3		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

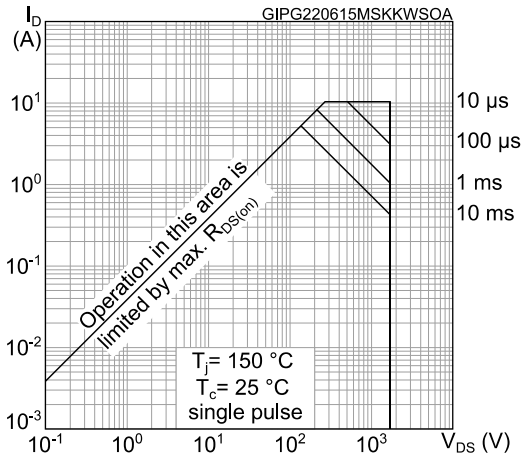


Figure 2. Normalized transient thermal impedance

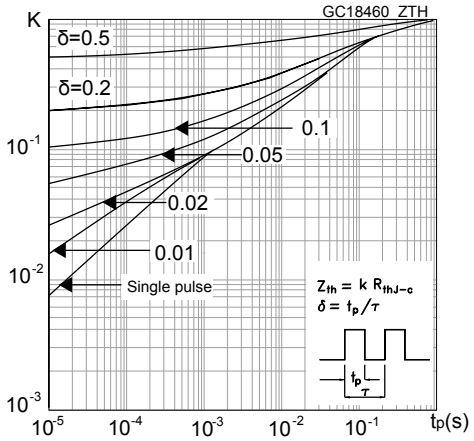


Figure 3. Typical output characteristics

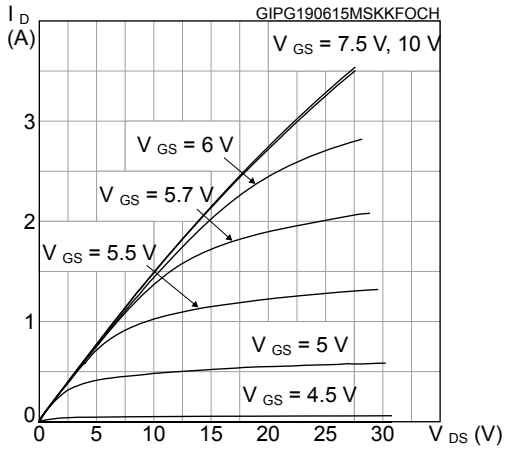


Figure 4. Typical transfer characteristics

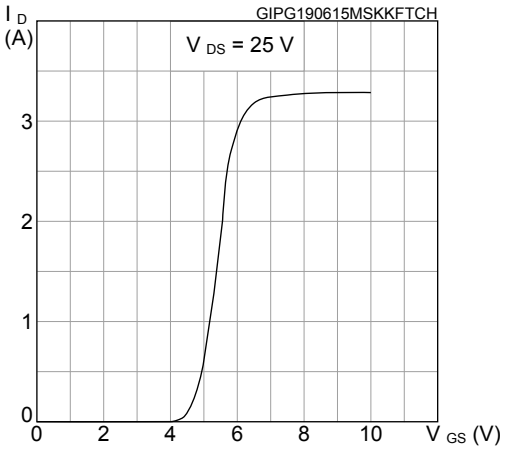


Figure 5. Typical gate charge characteristics

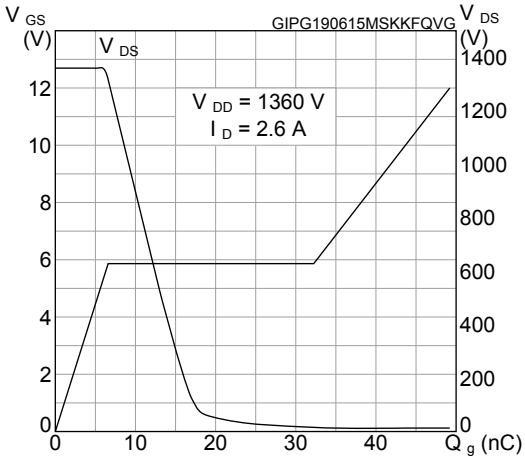


Figure 6. Typical drain-source on-resistance

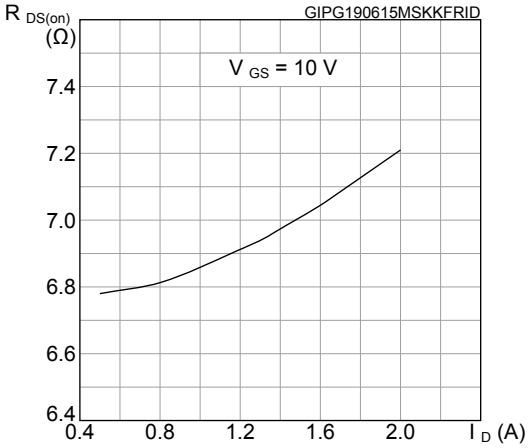


Figure 7. Typical capacitance characteristics

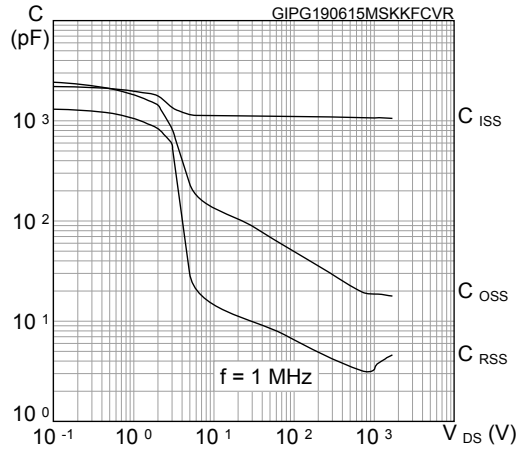


Figure 8. Maximum avalanche energy vs temperature

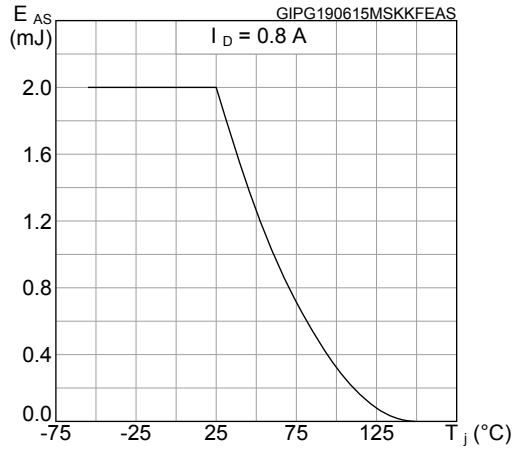


Figure 9. Normalized gate threshold vs temperature

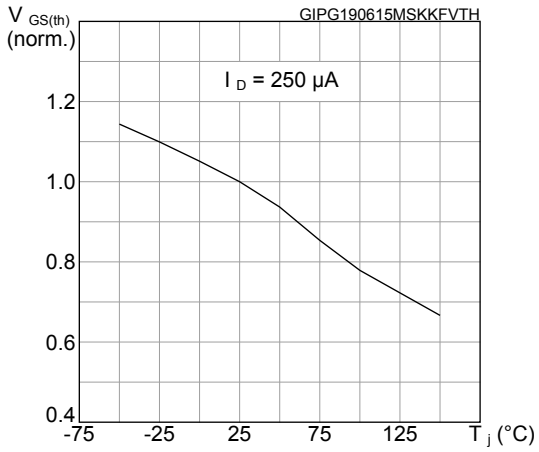


Figure 10. Normalized on-resistance vs temperature

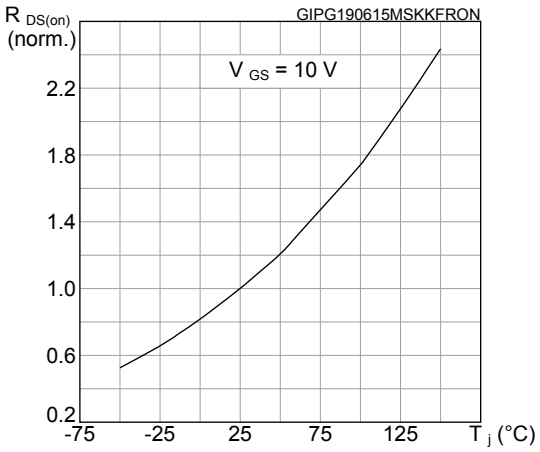


Figure 11. Typical reverse diode forward characteristics

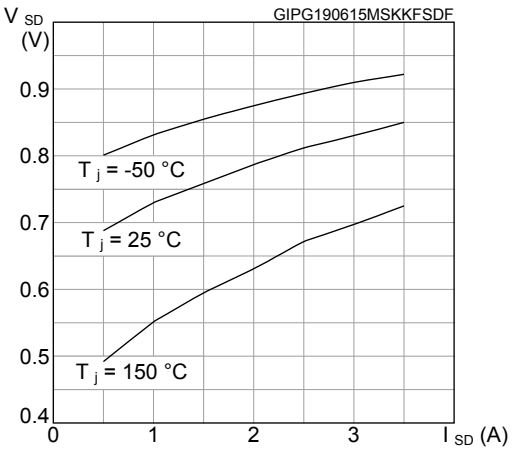
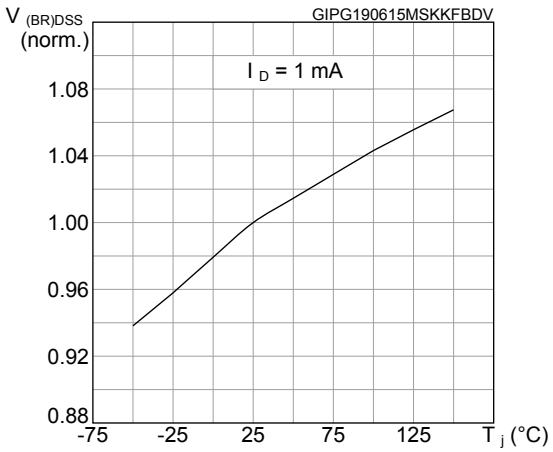


Figure 12. Normalized breakdown voltage vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

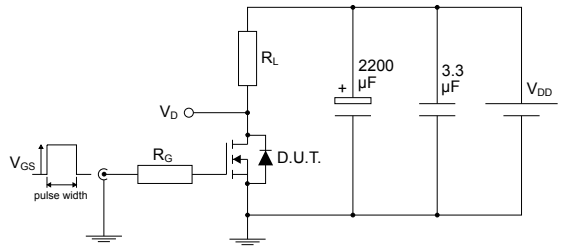


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Figure 14. Test circuit for gate charge behavior

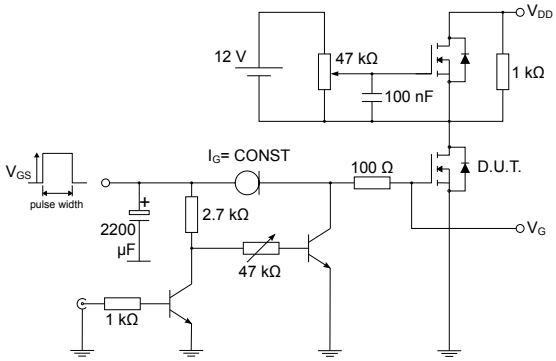

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Figure 15. Test circuit for inductive load switching and diode recovery times

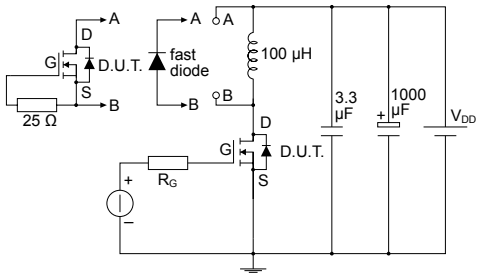

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Figure 16. Unclamped inductive load test circuit

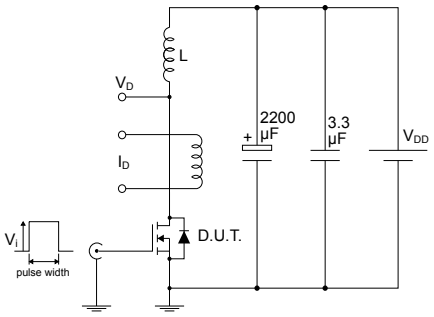

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Figure 17. Unclamped inductive waveform

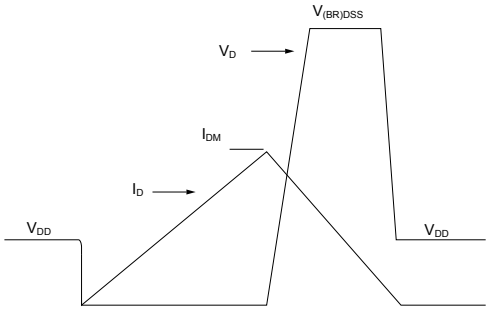

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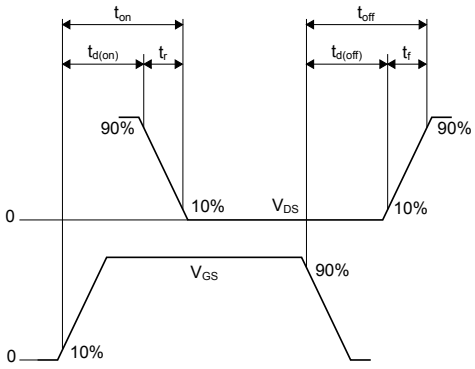
Figure 18. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 19. TO-247 package outline

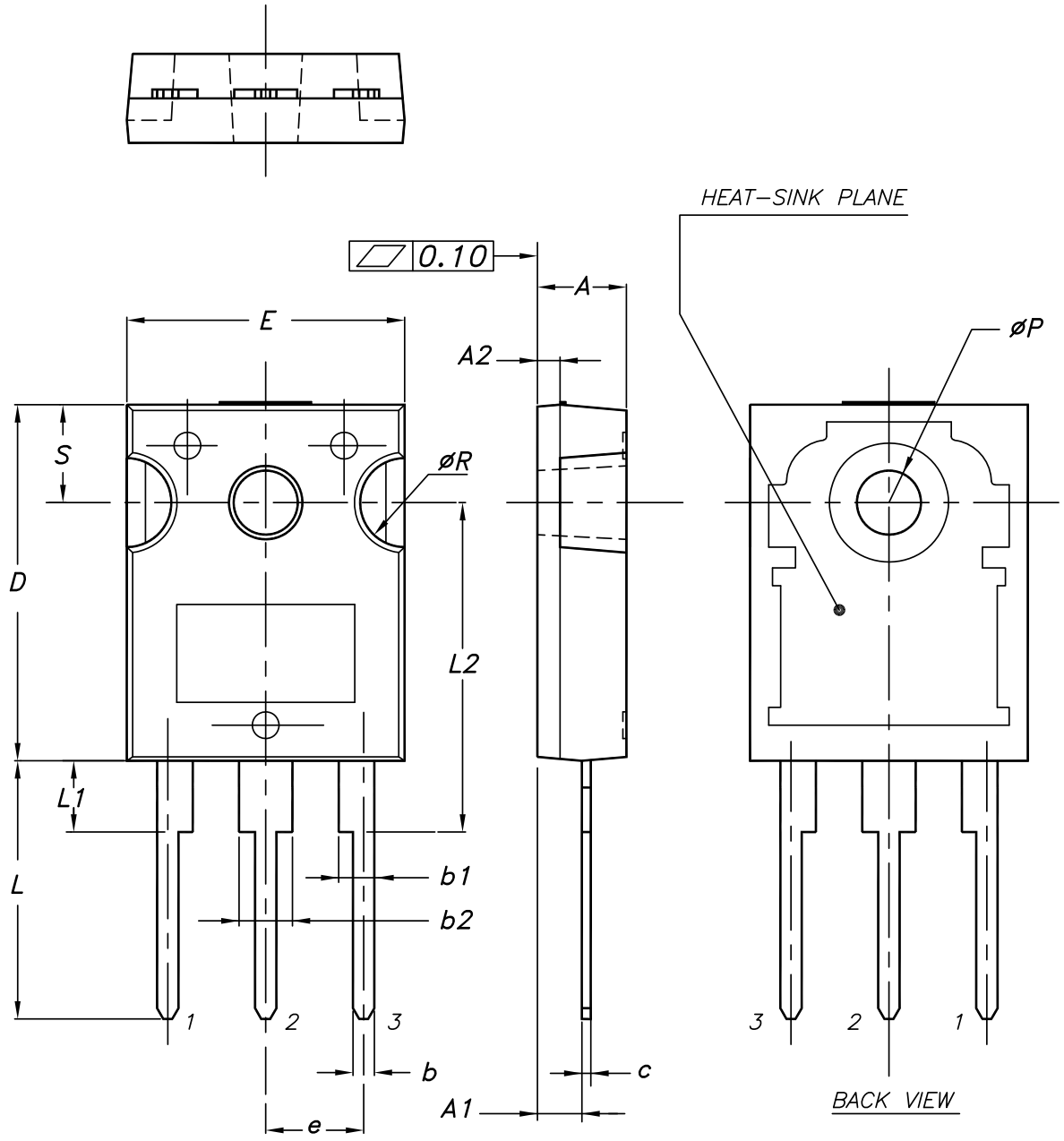

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Table 8. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
14-Sep-2015	1	First release.
22-Apr-2024	2	The part number STWA3N170 has been moved to a separate datasheet and the document has been updated accordingly. Updated *Section 4.1: TO-247 package information.* Minor text changes.
11-Feb-2026	3	Updated Table 7. Source-drain diode. Updated Section 4.1: TO-247 package information. Minor text changes.

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