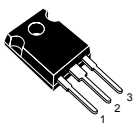
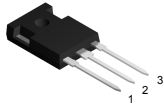


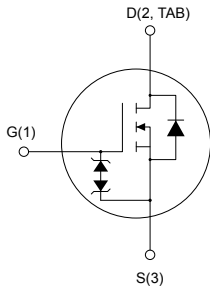
N-channel 600 V, 36 mΩ typ., 62 A, MDmesh DM6 Power MOSFETs in TO-247 and TO-247 long leads packages



TO-247



TO-247 long leads



AM01476v1_tab



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STW70N60DM6	600 V	42 mΩ	62 A
STWA70N60DM6			

- Fast-recovery body diode
- Lower R_{DS(on)} per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

These high-voltage N-channel Power MOSFETs are part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in R_{DS(on)} per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status links

[STW70N60DM6, STWA70N60DM6](#)

Product summary

STW70N60DM6

Order code	STW70N60DM6
Marking	70N60DM6
Package	TO-247
Packing	Tube

STWA70N60DM6

Order code	STWA70N60DM6
Marking	70N60DM6
Package	TO-247 long leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	62	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	39	A
$I_{DM}^{(1)}$	Drain current (pulsed)	220	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	390	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	1000	A/ μs
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 62\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.32	$^\circ\text{C/W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	$^\circ\text{C/W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1850	mJ

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 125\text{ }^\circ\text{C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 31\text{ A}$		36	42	$\text{m}\Omega$

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	4360	-	pF
C_{oss}	Output capacitance		-	235	-	
C_{rss}	Reverse transfer capacitance		-	13	-	
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0\text{ V}$	-	697	-	
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	1.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 62\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	99	-	nC
Q_{gs}	Gate-source charge		-	28	-	
Q_{gd}	Gate-drain charge		-	44	-	

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 31\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	28	-	ns
t_r	Rise time		-	49	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	96	-	ns
t_f	Fall time		-	12	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		62	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		220	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 62\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 62\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$	-	138	-	ns
Q_{rr}	Reverse recovery charge		-	0.69	-	μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 62\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	340	-	ns
Q_{rr}	Reverse recovery charge		-	4.6	-	μC
I_{RRM}	Reverse recovery current		(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	27	-

1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

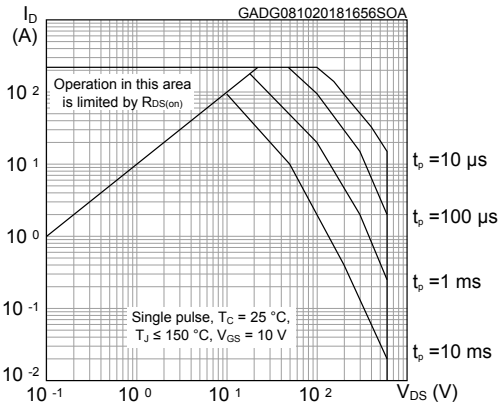


Figure 2. Thermal impedance

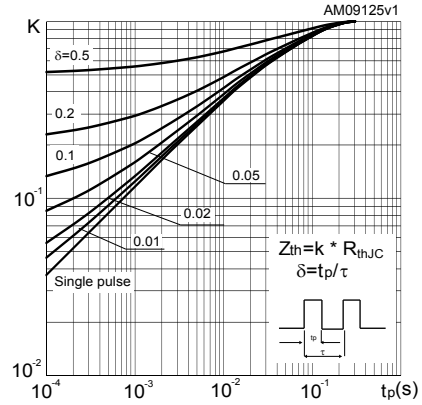


Figure 3. Output characteristics

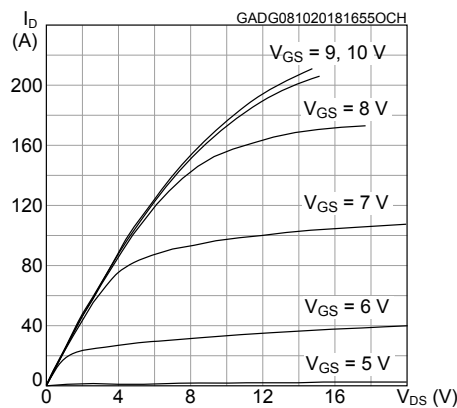


Figure 4. Transfer characteristics

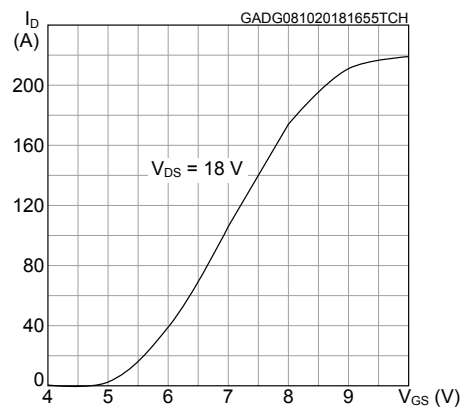


Figure 5. Gate charge vs gate-source voltage

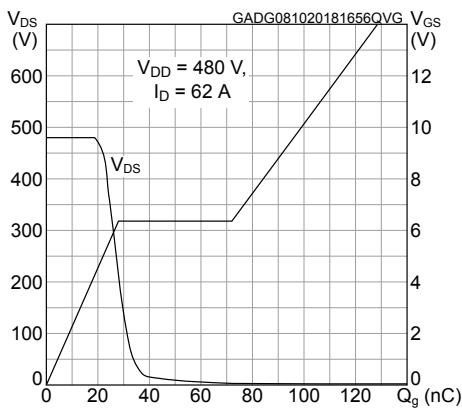


Figure 6. Static drain-source on-resistance

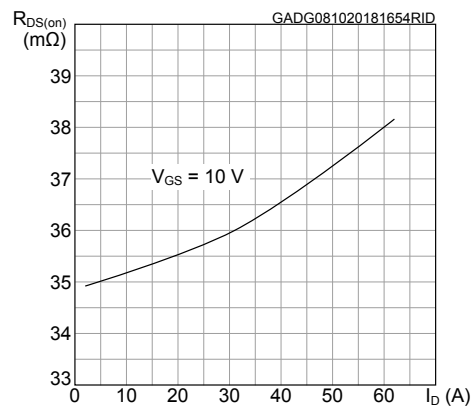
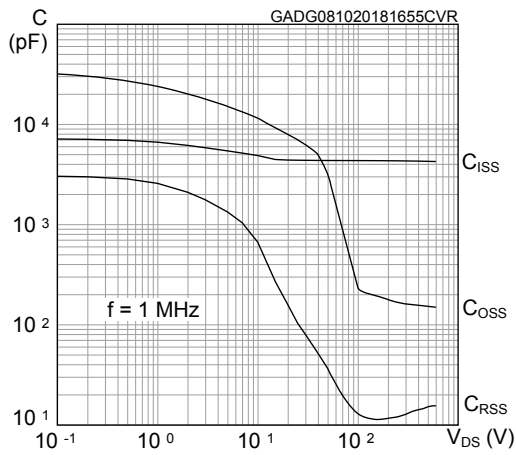
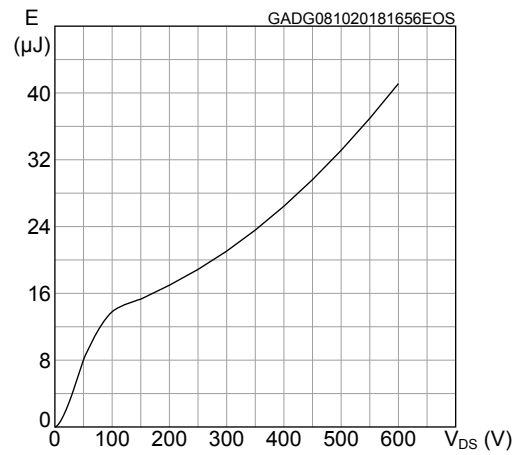
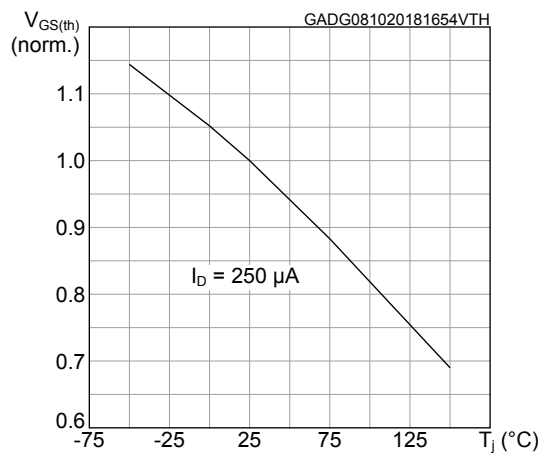
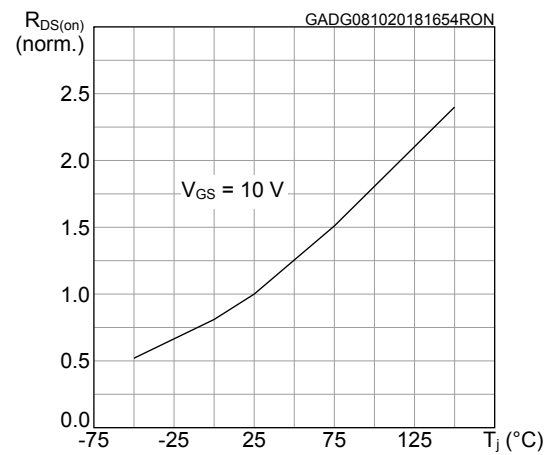
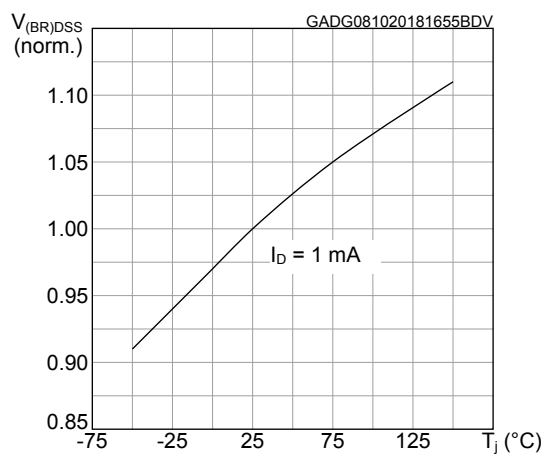
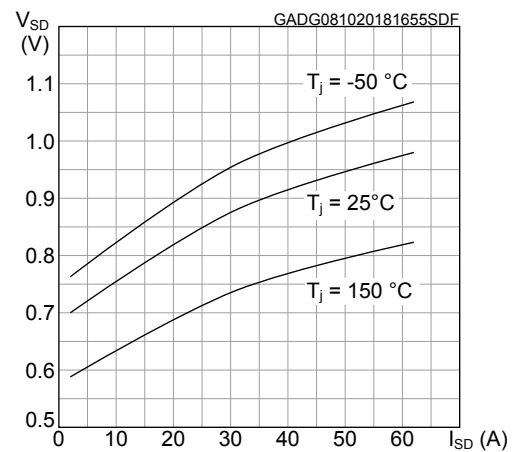
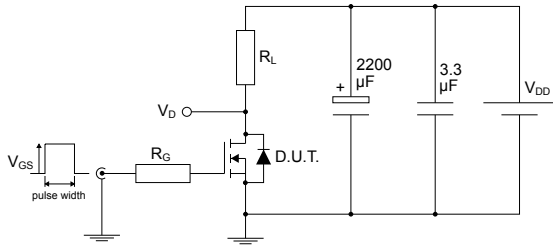
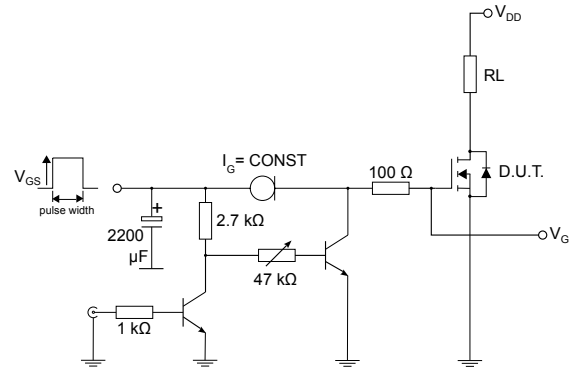


Figure 7. Capacitance variations

Figure 8. C_{OSS} stored energy vs V_{DS}

Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

Figure 12. Source-drain diode forward characteristics


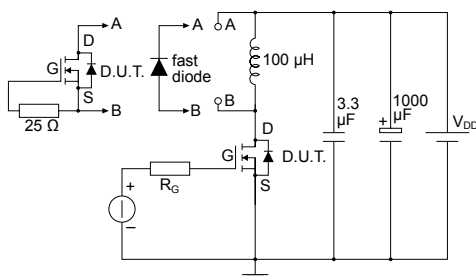
3 Test circuits

Figure 13. Test circuit for resistive load switching times


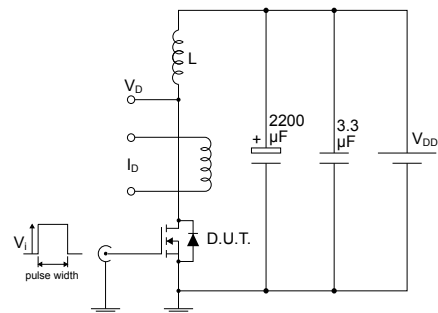
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Figure 14. Test circuit for gate charge behavior


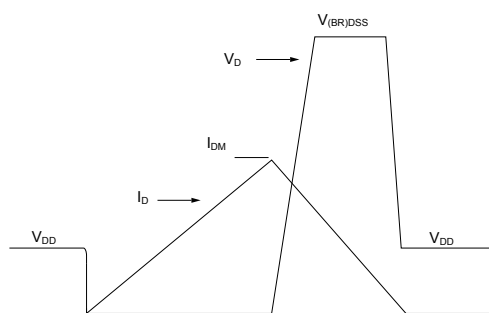
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Figure 15. Test circuit for inductive load switching and diode recovery times


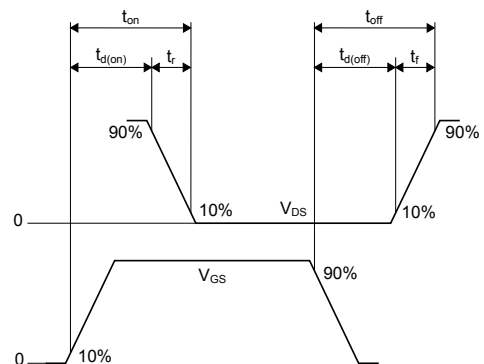
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


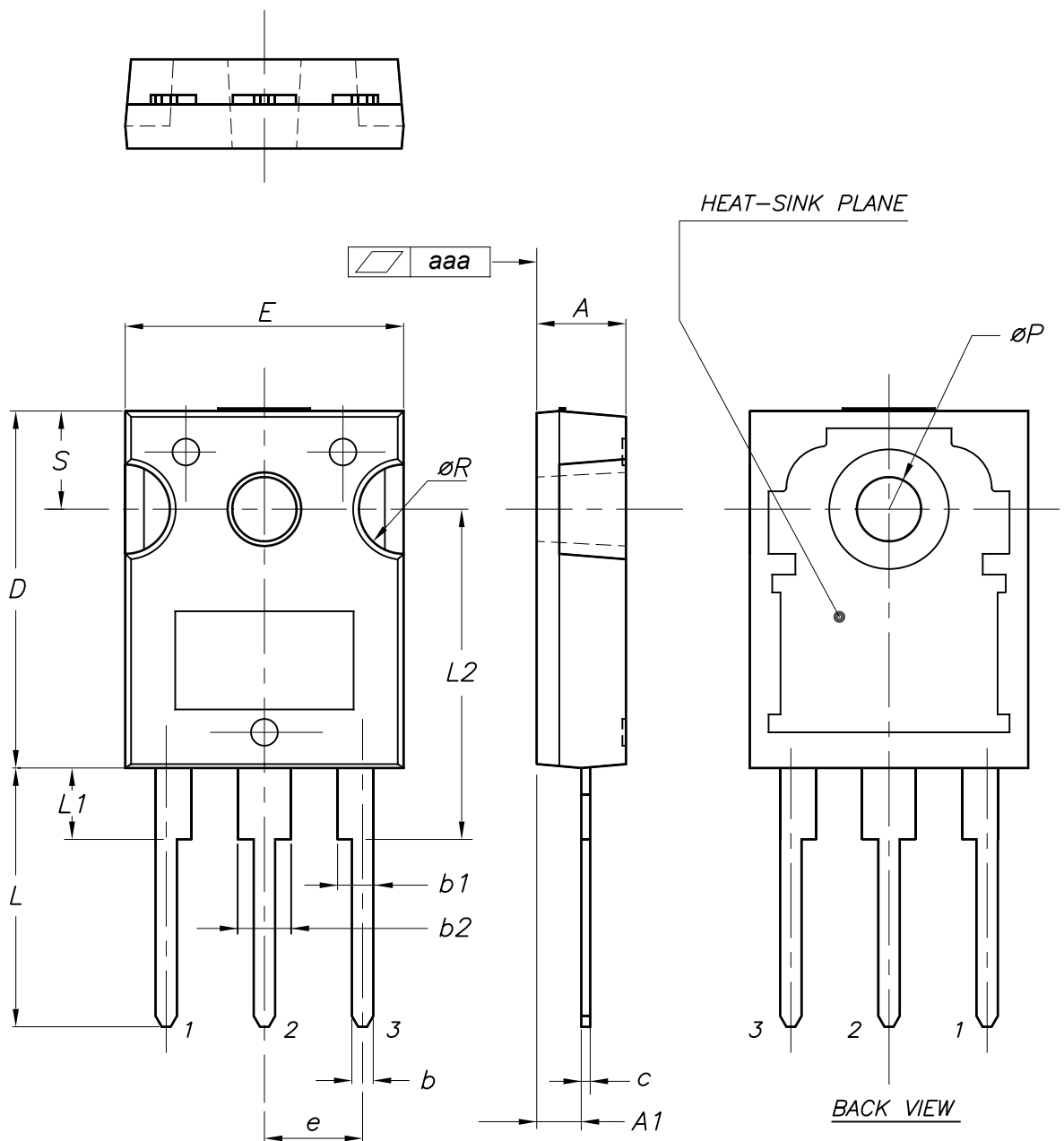
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 19. TO-247 package outline



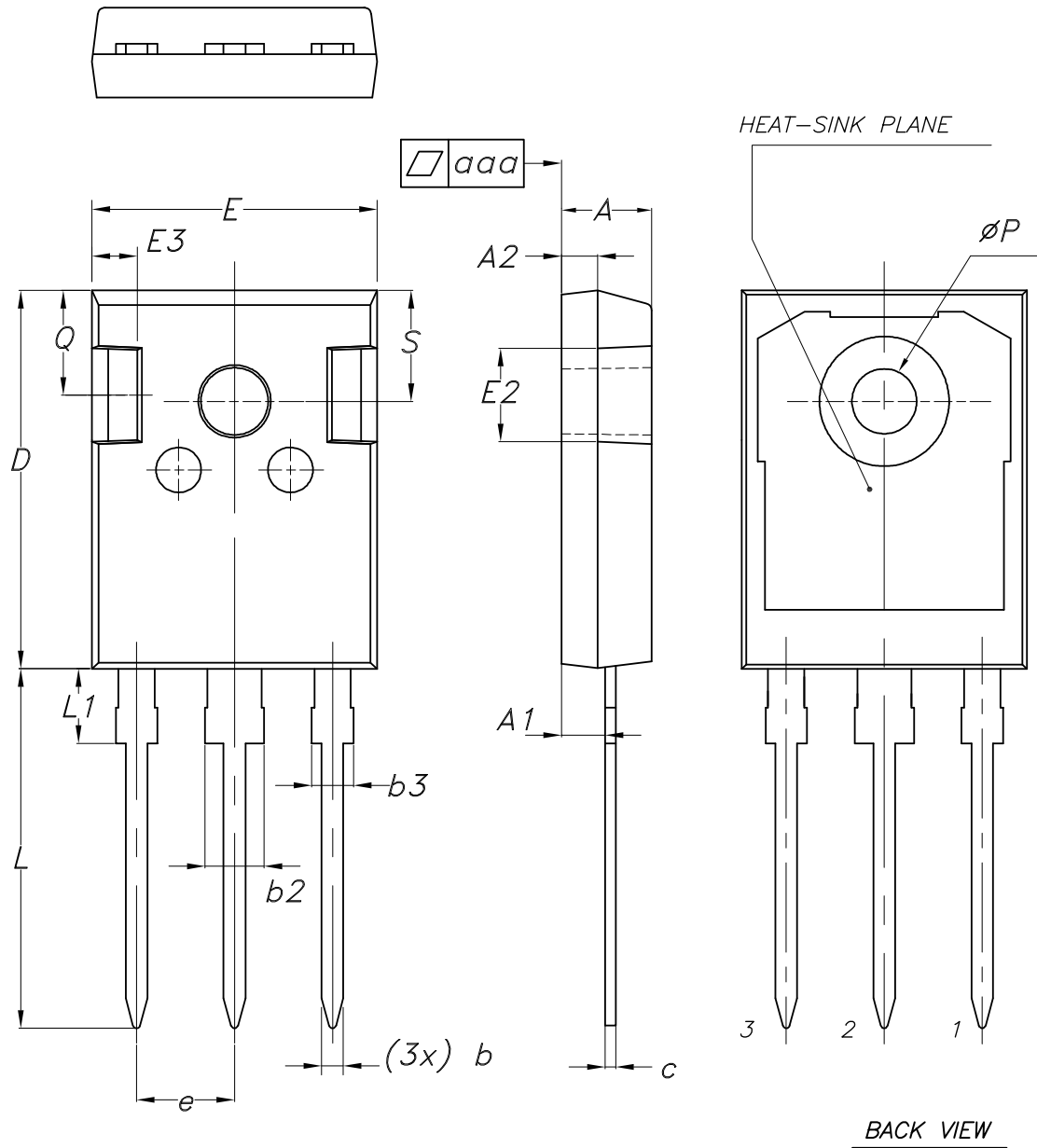
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Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.2 TO-247 long leads package information

Figure 20. TO-247 long leads package outline



8463846_3

Table 9. TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Nov-2017	1	First release.
10-Oct-2018	2	Removed maturity status indication from cover page. The document status is production data. Updated Section 1 Electrical ratings and Section 2 Electrical characteristics. Added Section 2.1 Electrical characteristics (curves). Minor text changes.
02-May-2019	3	Updated Table 6. Switching times. Minor text changes.
01-Jun-2020	4	Updated <i>Table 1. Absolute maximum ratings</i> and <i>Table 7. Source drain diode</i> .
21-Feb-2023	5	Updated <i>Table 4. On/off states</i> . Updated C_{oss} eq. on <i>Table 5. Dynamic characteristics</i> . Updated <i>Section 4 Package information</i> . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	TO-247 package information	8
4.2	TO-247 long leads package information	10
	Revision history	12



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