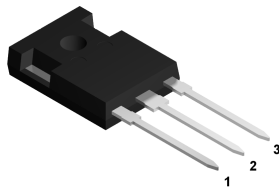
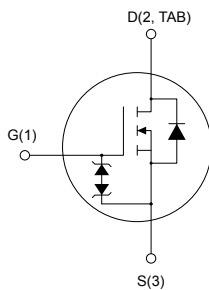


## N-channel 950 V, 110 mΩ typ., 38 A MDmesh K5 Power MOSFET in a TO-247 long leads package



TO-247 long leads



AM01476v1\_tab



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STWA40N95K5	950 V	130 mΩ	38 A

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STWA40N95K5](#)

#### Product summary

Order code	STWA40N95K5
Marking	40N95K5
Package	TO-247 long leads
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	38	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	24	
$I_{DM}^{(1)}$	Drain current (pulsed)	152	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	450	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 19\text{ A}$ ,  $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ .
3.  $V_{DD} = 760\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.28	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	50	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)	13	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	700	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	950			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 19\text{ A}$		110	130	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ kHz}$ , $V_{GS} = 0\text{ V}$	-	3300	-	pF
$C_{oss}$	Output capacitance		-	250	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}$ <sup>(1)</sup>	Equivalent capacitance, time-related	$V_{DS} = 0\text{ to }760\text{ V}$ , $V_{GS} = 0\text{ V}$	-	398	-	pF
$C_{o(er)}$ <sup>(2)</sup>	Equivalent capacitance, energy-related		-	142	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 760\text{ V}$ , $I_D = 38\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	93	-	nC
$Q_{gs}$	Gate-source charge		-	18.7	-	nC
$Q_{gd}$	Gate-drain charge		-	63.4	-	nC

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$ , $I_D = 19\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	33.5	-	ns
$t_r$	Rise time		-	51	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	91.5	-	ns
$t_f$	Fall time		-	10	-	ns

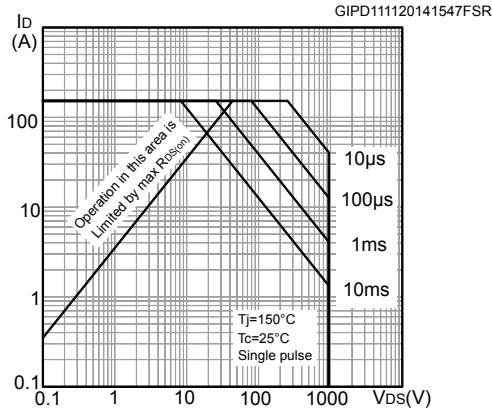
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 38\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 38\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	706		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	22		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	62		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 38\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	886		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	28.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	64		A

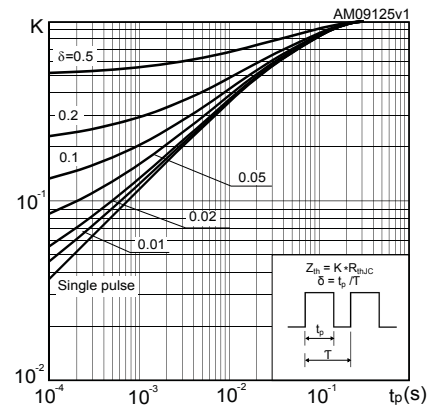
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

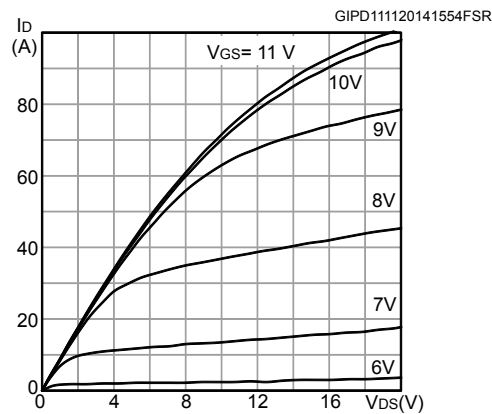
**Figure 1. Safe operating area**



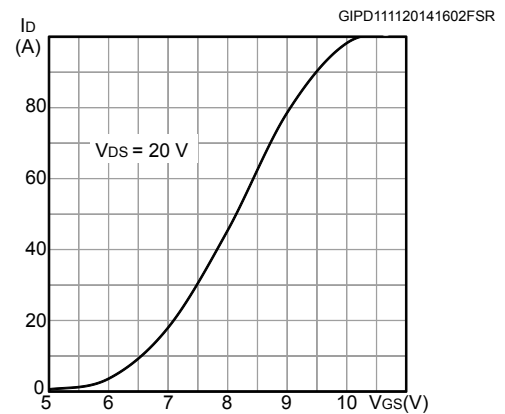
**Figure 2. Normalized transient thermal impedance**



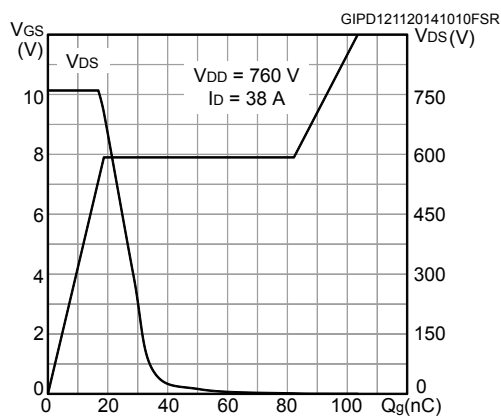
**Figure 3. Typical output characteristics**



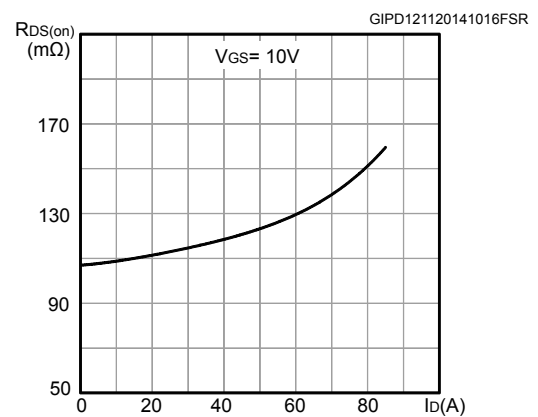
**Figure 4. Typical transfer characteristics**



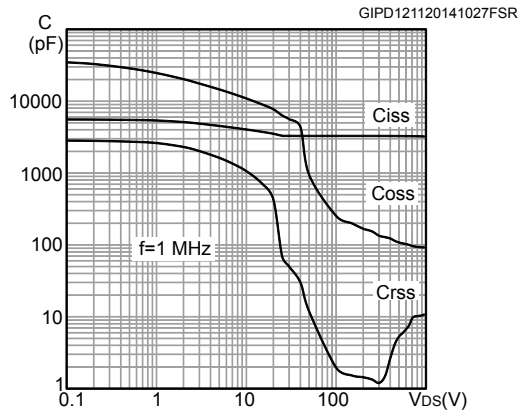
**Figure 5. Typical gate charge characteristics**



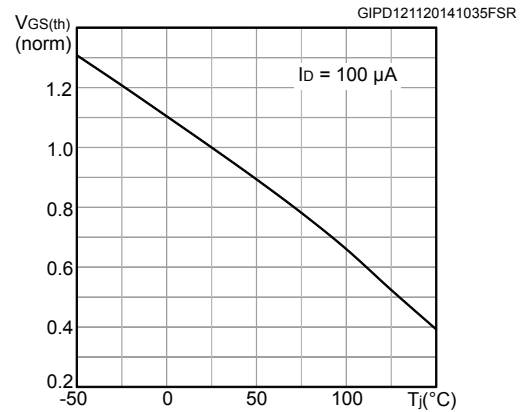
**Figure 6. Typical drain-source on-resistance**



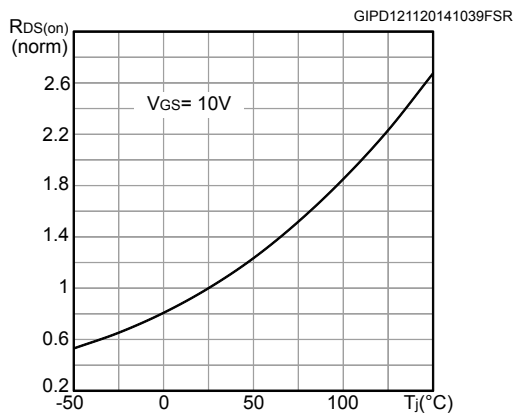
**Figure 7. Typical capacitance characteristics**



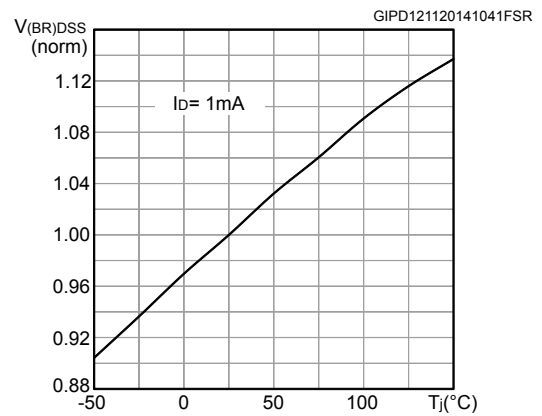
**Figure 8. Normalized gate threshold vs temperature**



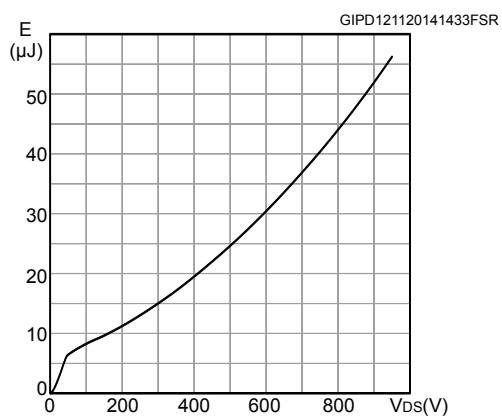
**Figure 9. Normalized on-resistance vs temperature**



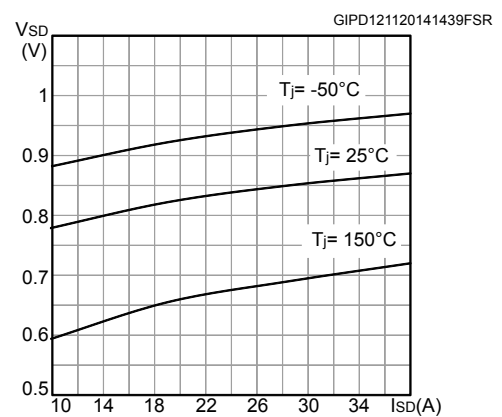
**Figure 10. Normalized breakdown voltage vs temperature**



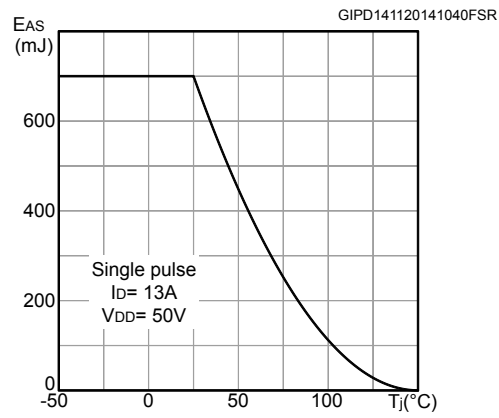
**Figure 11. Typical output capacitance stored energy**



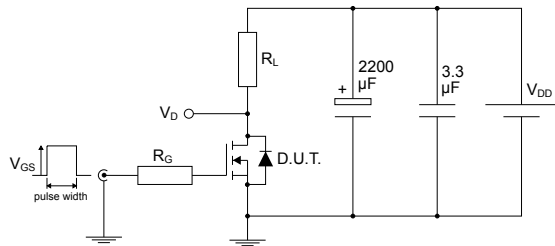
**Figure 12. Typical reverse diode forward characteristics**



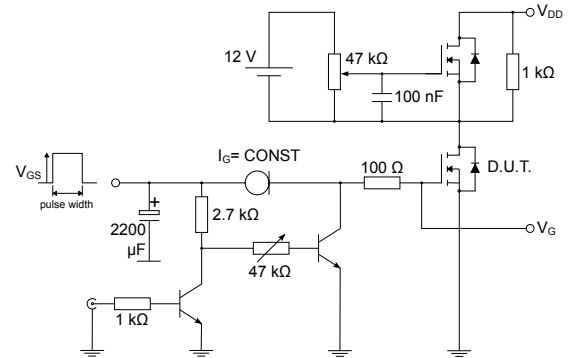
**Figure 13. Maximum output capacitance stored energy**



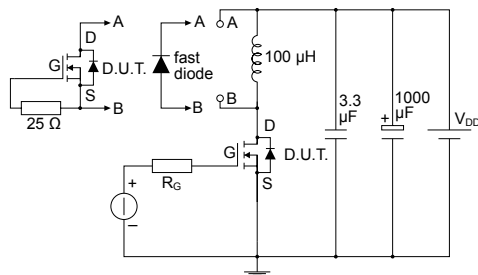
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


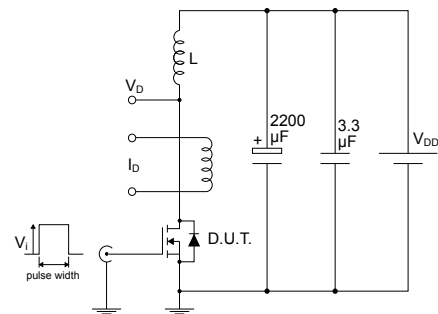
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**Figure 15. Test circuit for gate charge behavior**


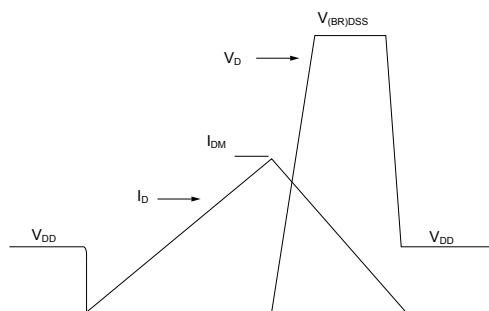
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


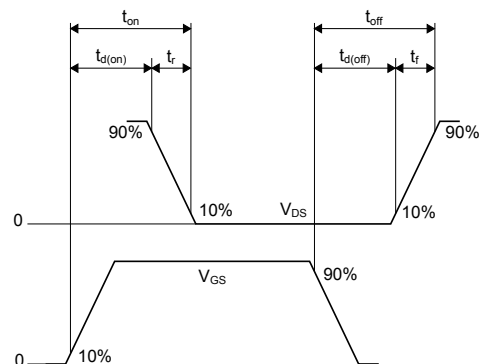
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


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**Figure 19. Switching time waveform**


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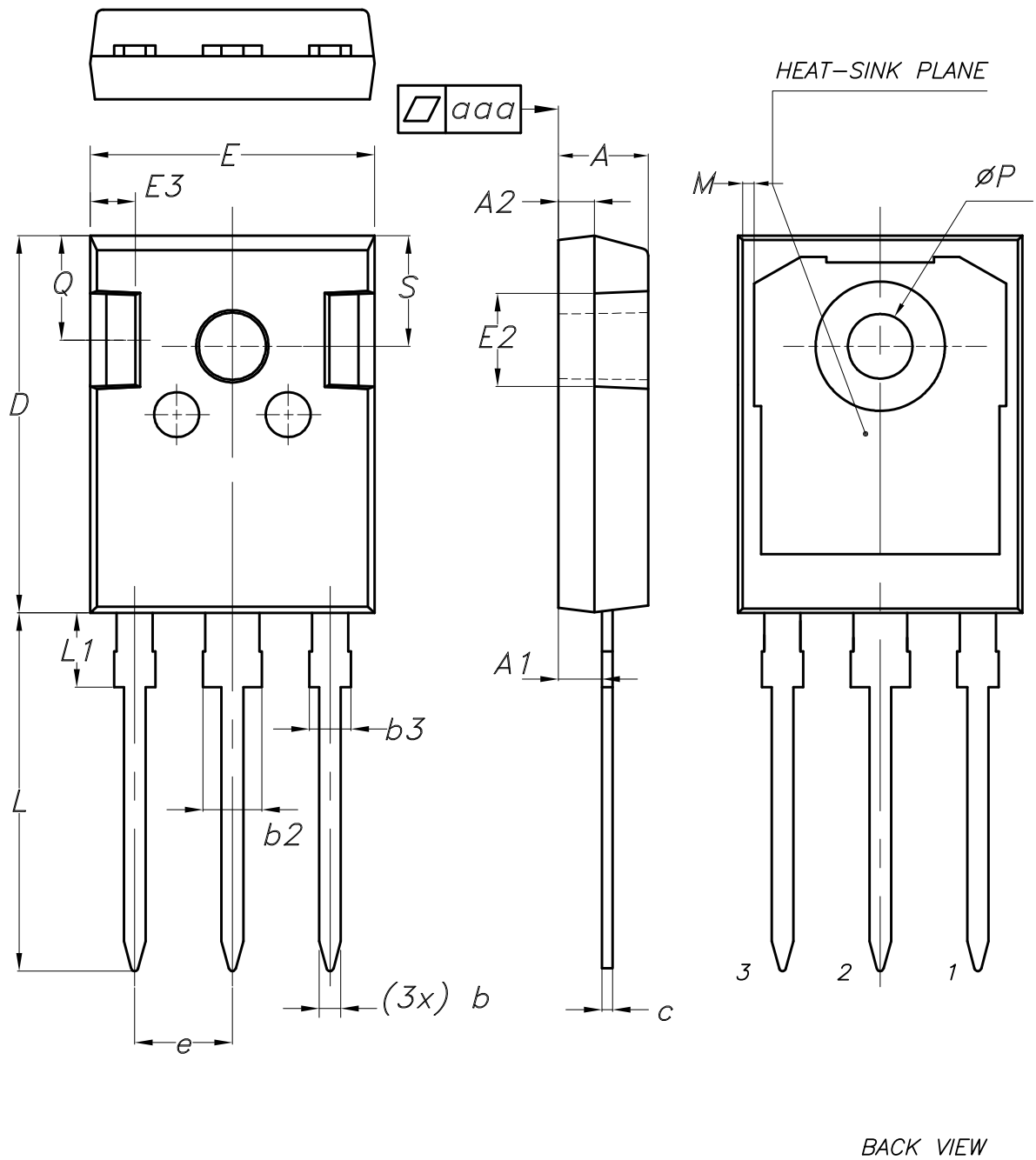


## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-247 long leads package information

Figure 20. TO-247 long leads package outline



8463846\_6

**Table 8. TO-247 long leads package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
M	0.35		0.95
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
05-Aug-2015	1	First release.
07-Apr-2025	2	Updated Section 4.1: TO-247 long leads package information. Minor text changes.

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