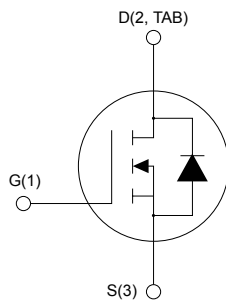
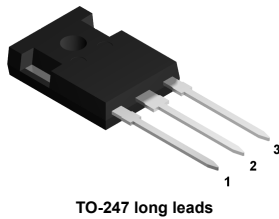


N-channel 600 V, 32 mΩ typ., 62 A MDmesh M9 Power MOSFET in a TO-247 long leads package



AM01475v1_no2en


Product status link
[STWA60N035M9](#)
Product summary

Order code	STWA60N035M9
Marking	60N035M9
Package	TO-247 long leads
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STWA60N035M9	600 V	35 mΩ	62 A

- Very low FOM ($R_{DS(on)} \cdot Q_g$)
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Application

- AC-DC converters
- DC-DC converters
- Microinverter

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	62	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	39	
$I_{DM}^{(1)}$	Drain current (pulsed)	250	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	321	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	900	A/ μs
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 31\text{ A}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.39	$^\circ\text{C/W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	$^\circ\text{C/W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	786	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			200	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 31\text{ A}$		32	35	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$, $V_{GS} = 0\text{ V}$	-	4830	-	pF
C_{oss}	Output capacitance		-	90.5	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	1300	-	pF
R_g	Intrinsic gate resistance	$f = 250\text{ kHz}$, open drain	-	0.8	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 31\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	112	-	nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge		-	43	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 31\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	28	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	81	-	ns
t_f	Fall time		-	4.2	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		62	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		250	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 62\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 62\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	277		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	3.1		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	29		A
t_{rr}	Reverse recovery time	$I_{SD} = 62\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	445		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	7		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	29		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

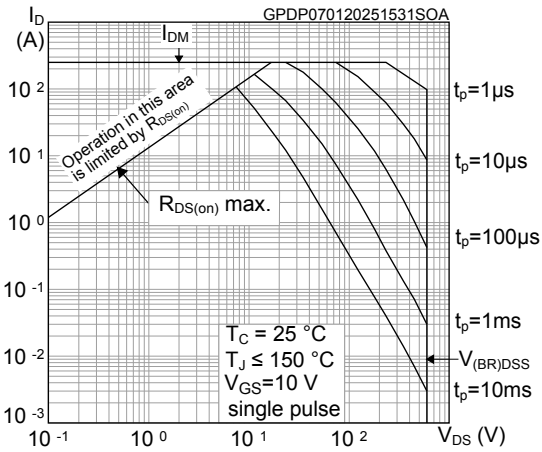
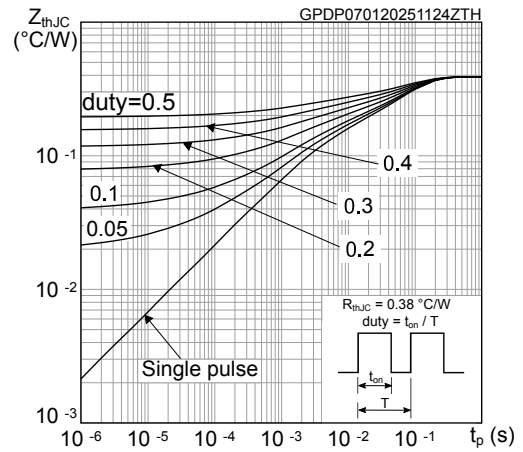
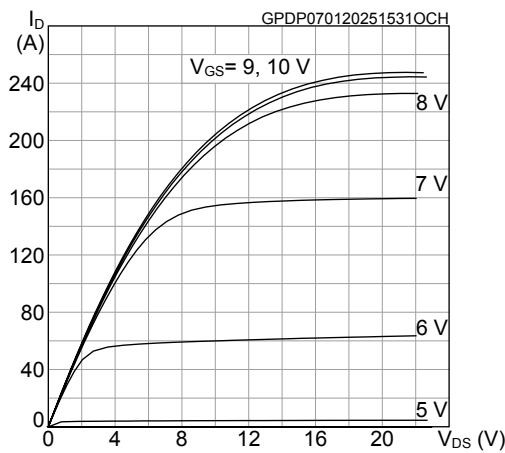
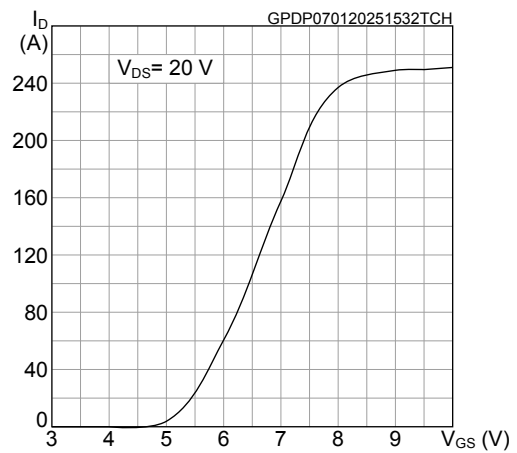
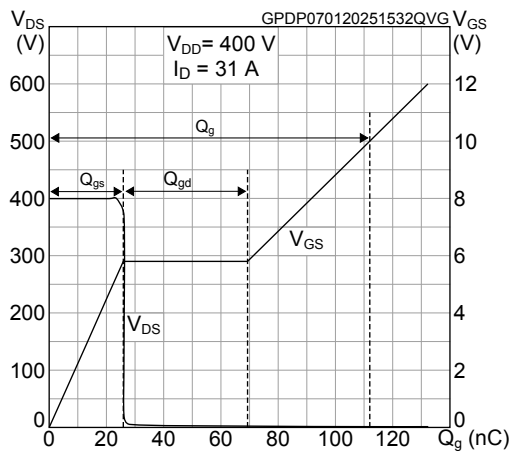
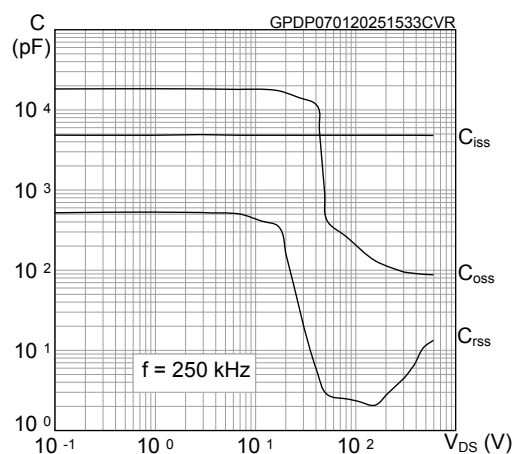
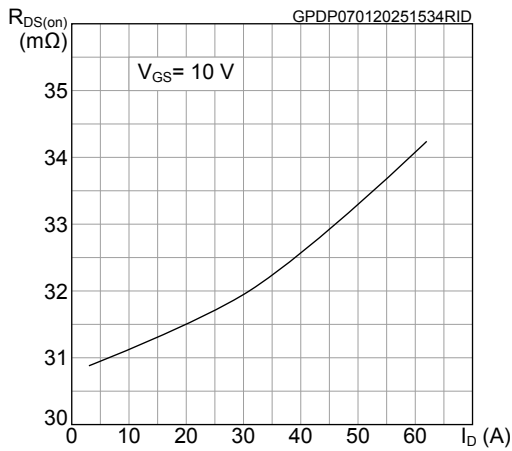
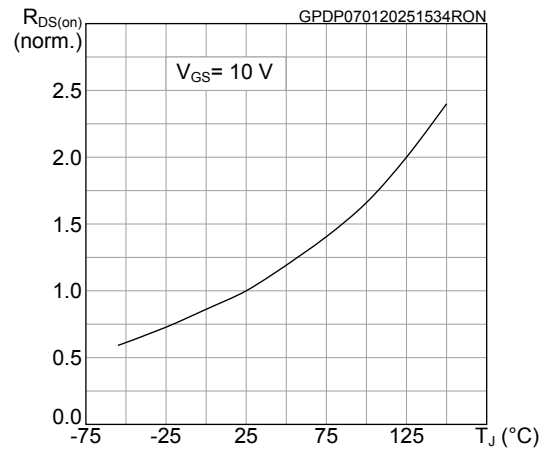
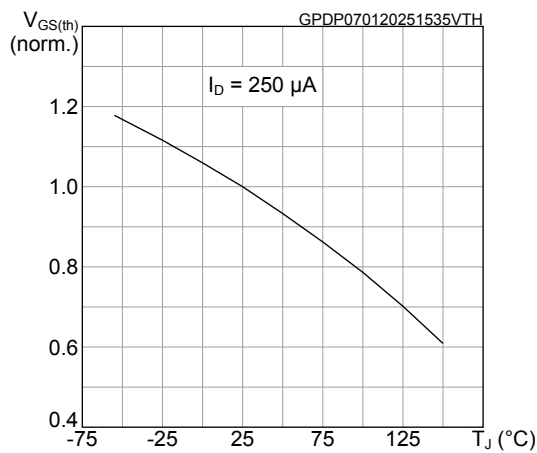
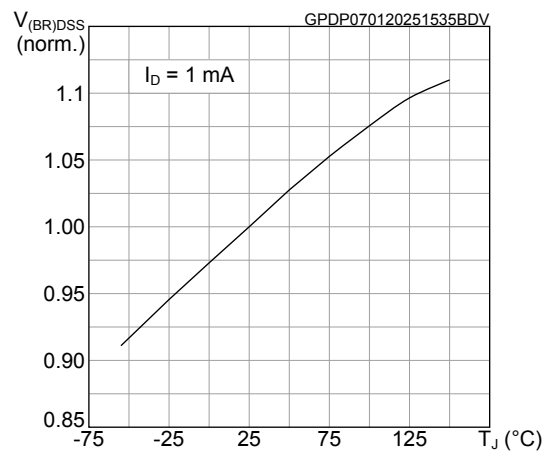
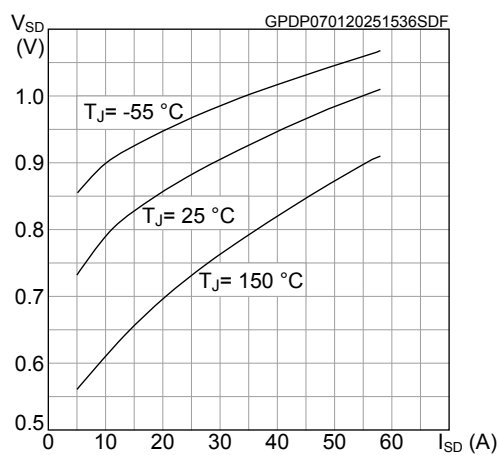
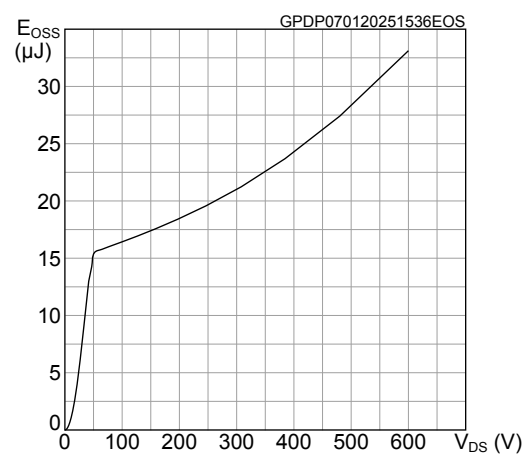
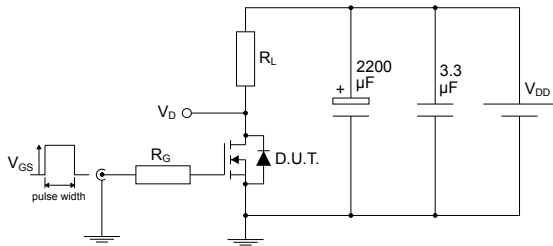
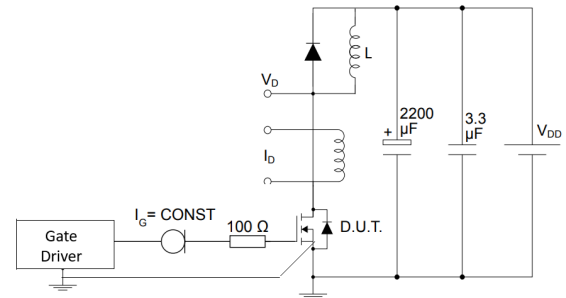
Figure 1. Safe operating area

Figure 2. Maximum transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical capacitance characteristics


Figure 7. Typical drain-source on-resistance

Figure 8. Normalized on-resistance vs temperature

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Typical reverse diode forward characteristics

Figure 12. Typical output capacitance stored energy


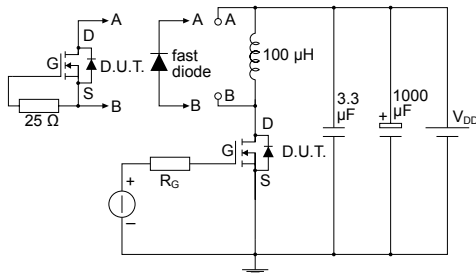
3 Test circuits

Figure 13. Test circuit for resistive load switching times


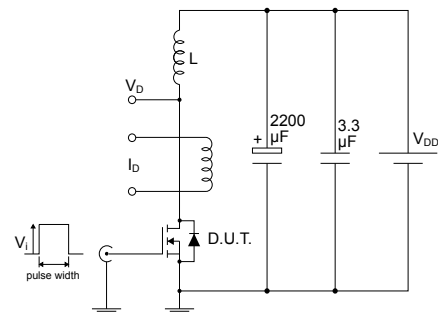
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Figure 14. Test circuit for gate charge behavior


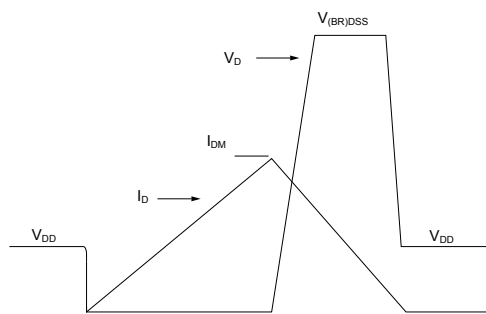
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Figure 15. Test circuit for inductive load switching and diode recovery times


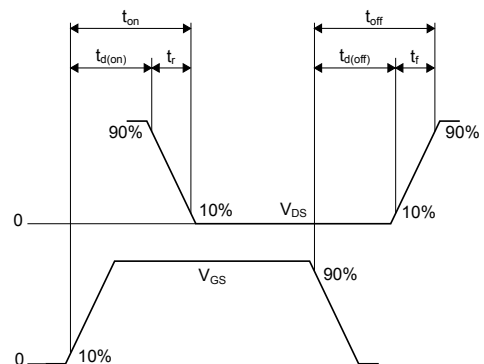
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


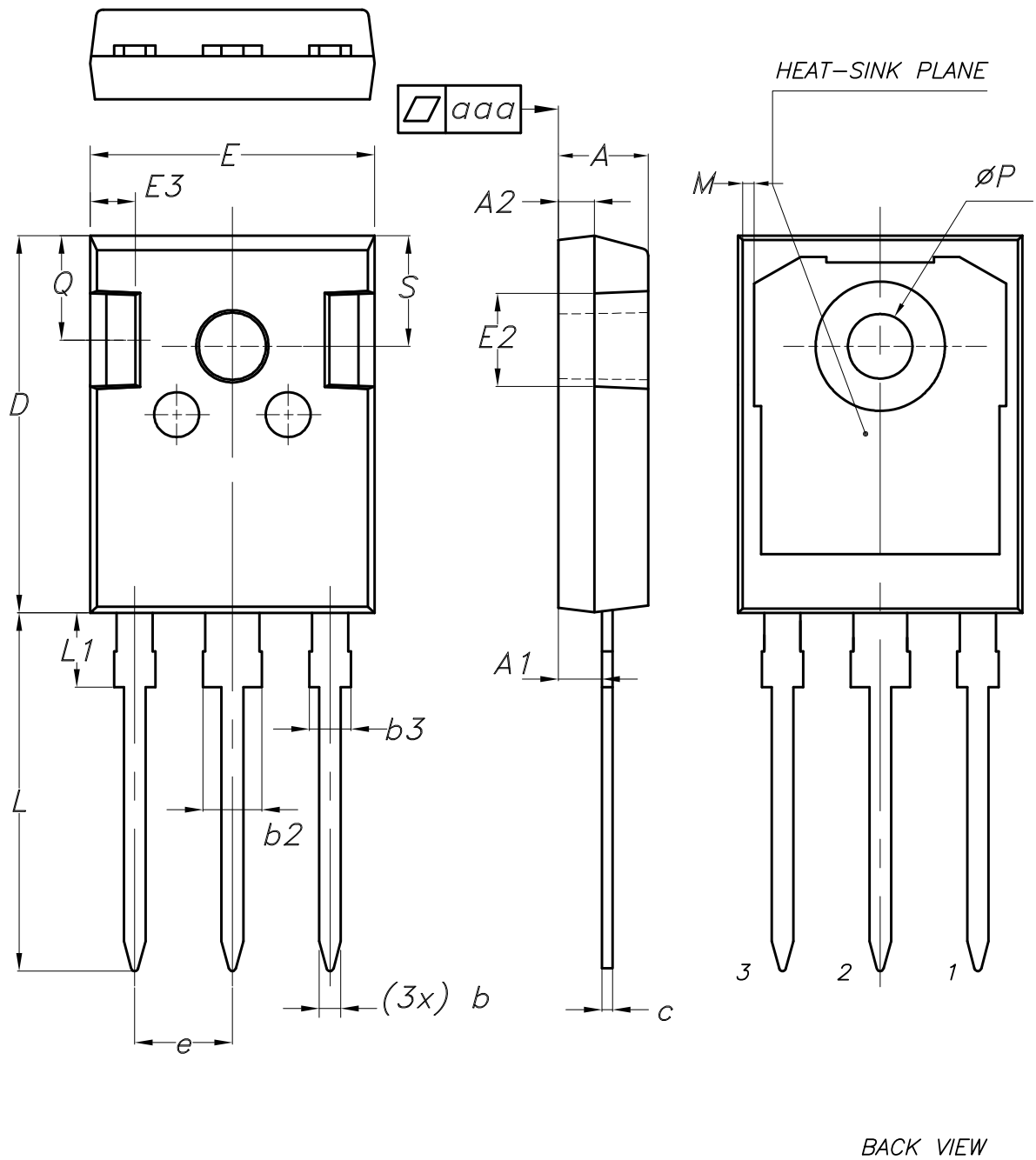
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline



BACK VIEW

8463846_5

Table 8. TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
M	0.35		0.95
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Jan-2025	1	First release.

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