STWA78N65M5AG

Automotive N-channel 650 V, 0.024 Ω typ., 69 A MDmesh M5 Power MOSFET in a TO-247 long leads package

Datasheet - preliminary data

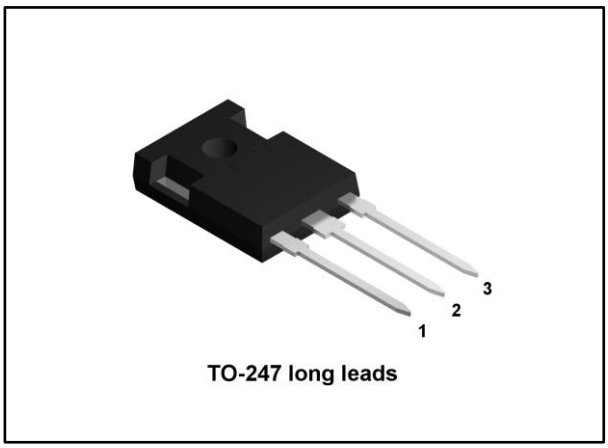
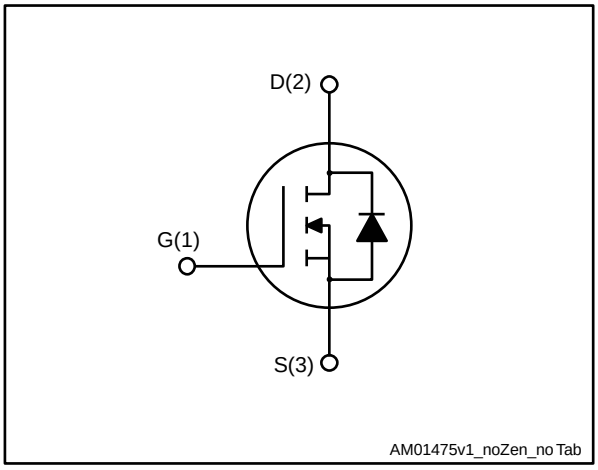


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STWA78N65M5AG	710 V	0.032 Ω	69 A

- Designed for automotive applications
- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STWA78N65M5AG	78N65M5	TO-247 long leads	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	69	A
I_D	Drain current (continuous) at T_C = 100 °C	41.5	A
I_{DM} (1)	Drain current (pulsed)	276	A
P_{TOT}	Total dissipation at T_C = 25 °C	450	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)$I_{SD} \leq 69$ A, di/dt = 400 A/µs, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 400 V

(3)$V_{DS} \leq 520$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.28	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	15	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	2000	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C=125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 34.5 A		0.024	0.032	Ω

Notes:

(1)Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	9000	-	pF
C_{oss}	Output capacitance		-	210	-	pF
C_{rss}	Reverse transfer capacitance		-	9	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	768	-	pf
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	205	-	pf
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	1.5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 34.5 A, V_{GS} = 0 to 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	203	-	nC
Q_{gs}	Gate-source charge		-	50	-	nC
Q_{gd}	Gate-drain charge		-	84	-	nC

Notes:

(1)$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

(2)$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 400 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"* and *Figure 20: "Switching time waveform"*)	-	163	-	ns
$t_{r(V)}$	Voltage rise time		-	14	-	ns
$t_{f(i)}$	Current fall time		-	14	-	ns
$t_{c(off)}$	Crossing time		-	26	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		69	A
I_{SDM}(1)	Source-drain current (pulsed)		-		276	A
V_{SD}(2)	Forward on voltage	I_{SD} = 69 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 69 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	504		ns
Q_{rr}	Reverse recovery charge		-	13		µC
I_{RRM}	Reverse recovery current		-	49		A
t_{rr}	Reverse recovery time	I_{SD} = 69 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	635		ns
Q_{rr}	Reverse recovery charge		-	19		µC
I_{RRM}	Reverse recovery current		-	59		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

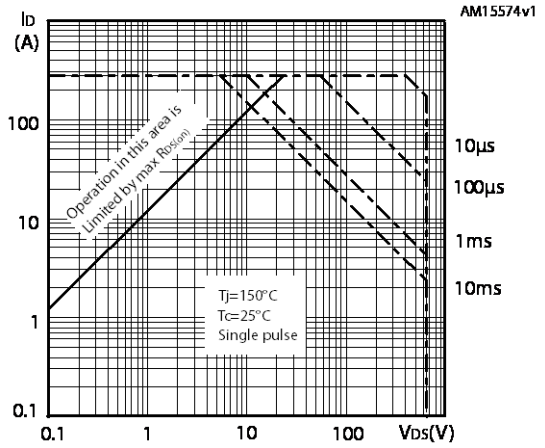


Figure 3: Thermal impedance

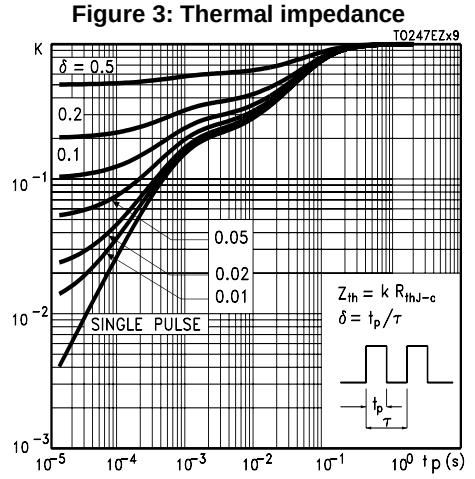


Figure 4: Output characteristics

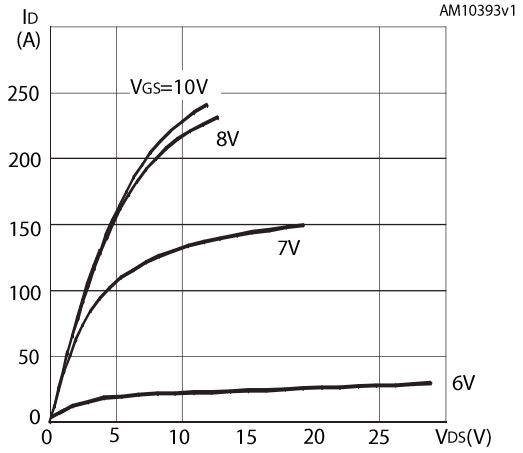


Figure 5: Tranfer characteristics

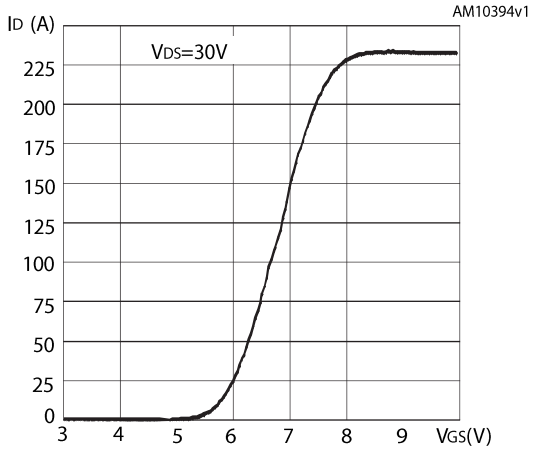


Figure 6: Gate charge vs gate-source voltage

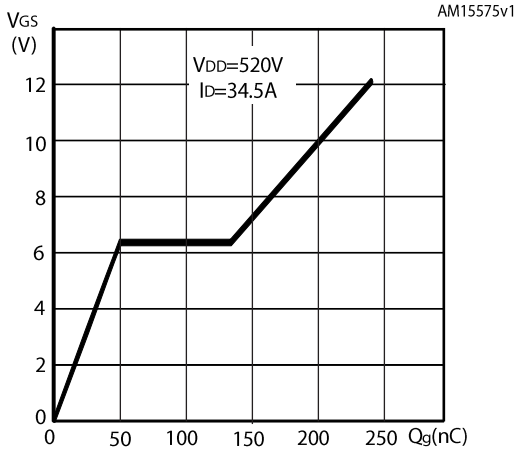


Figure 7: Static drain-source on-resistance

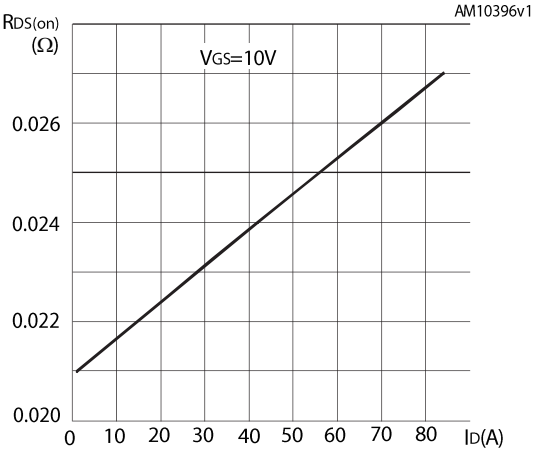


Figure 8: Capacitance variations

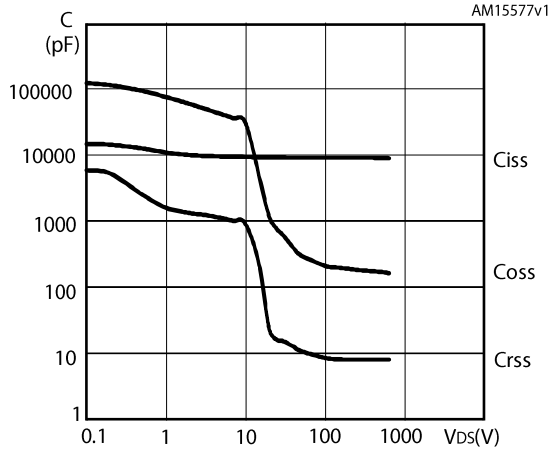


Figure 9: Output capacitance stored energy

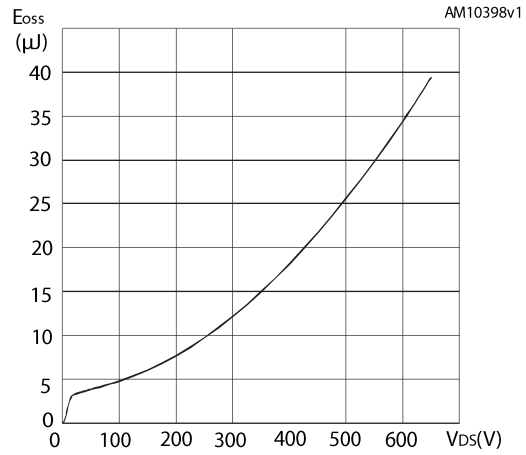


Figure 10: Normalized gate threshold voltage vs temperature

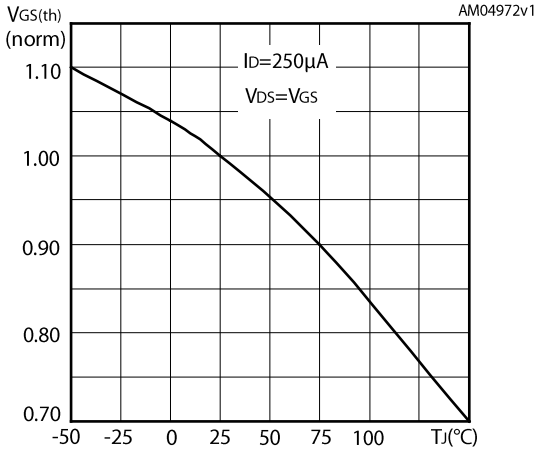


Figure 11: Normalized on-resistance vs temperature

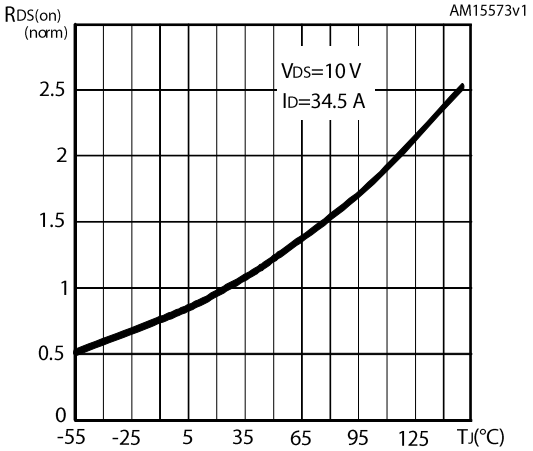


Figure 12: Source-drain diode forward characteristics

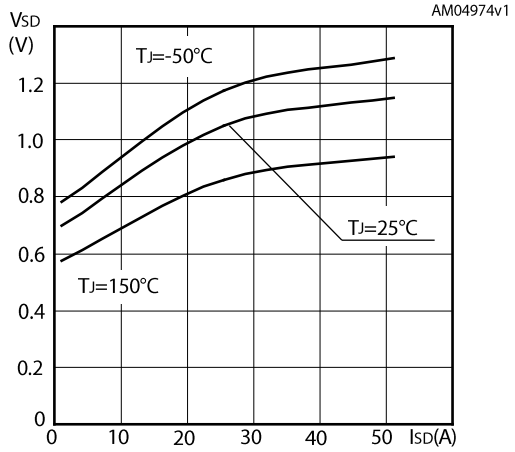


Figure 13: Normalized $V_{(BR)DSS}$ vs temperature

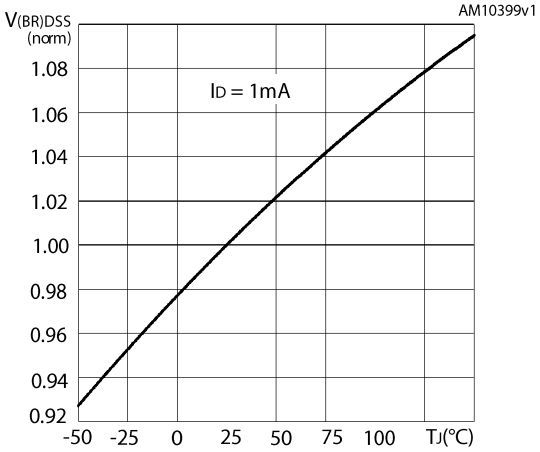
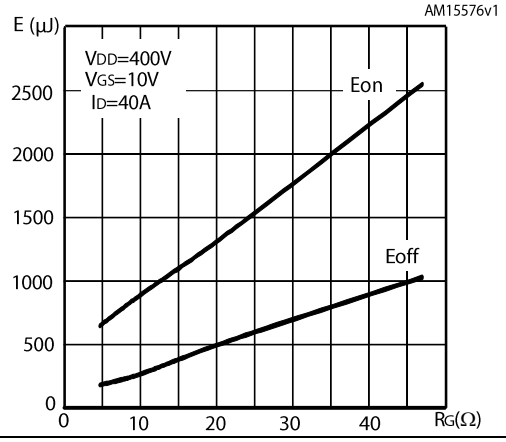


Figure 14: Switching energy vs gate resistance



E_{on} including reverse recovery of a SiC diode.

3 Test circuits

Figure 15: Test circuit for resistive load switching times

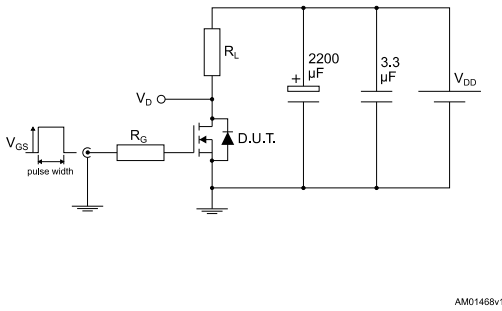


Figure 16: Test circuit for gate charge behavior

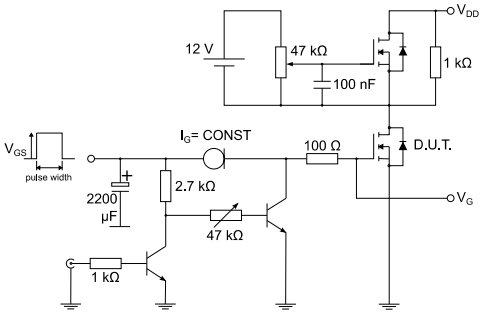


Figure 17: Test circuit for inductive load switching and diode recovery times

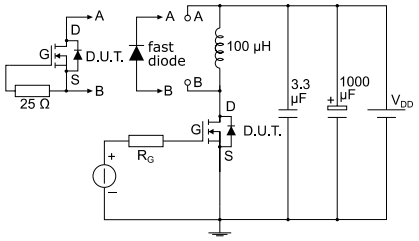


Figure 18: Unclamped inductive load test circuit

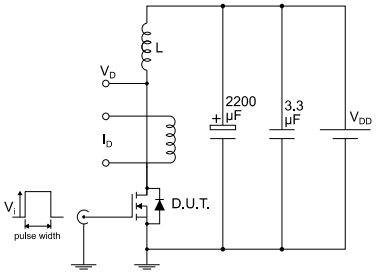


Figure 19: Unclamped inductive waveform

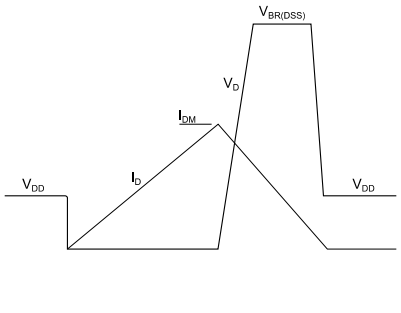
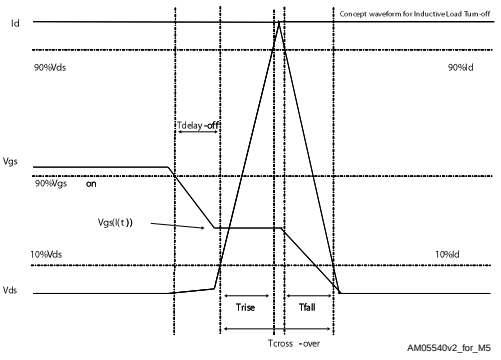


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-247 long leads package information

Figure 21: TO-247 long leads package outline

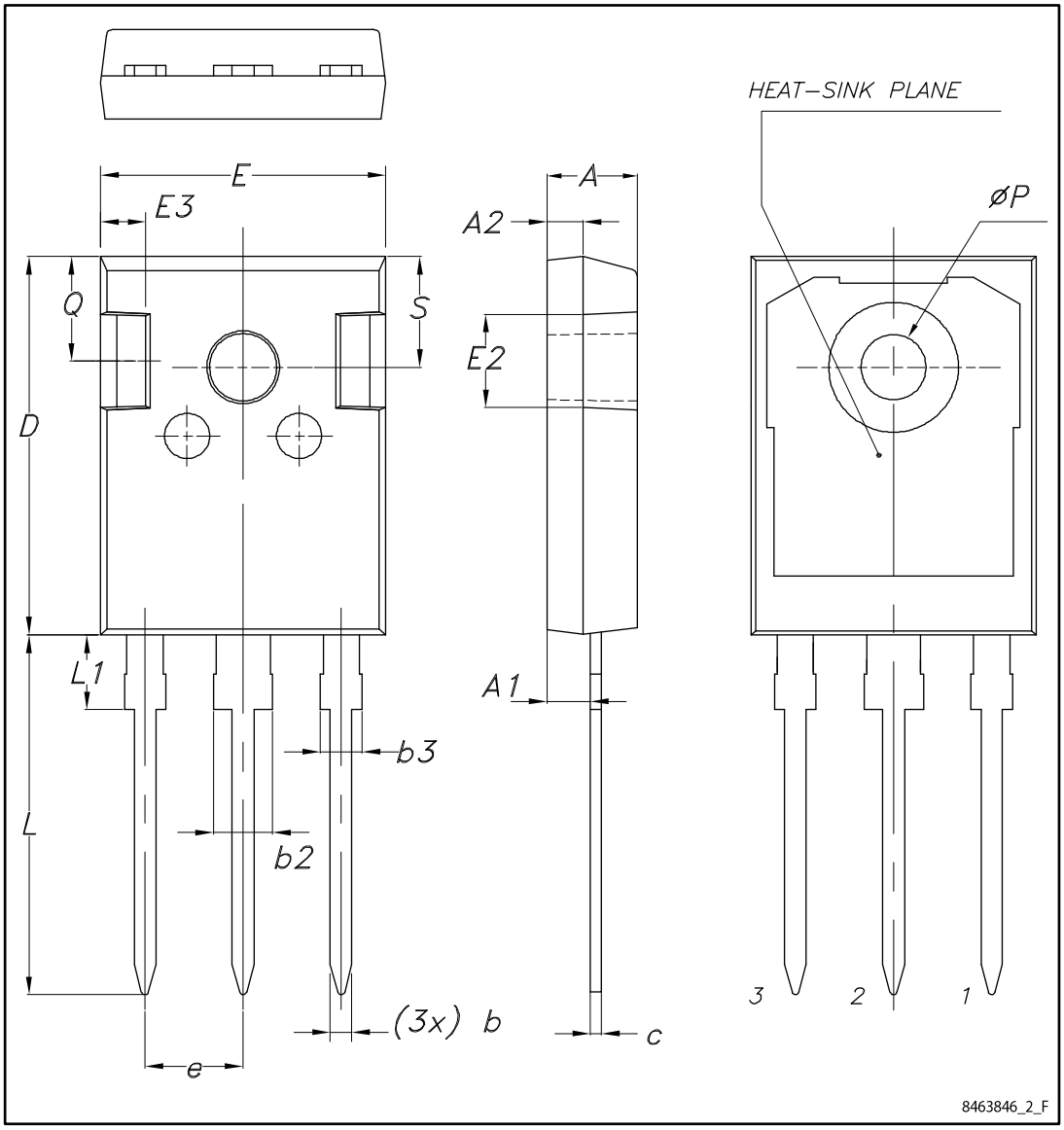


Table 9: TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
14-Aug-2017	1	Initial release.

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