TSC200, TSC201, TSC202

Datasheet

High voltage, current sense amplifier with open drain comparator and ref

MiniSO8

SO8

Maturity status link
TSC200, TSC201, TSC202

Features

- AEC-Q100 qualified
- Wide common-mode voltage: -16 to 80 V
- 2.7 to 18 V supply voltage
- Amplification gain:
  - TSC200: 20 V/V
  - TSC201: 50 V/V
  - TSC202: 100 V/V
- 0.6 V internal reference
- Internal open-drain comparator
- Latching capability on comparator
- High accuracy: 3.5 % max. error vs. temperature
- Bandwidth: 1 MHz (TSC200)
- Quiescent current: 1.8 mA maximum
- SO8 and MiniSO8 package

Applications

- High-side current sensing
- Low-side current sensing
- Overcurrent protection
- Automotive current sensing
- Telecom equipment
- Test and measurement equipment
- Industrial process control

Description

The TSC200, TSC201 and TSC202 are high-side current sense amplifiers which deliver an analog voltage output. They can sense current via a shunt resistor over a wide range of common-mode voltages, from -16 to +80 V, whatever the supply voltage is. They are available with an amplification gain of 20 V/V for TSC200, 50 V/V for TSC201, and 100 V/V for TSC202.

The TSC200, TSC201 and TSC202 integrate an open-drain comparator with output latch function and an internal 0.6 V voltage reference connected to its input. The external resistor divider can then set the switching threshold.

These devices fully operate over the broad supply voltage range of 2.7 to 18 V and over the automotive temperature range of -40 to +125 °C.

1 Block diagram and pin description

Figure 1. Block diagram

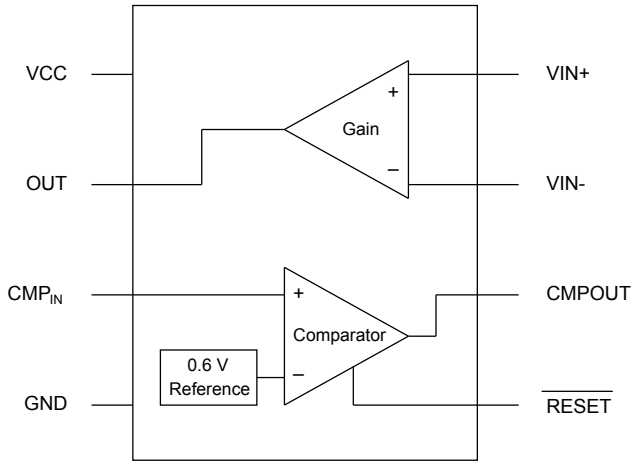


Figure 2. Pin connections (top view)

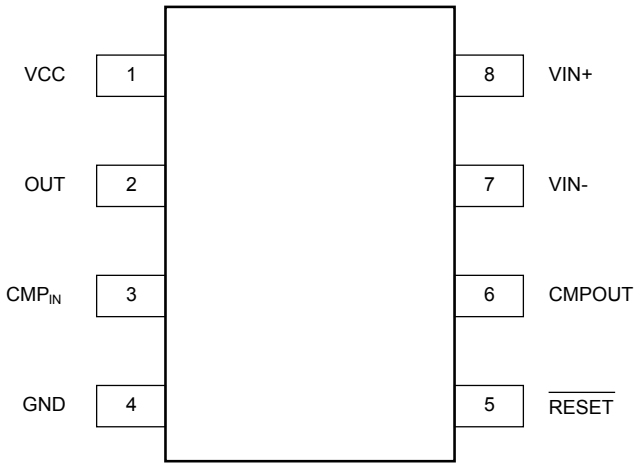


Table 1. Pin description

Pin	Pin name	Description
1	V_{CC}	Supply voltage
2	OUT	Current sense amplifier, output
3	CMP_{IN}	Comparator input
4	GND	Ground
5	RESET	Comparator reset pin, active low
6	CMP_{OUT}	Comparator output
7	V_{IN-}	Current sense amplifier, negative input
8	V_{IN+}	Current sense amplifier, positive input

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		-0.3 to 18.3	V
V_{IN} +, V_{IN-}	Differential voltage (V_{IN+}) – (V_{IN-})		25% V_{CC} (1)	
	Common-mode voltage on input pins		-18 to +82	
CMP_{IN}, RESET	Voltage present on pins V_{IN+}, V_{IN-}, CMP_{IN}, RESET		Gnd -0.3 to Vcc +0.3	V
OUT	Analog output		Gnd -0.3 to Vcc +0.3	
CMP_{OUT}	Voltage present on pin CMP_{OUT}		Gnd -0.3 to 18.3	
I_{IN}	Input current on V_{IN+}, V_{IN-}		5	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature		-65 to 150	°C
ESD	Human Body Model (HBM)		4000	V
	Charged Device Model (CDM)		1000	
R_{THJA}	Thermal resistance junction to ambient	SO8	125	°C/W
		MiniSO8	190	

1. *For V_{CC} ≥ 12 V, Vdiff must not exceed 3 V.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 18	V
V_{ICM}	Common-mode voltage on input pins	-16 to +80	V
T	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 4. Electrical characteristics of the Current sense amplifier at V_{CC} = 12 V, V_{ICM} = 12 V, V_{Sense} = 100 mV, R_L = 10 kΩ to GND, $R_{pull-up}$ = 5.1 kΩ connected from CMP_{OUT} to V_{CC}, CMP_{IN} = GND, T = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input						
V_{Sense}	Full scale sense input voltage			0.15	$\frac{V_{CC}-0.25}{Gain}$	V
V_{ICM}	Common-mode input range	Tmin < T < Tmax	-16		80	V
CMR	Common-mode rejection	V_{IN}+ = -16 to 80 V,	80	110		dB
		V_{IN}+ = 12 to 80 V, Tmin < T < Tmax	100	120		
Vos	Offset voltage, RTI (1) (2)	T = 25 °C	-2.5	±0.1	+2.5	mV
		25 °C < T < Tmax	-3		+3	
		Tmin < T < 25 °C	-3.5		+3.5	
|ΔVos/ΔT|	Offset drift (RTI) vs. temperature	Tmin < T < Tmax		0.5		µV/°C
SVR	Supply voltage rejection, RTI	V_{OUT} = 2 V, V_{IN}+ = 18 V, V_{CC} = 2.7 to 18 V,Tmin < T < Tmax		3	100	µV/V
I_{IB}	Input bias current, V_{IN-} pin	Tmin < T < Tmax		±0.5	±16	µA
Output (V_{Sense} ≥ 20 mV)						
G	Gain	TSC200 TSC201 TSC202		20 50 100		V/V
E_G	Gain error	V_{Sense} = 20 to 100 mV Tmin < T < Tmax		±0.05	±1 ±2	%
TE_G	Total output error (3)	V_{Sense} = 120 mV, V_{CC} = 16 V Tmin < T < Tmax		±0.1	±2.2 ±3.5	%
NLE	Non linearity error	V_{Sense} = 20 to 100 mV		±0.002		%
R_O	Output impedance			1.5		Ω
C_{Load}	Maximum capacitive load	No sustained oscillation		10		nF
Output (V_{Sense} < 20 mV)						
Output	TSC200, TSC201, TSC202	-16 ≤ V_{ICM} < 0 V		300		mV
	TSC200 TSC201 TSC202	0 ≤ V_{ICM} ≤ Vcc, V_{CC} = 5 V			400 1000 2000	
	TSC200, TSC201, TSC202	Vcc < V_{ICM} ≤ 80 V		300		
Voltage output						
V_{OH}	Output swing to the positive rail	V_{IN-} = 11 V, V_{IN}+ = 12 V, Tmin < T < Tmax		V_{CC} - 0.15	V_{CC} - 0.25	V
V_{OL}	Output swing to GND	V_{IN-} = 0 V, V_{IN}+ = -50 mV, Tmin < T < Tmax TSC200 TSC201 TSC202		4	50 65 100	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dynamic performances						
BW	C_{Load} = 5 pF	TSC200 TSC201 TSC202		1 0.4 0.3		MHz
SR	Slew rate			7		V/µs
Ts	Settling time	V_{Sense} = 10 to 100 mVpp Up to 1 % final value, C_{Load} = 5 pF		2		µs
Noise, RTI						
E_N	Voltage noise density	f = 100 kHz		55		nV/√Hz
Power supply						
I_{CC}	Current consumption	V_{OUT} = 2 V		0.84	1.8	mA
		V_{Sense} = 0 mV, Tmin < T < Tmax			1.85	
C_POR	Comparator POR threshold (4)			1.5		V

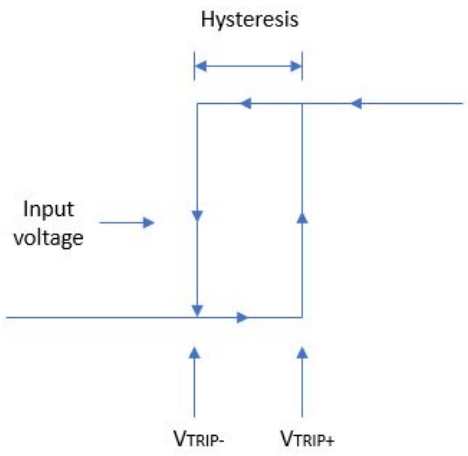
1. *RTI stands for "Related to input".*
2. *Offset is extrapolated from measurements of the output at V_{Sense} of 20 mV and 100 mV.*
3. *Total output error considers effects of gain error and V_{OS} inaccuracy.*
4. *The TSC200, TSC201 and TSC202 are designed to power up with the comparator in a defined reset state as long as RESET is open or grounded. The comparator is in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If RESET is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.*

Table 5. Electrical characteristics of the Comparator at V_{CC} = 12 V, V_{ICM} = 12 V, V_{Sense} = 100 mV, R_L = 10 kΩ to GND, $R_{pull-up}$ = 5.1 kΩ connected from CMP_{OUT} to V_{CC}, T = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input						
V_{TH}	Threshold	T = 25 °C	590	608	620	mV
		Tmin < T < Tmax	586		625	
Hyst	Hysteresis (1)	Tmin < T < Tmax		-9		
I_{IB}	Input bias current, CMP_{IN} pin (2)	T = 25 °C		0.005	10	nA
		Tmin < T < Tmax			15	
V_{IN}	Input voltage range, CMP_{IN} pin		0		V_{CC} -1.5	V
Output (open-drain)						
Av	Large signal differential voltage gain	CMP_{OUT} from 1 to 4 V R_L ≥ 15 kΩ connected to 5 V		200		V/mV
I_{OH}	High level leakage current (3) (4)	V_{ID} = 0.4 V, V_{OH} = V_{CC}		0.0001	1	µA
V_{OL}	Low level output voltage (3)	V_{ID} = -0.6 V, I_{OL} = 2.35 mA		140	300	mV
Response time						
T_P	Response time (5)	R_L to 5 V, C_{Load} = 15 pF, 100 mV input step with 5 mV overdrive		0.3		µs
$\overline{RESET}$						
V_T	$\overline{Reset}$ threshold (6)			1.1		V
R_I	Input impedance			2		MΩ
T_{DW}	Minimum $\overline{Reset}$ pulse width			0.1		µs
T_D	Propagation delay			0.1		µs

1. *See Figure 3 for details, Hysteresis=V_{TRIP}- - V_{TRIP}+.*
2. *Specified by design.*
3. *V_{ID} is the differential voltage present at the comparator inputs.*
4. *Open-drain output can be pulled up to 2.7~18 V range, regardless of V_{CC}.*
5. *The comparator response time specified is the time interval between the input step and the instant when the output crosses 1.4 V.*
6. *The RESET input has an internal 2 MΩ (typical) pull-down. In case RESET pin is left open, the output shows a LOW state, with transparent comparator operation.*

Figure 3. Typical comparator hysteresis



4 Typical performance characteristics

T = 25 °C, V_{CC} = 12 V, V_{IN+} = 12 V and V_{Sense} = 100 mV (unless otherwise specified).

Figure 4. Gain vs. frequency (C_L = 1000 pF)

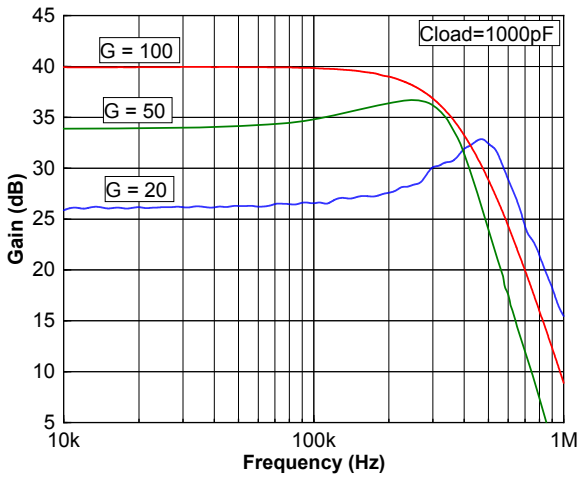


Figure 5. Gain vs. frequency (C_L = 100 pF)

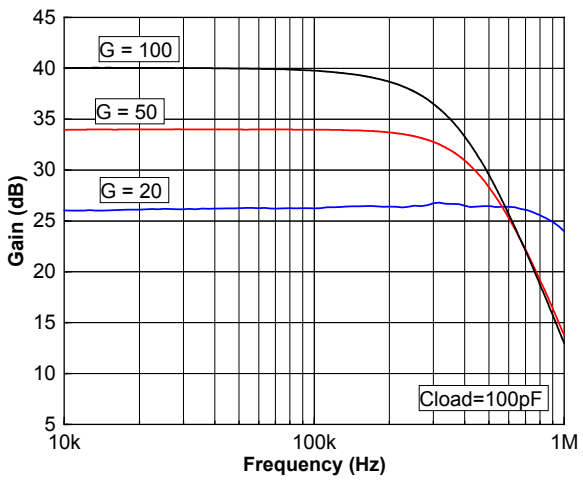


Figure 6. Gain plot

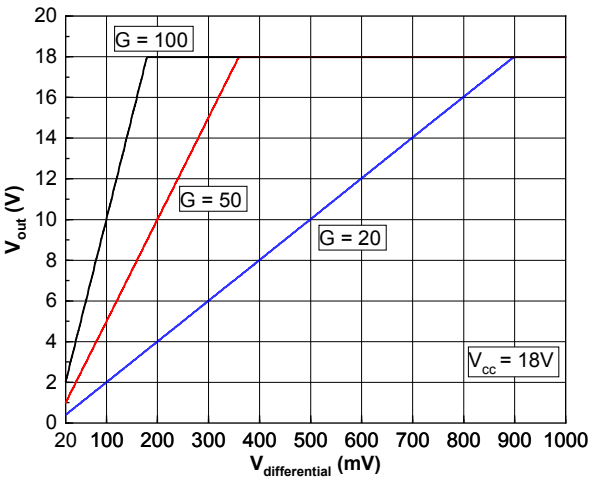


Figure 7. CMRR and PSRR vs. frequency

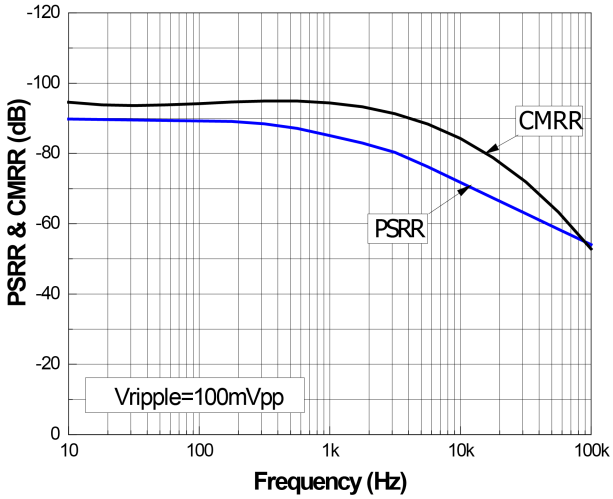


Figure 8. Output error vs. V_{sense}

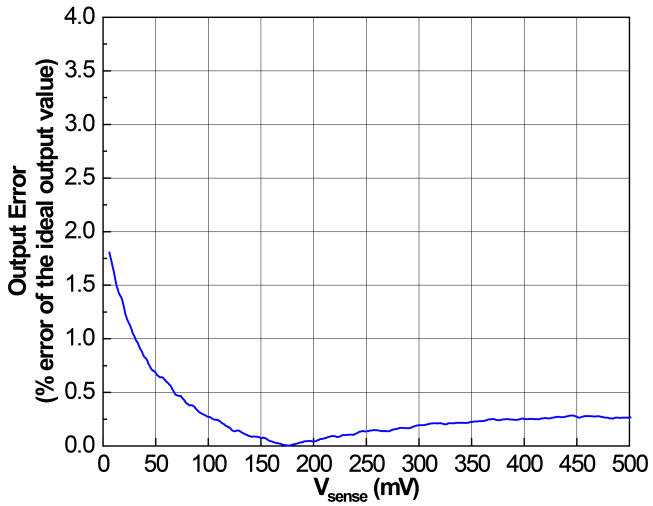


Figure 9. Output error vs. common-mode voltage

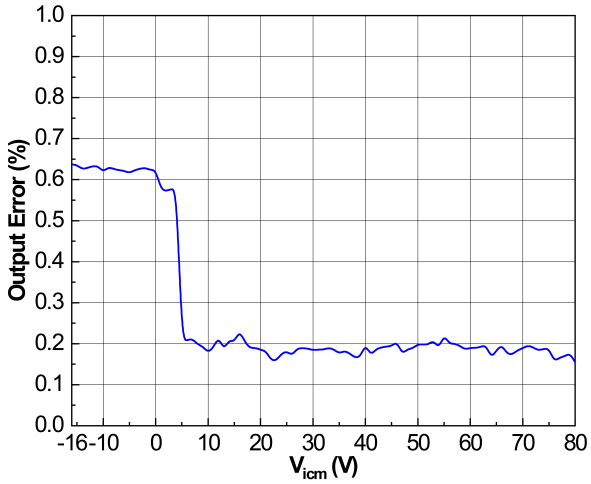


Figure 10. Output current vs. output voltage at V_{CC} = 2.7 V

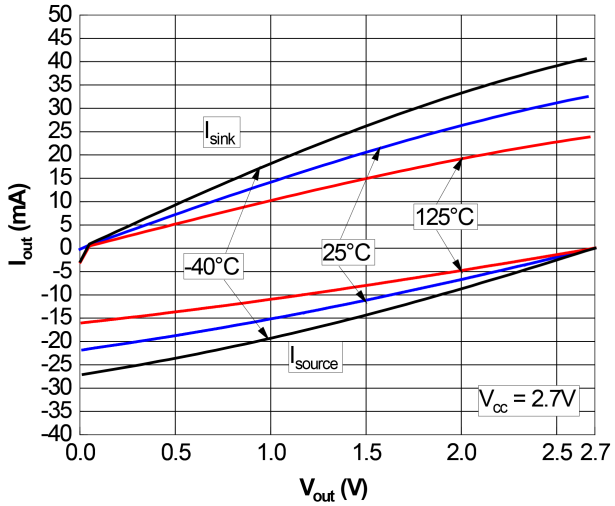


Figure 11. Output current vs. output voltage at V_{CC} = 12 V

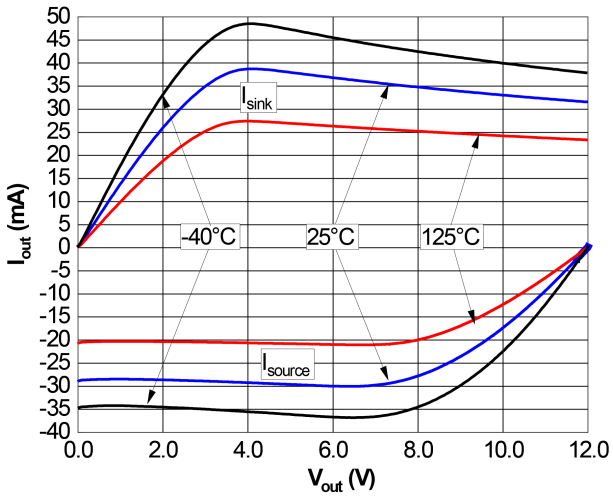


Figure 12. Quiescent current vs. output voltage

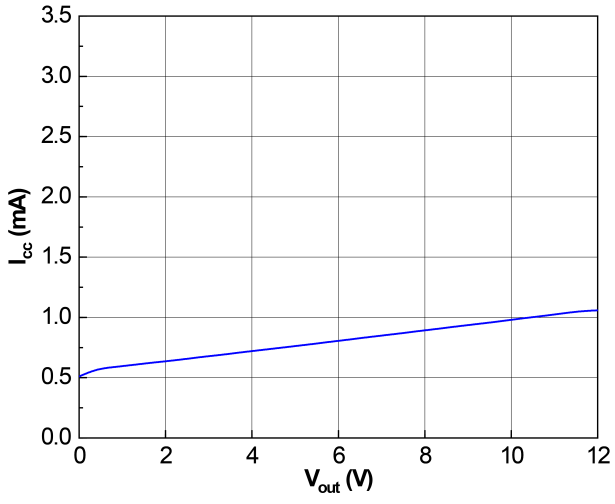


Figure 13. Quiescent current vs. common-mode voltage

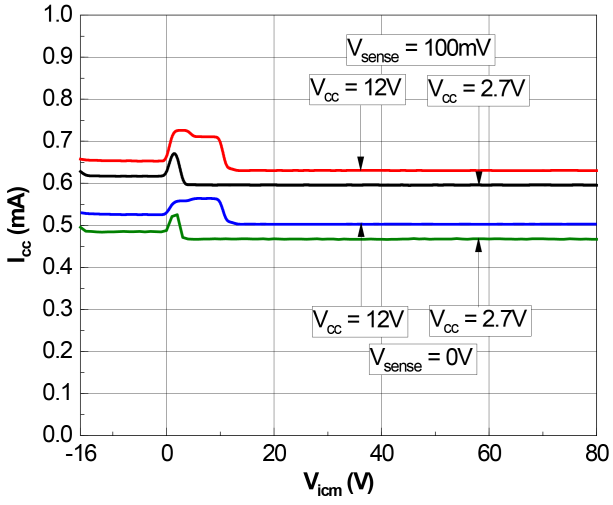


Figure 14. Output short-circuit current vs. supply voltage

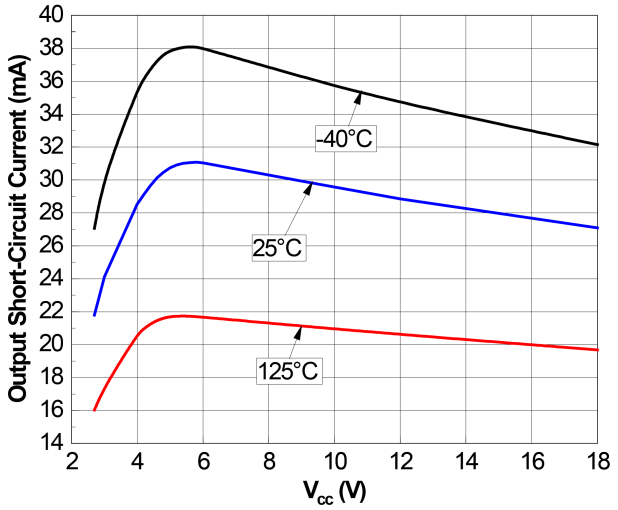


Figure 15. Step response for 20 to 30 mV V_{sense} G = 20

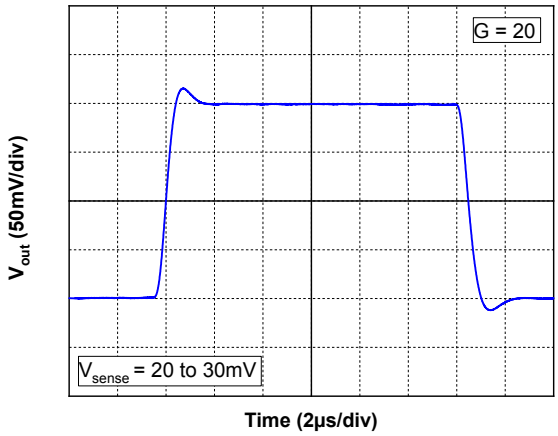


Figure 16. Step response for 20 to 110 mV V_{sense} G = 20

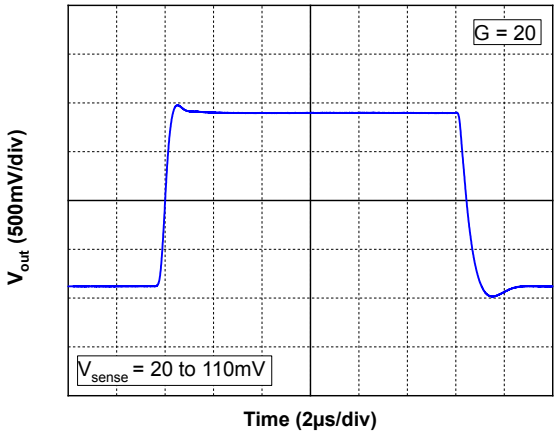


Figure 17. Step response for 90 to 100 mV V_{sense} G = 20

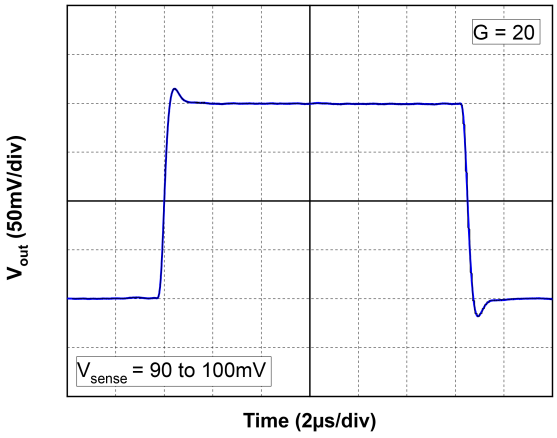


Figure 18. Step response for 20 to 30 mV V_{sense} G = 50

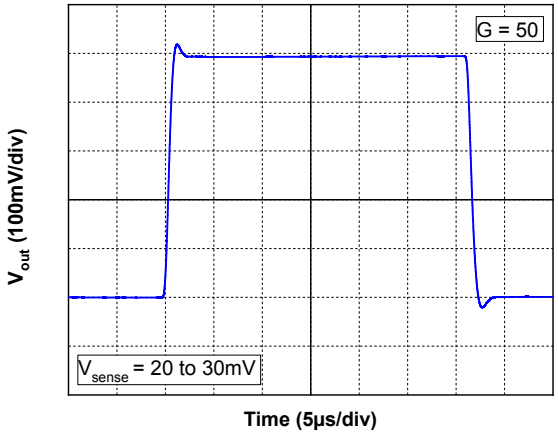


Figure 19. Step response for 20 to 110 mV V_{sense} G = 50

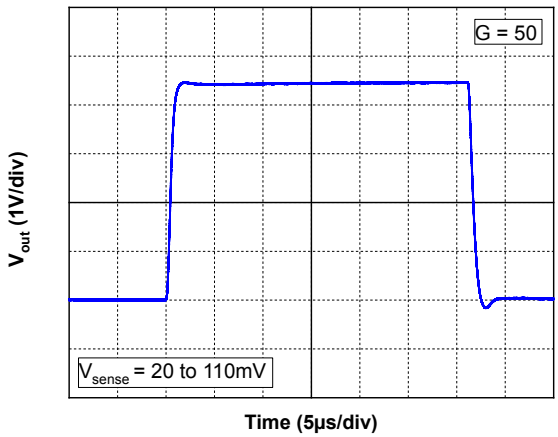


Figure 20. Step response for 90 to 100 mV V_{sense} G = 50

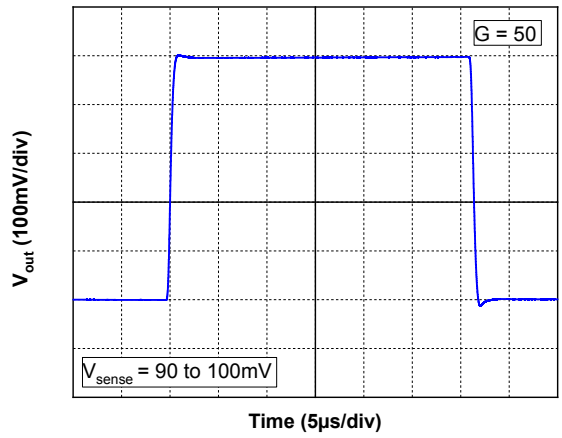


Figure 21. Step response for 20 to 110 mV V_{sense} G = 100

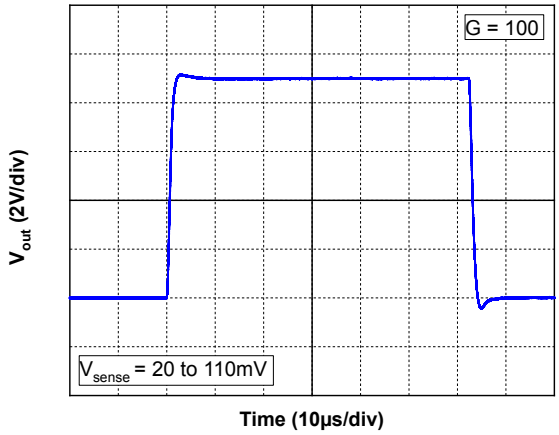


Figure 22. Comparator V_{OL} vs. I_{SINK}

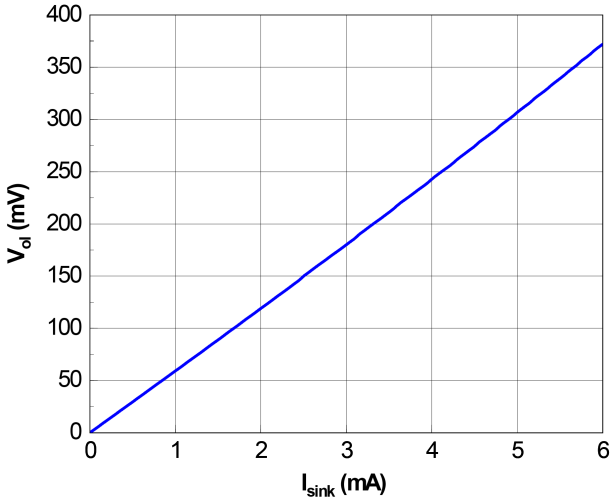


Figure 23. Comparator trip points vs. V_{CC}

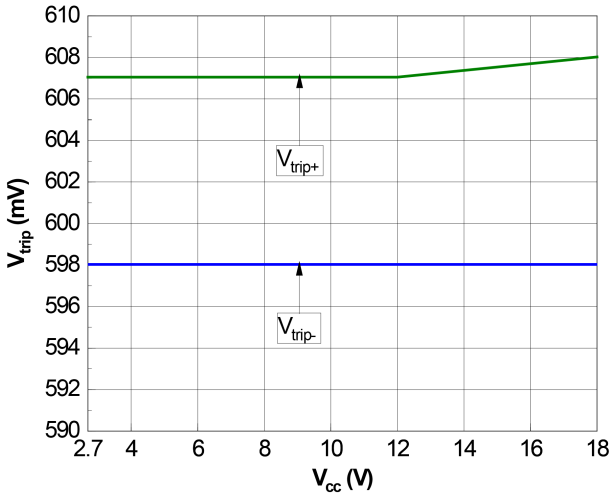


Figure 24. Comparator trip points vs. temperature

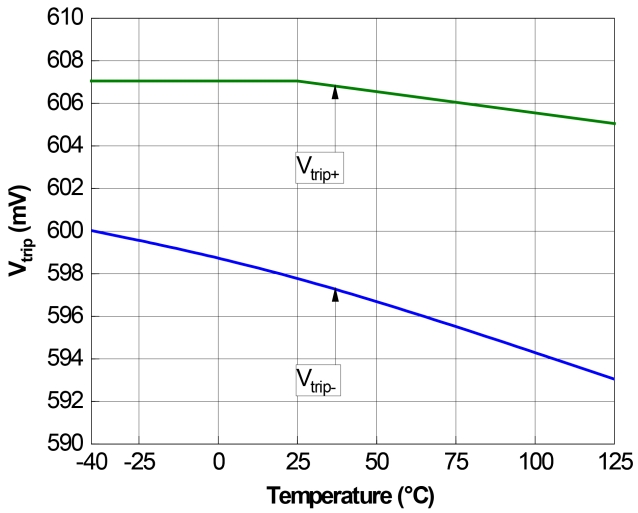


Figure 25. Comparator reset voltage vs. V_{CC}

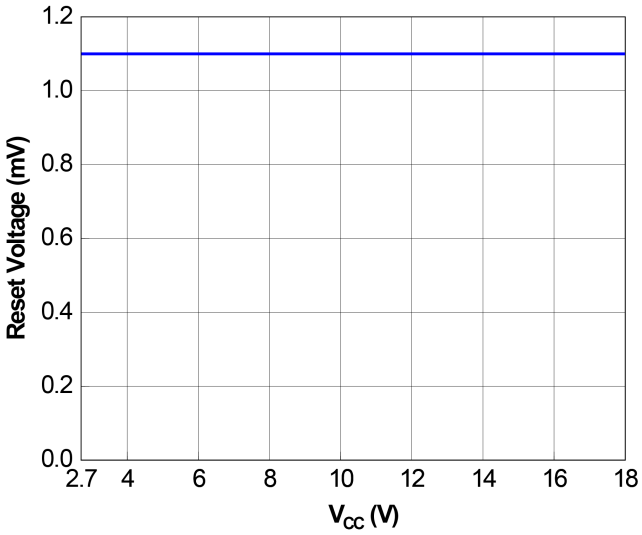


Figure 26. Comparator propagation delay vs. overdrive voltage

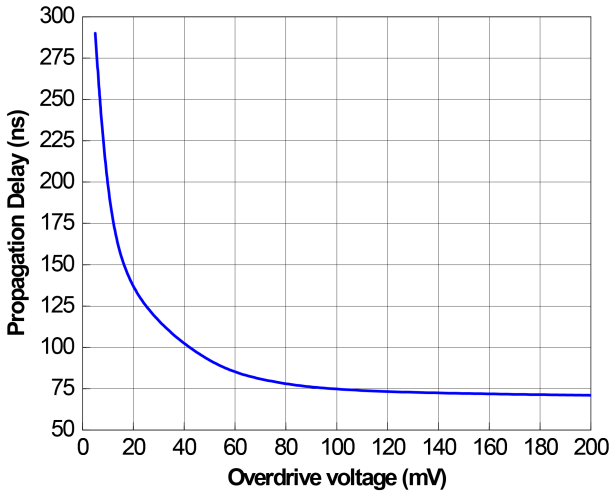


Figure 27. Comparator propagation delay vs. temperature

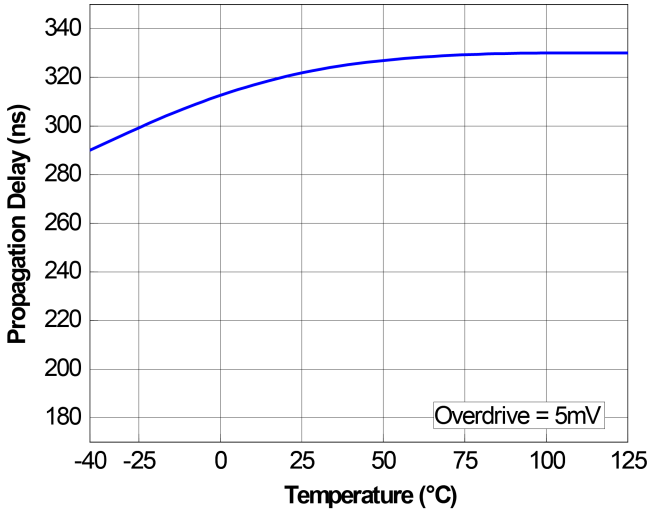
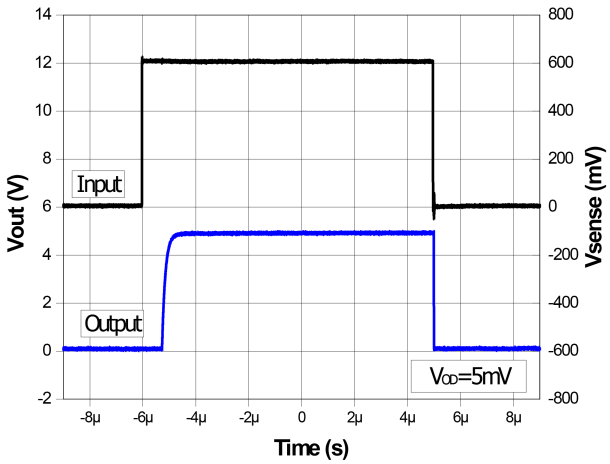


Figure 28. Comparator propagation delay



5 Application information

5.1 Overview

The TSC200, TSC201, and TSC202 devices are designed to measure current by amplifying the voltage across a shunt resistor connected to its input. Thanks to a bandgap reference and a comparator, which is able to latch the output, the TSC20x family is the perfect candidate for overcurrent protection.

TSC200, TSC201, and TSC202 are current-sensing amplifiers with a respective gain of 20 V/V, 50 V/V, and 100 V/V. They provide an extended input common range from -16 V up to 80 V, while the devices can operate from 2.7 to 18 V. They can operate either as low side or high side current sensing amplifiers.

The parameters are very stable in the full V_{CC} range, and several characterization curves show the characteristics of the TSC20x devices at 12 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to 125 °C.

5.2 Theory of operation

The main feature of the TSC200, TSC201, and TSC202 is the ability to work with an input common-mode voltage largely beyond the power supply V_{CC} range (2.7 V to 18 V). It is ideal, for example, in wireless infrastructure equipment to monitor the current flowing into a power amplifier. The integrated comparator and reference output allows for an overcurrent protection implementation.

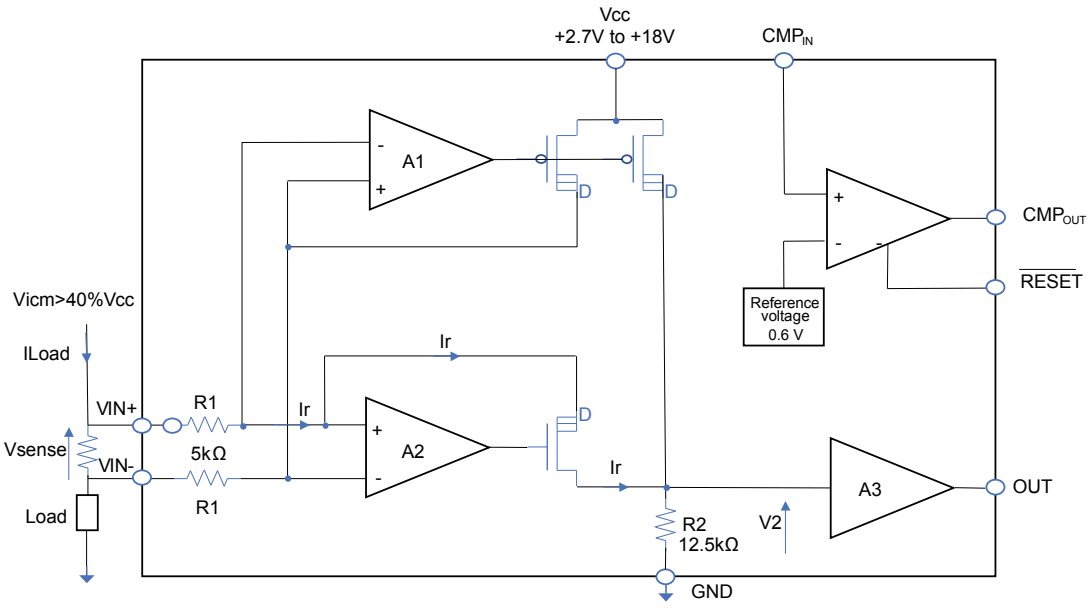
The internal topology used in the TSC200, TSC201, and TSC202 is different from a classic instrumentation amplifier approach. The TSC20x family offers a high CMRR, without any special care towards the internal resistance matching and low input bias current.

Nevertheless, this topology implies three operation functional modes for the TSC20x. These modes are a function of two main variables: the differential input voltage V_{sense} (resulting in a current flowing into the shunt resistance) and the input common-mode voltage Vicm, relative to the supply voltage V_{CC}.

Mode 1: V_{sense} > 20 mV and V_{icm} > 40% V_{CC}

Figure 29 depicts a simplified diagram, explaining the main functional principle of TSC20x for the mode 1 operation.

Figure 29. Simplified diagram when V_{icm} > 40% V_{CC}



When the input common-mode voltage is higher than 40% of the V_{CC}, the amplifier A2 is active. An Iload current flowing into the shunt generates V_{sense}, a small differential voltage between TSC20x's input pins. Due to the A2 amplifier, a current Ir flows through the input pin IN+. This current Ir is equal to V_{sense}/5 kΩ and is converted through R2, into the voltage V2 as described in equation 1.

$$V2 = 2.5 * Vsense \quad (1)$$

It is finally amplified by the A3 amplifier.

$$Vout = V2 * A3 \quad (2)$$

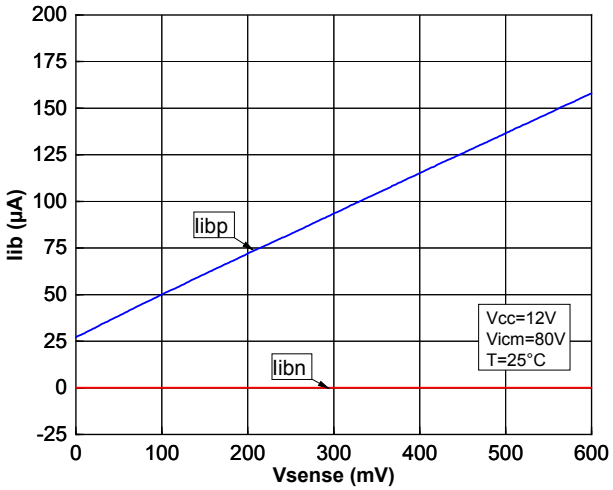
In case of TSC200 A3 = 8

In case of TSC201 A3 = 20

In case of TSC202 A3 = 40

The input bias current of IN+ is composed of the supply current of the input stage (roughly 30 µA), as well as Ir. The value of Ir is directly linked to the sensing voltage Vsense. Figure 30 shows the sum of bias current into the input pins.

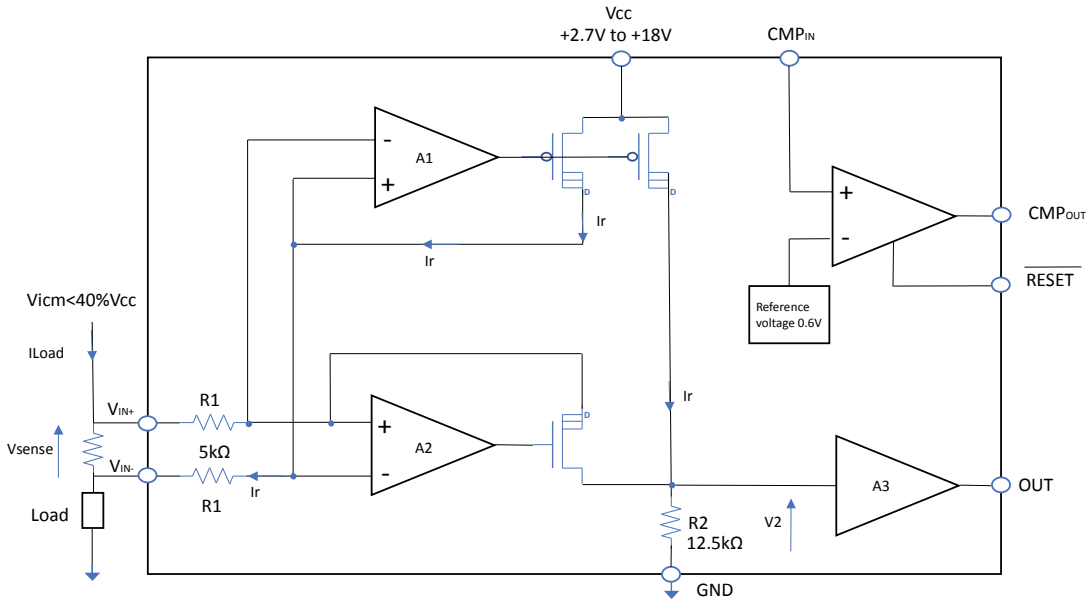
Figure 30. Input bias current vs. V_{sense} for a V_{icm} = 80 V



Mode 2: V_{sense} > 20 mV and V_{icm} < 40% V_{CC}

Figure 31 depicts a simplified diagram, explaining the main functional principle of TSC20x for the mode 2 operation.

Figure 31. **Simplified diagram when V_{icm} < 40% V_{CC}**

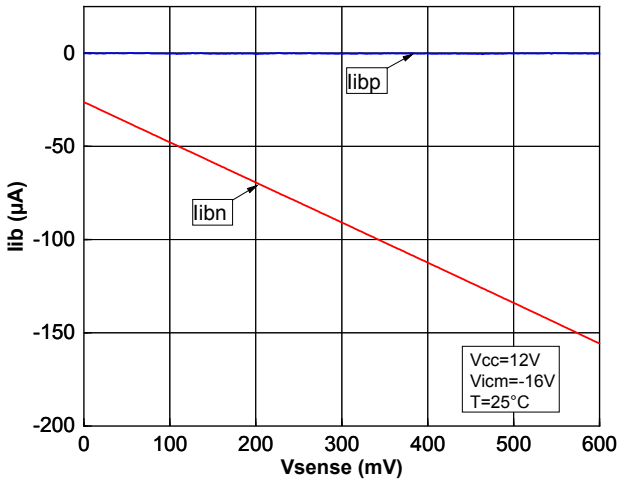


When the input common-mode voltage is lower than 40% of the Vcc, this time the amplifier A1 is active. A Iload current flowing into the shunt generates Vsense, a small differential voltage between input pins of the TSC20x. Due to the A1 amplifier, a current Ir, equal to Vsense/5kΩ, flows through the input pin IN-. This Ir current is recopied from a precision current mirror whose output is directed into R2, converting the signal back into a voltage V2 as described by equation 1, and then amplified by the A3 amplifier as described by equation 2.

The input bias current of IN- is composed of the supply current of the input stage (roughly 30 µA), as well as the Ir. The value of Ir is directly linked to the sensing voltage Vsense.

Figure 32 shows the sum of bias current into the input pins.

Figure 32. **Input bias current vs. V_{sense} for a V_{icm} = -16 V**



In mode 2 the accuracy might be slightly lower than in mode 1 as described by Figure 9. That difference is principally due to the current Ir recopy.

Mode 3: V_{sense} < 20 mV over the V_{icm} range

The TSC20x has not been designed to measure extremely low current, or rather low input differential voltage. When the voltage across the shunt resistor becomes lower than 20 mV, a larger than normal offset can appear. For example, for the TSC200, an output voltage V_{out} = 0.4 V max can be measured while the V_{sense} = 0 V, which leads to output errors higher than expected.

As seen in the previous chapter, the way the TSC20x family works is to transform a small differential input Vsense into a proportional current Ir, and then amplify it through the internal resistance R2.

But when the V_{sense} voltage is too low, the Ir current becomes very low as well and the transconductance of the transistor becomes very low, as a consequence of a loss of precision for V_{sense} < 20 mV.

Figure 33 and Figure 34 describe the output voltage distribution of a large amount of TSC200 samples when the differential input voltage V_{sense} = 0 V, for a input common voltage V_{icm} = 0 V and V_{icm} = 12 V.

Figure 33. V_{OUT} when V_{sense} = 0 V, V_{CC} = 5 V, V_{icm} = 0 V

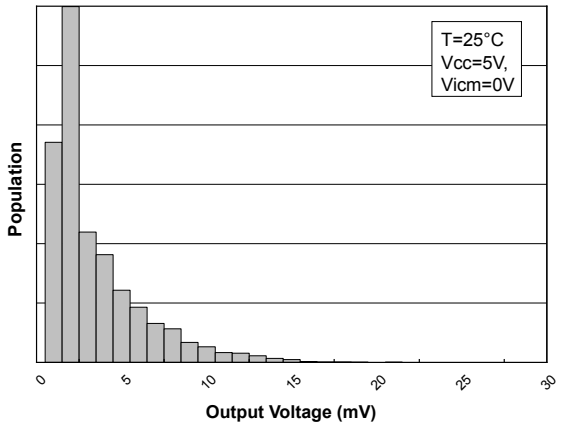
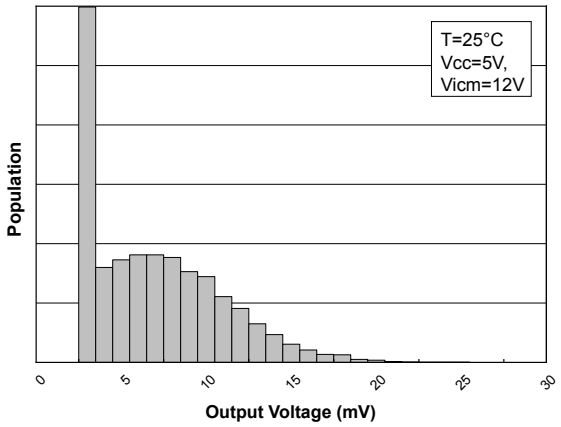


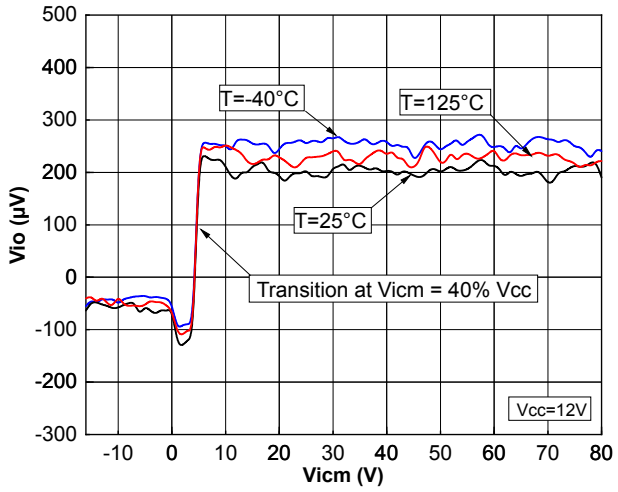
Figure 34. V_{OUT} when V_{sense} = 0 V, V_{CC} = 5 V, V_{icm} = 12 V



V_{icm} = 40% V_{CC}

The transition V_{icm} = 40% V_{CC} is the most sensitive one as it is a transition between the A1 and A2 amplifiers. While the architecture has been optimized to smooth this transition, a change in V_{io} can be observed at this step, as demonstrated in Figure 35.

Figure 35. Input voltage offset over V_{icm} and temperature



The transition between amplifiers A1 and A2 can also be observed on a dynamic signal, when the common mode voltage varies around a V_{icm} = 40% V_{CC}.

5.3 Rsense selection

The selection of the shunt resistor is a tradeoff between dynamic range and power dissipation.

Generally, in high current sensing applications, the focus is to reduce the power dissipation (RI²) as much as possible by choosing the lowest shunt value. It is quite easy if the full-scale current to be measured is low.

In low current application, the Rsense value could be higher to minimize the impact of the offset voltage of the circuit. Keep in mind that due to the input bias of several µA the TSC20x cannot measure current in the same range.

The tradeoff is mainly when the dynamic range of current to be measured is large, meaning there is an ability to measure with the same shunt value low current to high current. Generally, the current full scale Imax defines the shunt value thanks to the full output voltage range, the gain of the TSC20x.

At first order, the full current range to measure through Rsense can be defined by equation 3, just by taking the gain error and input offset voltage as inaccuracy parameters:

$$Isense_full_scale*Rsense = \frac{Vcc - 250mV}{TSC_Gain(1 + Eg)} - \left|Vio\right| \quad (3)$$

Its purpose is to highlight that the product Rsense * TSC_gain is determined by the application, and that once one of these two parameters is selected, the maximum value of the second one can be calculated.

5.4 Input offset voltage drift vs. temperature

The maximum input offset voltage drift vs. temperature is defined as the offset variation related to the offset value measured at 25 °C. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift vs. temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift vs. temperature is computed using equation 4.

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right| \quad (4)$$

Where T = -40 °C and 125 °C.

The TSC20x datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.5 Error calculation

The principal sources of errors such as input offset voltage, gain error, and common-mode rejection ratio are described separately in the electrical characteristic section. This chapter summarizes the most important errors to take into account during a design phase.

- Input offset voltage error

Equation 5 depicts a first order error calculation taking into account the input offset voltage. In an environment with unstable temperature, it is important to consider the deviation of the Vio. The error linked to the input offset on the output voltage can be written as equation 5:

$$Vio\ Error = [\pm Vio \pm (Dvio/DT)*\Delta T]*Gain \quad (5)$$

- Gain error and shunt resistance accuracy

$$Gain\ error = Gain(1 + \varepsilon gain) \quad (6)$$

$$Rsense\ error = Gain(1 + \varepsilon Rsense) \quad (7)$$

Where Ɛgain is the gain error 2% max for the TSC20x.

Where ƐRsense is the shunt resistance error. Shunt resistors from 5 mΩ to 100 mΩ are available within 1% accuracy or better.

- CMR error

In the electrical characteristics, CMR is specified at one input common-mode voltage. To take into consideration the variation of the input voltage offset depending on Vicm, the calculus must be done from this known point. In the electrical characteristics all the parameters are defined at Vicm = 12 V, so it must be taken as the reference point.

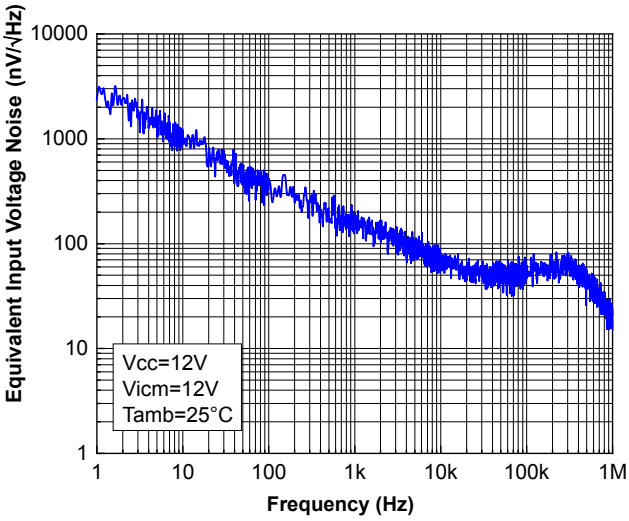
The error on output voltage V_{out} due to a common-mode voltage variation can be written as the equation 8:

$$CMR\ error = \pm \frac{Vicm - 12V}{CMR} * Gain \quad (8)$$

- Noise

Figure 36 expresses the noise referred to the input of the TSC200 over the frequency:

Figure 36. Input referred noise vs. frequency



This device shows a 1/f noise until 30 kHz frequency. Above this limit, the white noise density is 55 nV/√Hz, until the bandwidth of the TSC200.

The noise can then be expressed in two terms, the first one related to the 1/f noise, and the second due to the white noise. If we consider that there is no additional filter on the TSC200, and it is only bandwidth limited, it can be considered that over 1 MHz, there is an attenuation of the noise with a first order filtering. So, the equivalent noise bandwidth is $1\ MHz.\frac{\pi}{2}$.

The RMS value of the output noise is the integration of the spectral noise over the bandwidth of interest and can be expressed as equation 9:

$$enRMS = \left(\sqrt{\int_{0.1}^{30000} \left(\frac{55.10^{-9}}{\sqrt{\frac{f}{30.10^{3}}}} \right)^{2} df + \int_{0.1}^{1000000.\frac{\pi}{2}} \left(55.10^{-9}\right)^{2} df} \right) * Gain \quad (9)$$

- Total error

The maximum total error expected on the output of the device can be expressed as the sum of the different sources described just above. The total output accuracy can be written as equation 10.

$$Vout_{err} = Gain * Rsense * |Iload| (\varepsilon gain + \varepsilon Rsense) + Gain.|Vio| + Gain . \frac{|Vicm - 12V|}{CMR} + noise \quad (10)$$

Iload is the current flowing into the shunt, and output noise is described by equation 9.

Equation 10 has been described for a temperature of 25 °C. With any temperature variation, ΔVio/dT error term must be added. Furthermore, if the power supply is susceptible to change, the SVR parameter must also be considered.

- Example

The example below allows for a better understanding of the maximum total error that can happen on the output of the TSC200.

- Use case:
  - Vcc = 5 V
  - Vicm = 48 V
  - Temperature = 25 °C
  - Iload = 5 A
  - Shunt 20 mΩ with 1% accuracy

Theoretically, the expected output voltage should be V_{out} = Rshunt * Iload * 20 = 2 V.

From the above equations, all the error terms by using the maximum value of the electrical characteristic (when available) are detailed in order to express as much as possible, the worst-case condition. The % error on output of the following table is expressed in reference to V_{out}.

Table 6. Error on output

Error source	Calculus	Output voltage error	% error on output
Gain error	$20 * 20.10^{-3} * 5 * 1\%$	20 mV	1%
Vio error	$20 * 2.5\,mV$	50 mV	2.5%
CMRR error	$20 * \frac{48V - 12V}{\frac{100}{10^{20}}}$	7.2 mV	0.4%
Noise	$20 * \frac{55nV}{\sqrt{Hz}} \sqrt{30\,kHz * \left(\ln(30k) - \ln(0.1)\right) + 1\,MHz * \frac{\pi}{2} - 0.1\,Hz}$	1.5 mV_{RMS}	0.2% (1)
Total		77.2 mV +1.4 mV_{RMS}	4.1%

1. *The percentage is based on voltage peak value (3 times RMS value).*

So, the maximum output voltage in the worst case condition at ambient temperature is 2.077 V + 1.5 mV_{RMS} instead of the expected 2 V. This represents an error in the current reading of about 4.1%. 1% more must be added due to the shunt accuracy.

It is important to note that this calculus has been done by using all the maximum values and all the error terms have been added to each other, meaning that the chance to get 4.1% precision in the above use case is extremely low, even on the whole population the actual error is to a great extent smaller.

5.6 Root sum square approximation

A more realistic calculus is to use a statistical approach. Total error can be determined by using the root-sum-of-the-squares (RSS), a simplified statistical method to combine the error terms. With this approach, the average values considered are zero, and the maximum parameter values given in the datasheet have all the same Cpk (the maximum is given for all values with the same number of sigma) max. = K * sigma.

So, the error can be written as equation 11.

$$Error = \sqrt{\sum k.sigma^2} = \sqrt{\sum \left(\max datasheet\right)^2} \quad (11)$$

All these parameters must be summed up as described by equation 11.

$$Error_Rss = \sqrt{\left((\varepsilon G)^2 + (\varepsilon shunt)^2 + \left(\frac{Vio}{Rshunt.Isense}\right)^2 + \left(\frac{\frac{Vicm - 12V}{CMRR}}{Rshunt.Isense}\right)^2\right)} \quad (12)$$

We can expect a current of 5 A, an error of 2.9% @ 25 °C.

The error expected in this case is largely better (2.9%), than the worst-case calculation (5.1%), and above all more realistic.

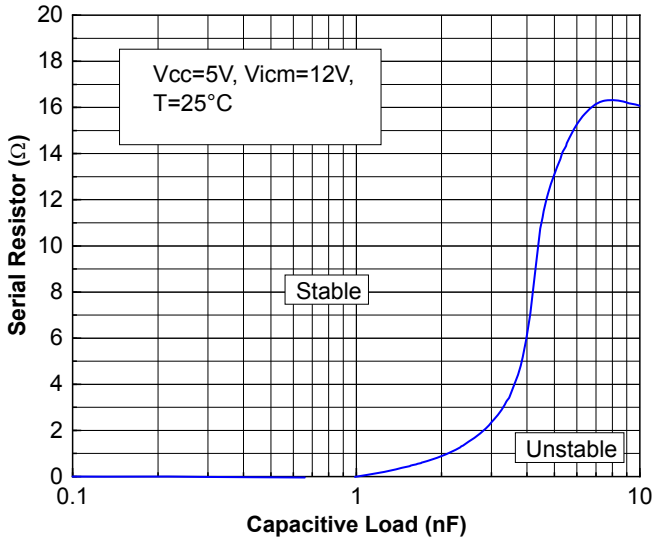
5.7 Stability

Driving large capacitive C_{load}

Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response.

Figure 37 shows the serial resistor that must be added to the output to make the system stable for a given capacitive load. The criteria chosen to ensure the stability of the system is an overshoot lower than 30% and with a settling time at 2.5% of the final value lower than 20 µs.

Figure 37. Stability criteria with a serial resistor at V_{CC} = 5 V



5.8 Power supply recommendation

To decouple the TSC20x correctly, it is recommended to place a 100 nF bypass capacitor between V_{cc} and Gnd. This capacitor must be placed as close as possible to the supply pins. Figure 38 describes the application setup for the startup phase. A V_{icm} = 12 V and a V_{sense} = 70 mV are set on the input pins of the current sensing. The current sensing output is directly connected to the comparator input pin.

Figure 39 shows a startup time for current sensing and integrated comparator, with a decoupling capacitance of 100 nF.

Figure 38. **Startup time schematic**

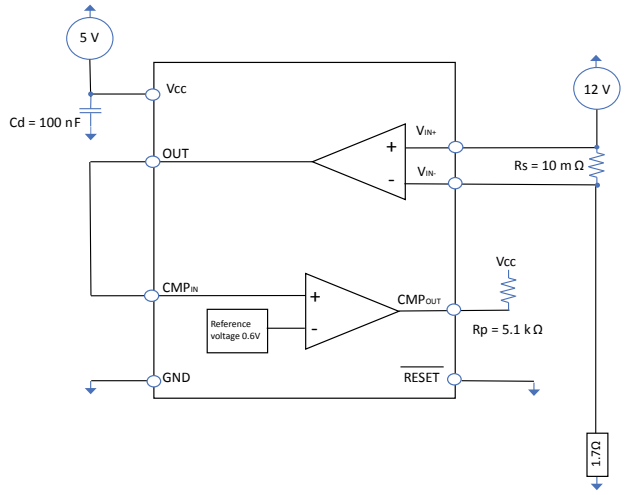
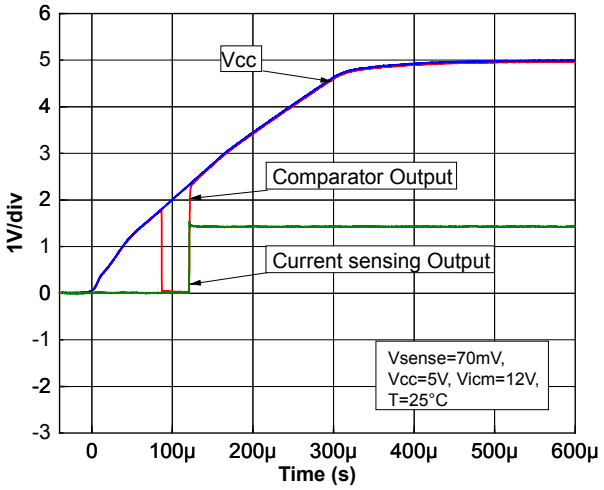


Figure 39. **Startup time with a decoupling capacitance of 100 nF**



5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the current sensing, load, and power supply. It is good practice to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

When using a shunt resistance lower than 1 Ω, it is important to use a 4-wire connection technique to sense the current as described in the schematic below. Effectively, this technique allows pairs of current-carrying and voltage-sensing electrodes to separate, and to take more accurate measurements by eliminating the lead and contact resistance from the measurements.

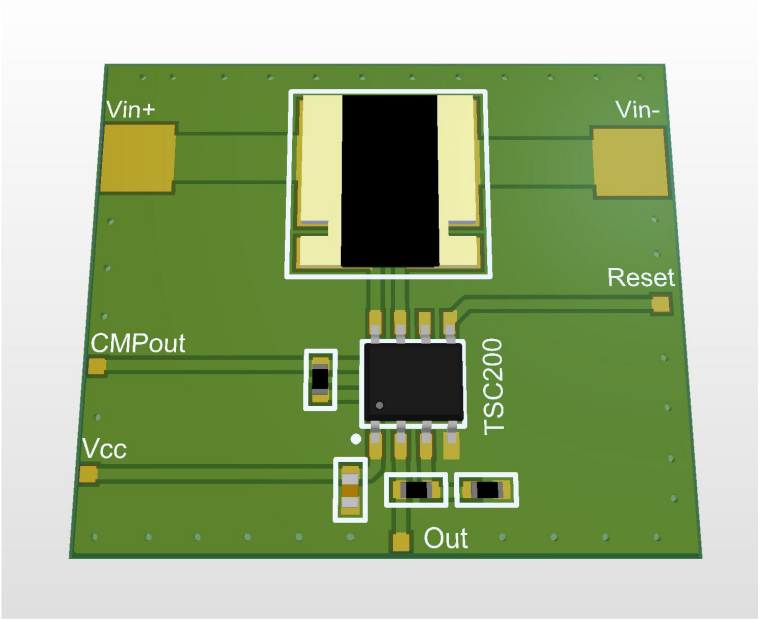
It is also important to treat the track connected to the input pin of the TSC20x as a differential pair. Thus, it must have the same length and width, and ideally be placed on the same PCB plane, and above all, it must be routed as far as possible from noisy sources. As this track carries the input bias current in a range of tens of µA, it can be designed small, but always taking into account resistivity. Any via in these input tracks are non-recommended to avoid any parasitic resistance in this path.

To minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

A ground plane generally helps to reduce EMI, which is why it is generally recommended to use a multilayer PCB, and use the ground planes as a shield to protect the internal track. In this case, pay attention to separate the digital from the analog ground and avoid any ground loop. To minimize EMI impact, it is important to reduce loop areas, which act as antennas.

Figure 40 suggests a possible routing for the TSC200, to minimize as much as possible a parasitic effect.

Figure 40. **Recommended layout**



5.10 EMI rejection ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of the current sensing device. An adverse effect that is common to many current sensing devices is a change in the offset voltage as a result of RF signal rectification.

A first order, an internal low pass filter, is included on the input of the TSC20x to minimize susceptibility to EMIRR. Figure 41 shows the EMIRR on pin IN+, Figure 42 shows the EMIRR on pin IN- of the TSC200 measured from 10 MHz up to 2.4 GHz.

Figure 41. **EMIRR on pin+**

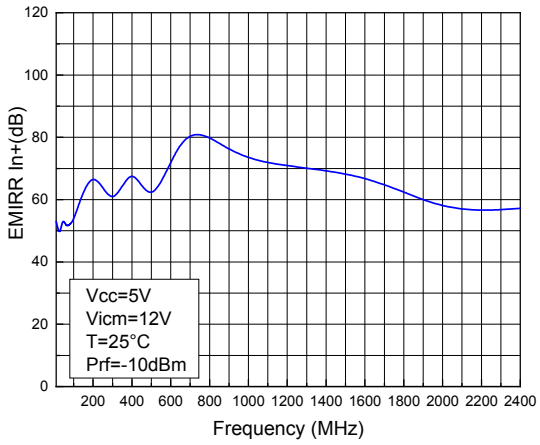
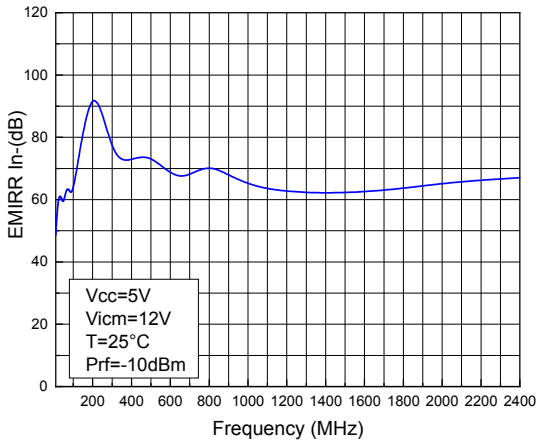


Figure 42. **EMIRR on pin-**



5.11 Overload recovery

Overload recovery is defined as the time required for the current sensing output to recover from a saturated state to a linear state.

The saturated state occurs when the output voltage gets very close to either rail in the application. It normally results from an excessive input voltage.

When the output of the TSC200 enters into a saturated state it needs less than 3 µs to get back to a linear state as shown by Figure 43 and Figure 44.

Figure 43. Negative overvoltage recovery V_{CC} = 5 V

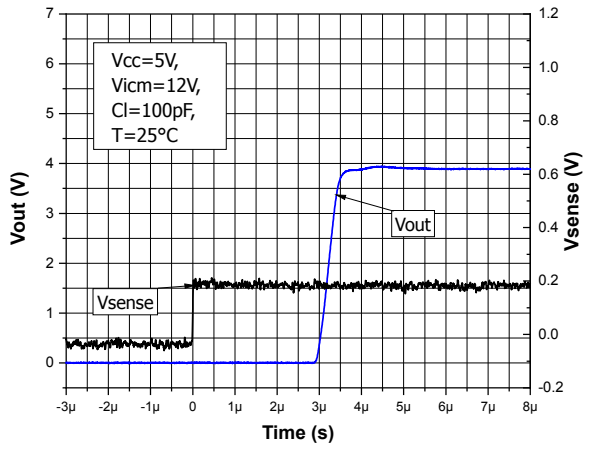
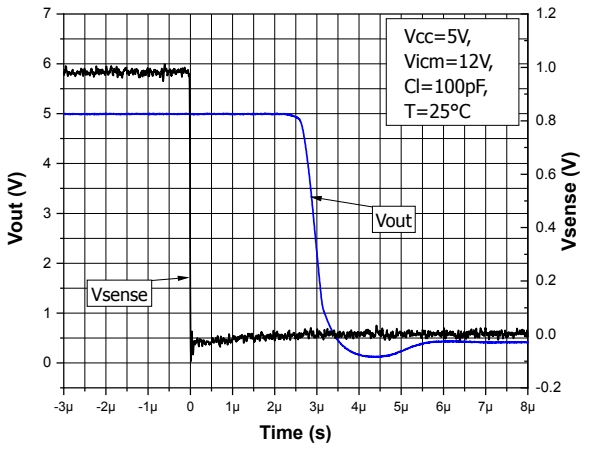


Figure 44. Positive overvoltage recovery V_{CC} = 5 V

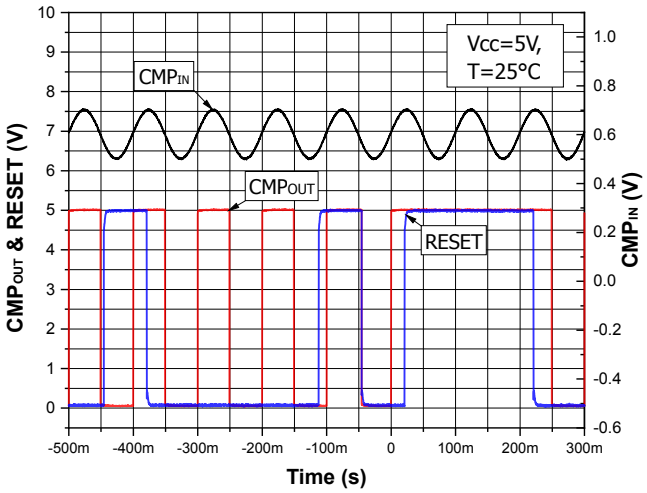


5.12 Comparator

The TSC20x family integrates an open-drain comparator, which can be useful for an overcurrent protection function. It is generally recommended to use a 5.1 kΩ pull up resistance on the output. The voltage applied on the pull up resistance must be in the 1.8 to 18 V range, regardless of the V_{CC}. This comparator offers a 300 ns (typical) response time for a small overdrive of 5 mV and lower than 100 ns for an overdrive higher than 50 mV.

The comparator can latch the information and reset it thanks to the RESET pin. Nevertheless, if the RESET pin is left open or connected to the ground, the output latch feature is not functional anymore, and the output acts as a classic comparator. If the RESET pin is connected to a voltage higher than 1.1 V, once CMP_{IN} rises above 608 mV, CMP_{OUT} latches and remains in this state even if CMP_{IN} drops below 608 mV. Pulsing the RESET pin to ground for at least 0.1 µs resets the latch. See Figure 45.

Figure 45. Comparator latching capability



5.13 Overcurrent response time

The TSC20x is composed of a current sensing and a comparator, which are two essential IPs to detect the occurrence of an overcurrent, and alerting its presence. Thanks to a typical slew rate of 7 V/µs for the current sensing and 300 ns as propagation delay for the comparator, the TSC200 is a perfect device for fast overcurrent protection application.

The overcurrent protection circuit, shown in Figure 46, uses the TSC200 to control an external P-channel MOSFET which opens the current path under overload conditions. The latched output of the TSC200's comparator prevents the circuit from oscillating, and the push-button resets the current path after an overcurrent condition.

In the typical application described in Figure 46, a current in the range of 2 A to 20 A is monitored through a shunt of 10 mΩ. The TSC200 is powered with a V_{CC} = 5 V.

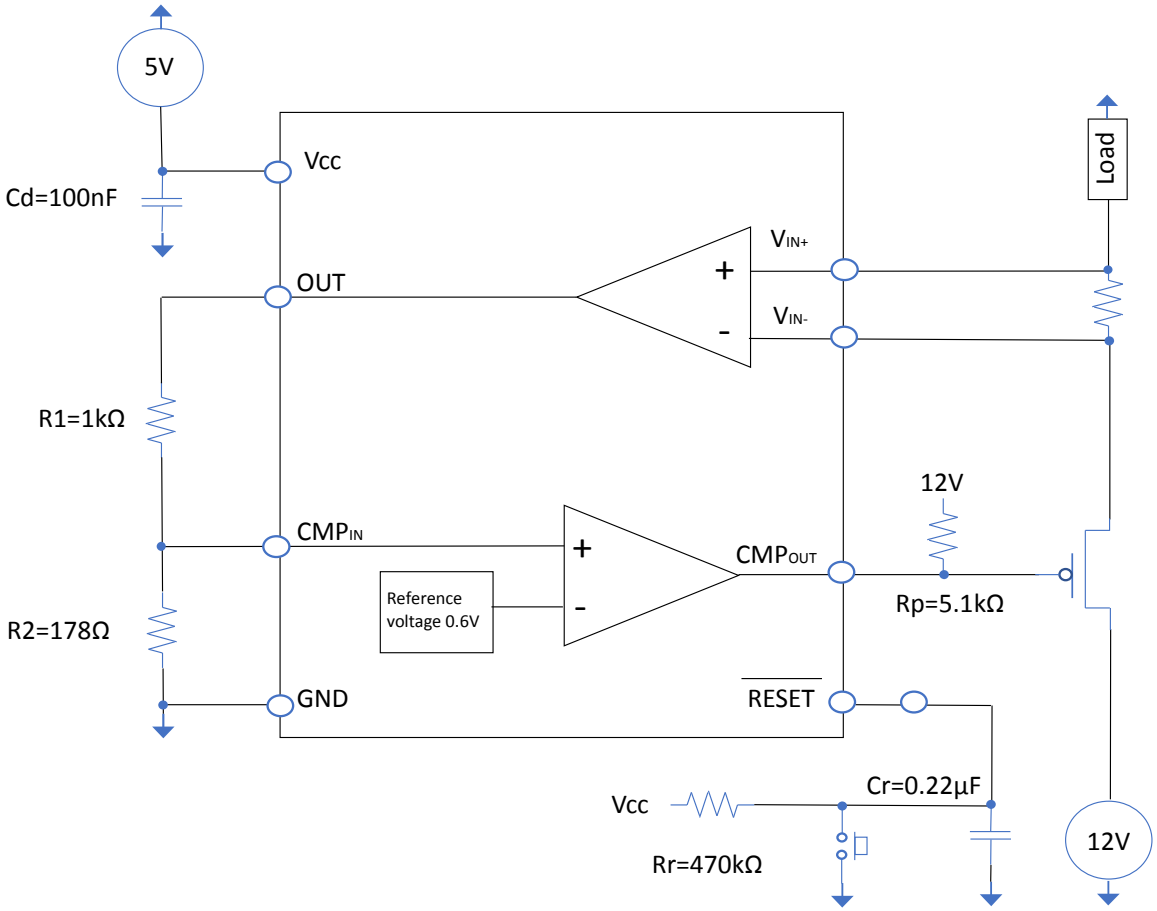
The full-scale output voltage should theoretically be in the range of 400 mV to 4 V.

The output voltage range 4 V to 5 V is reserved for OCP detection. So, the divider bridge on the comparator input is selected as follows:

R1 = 178 Ω

R2 = 1 kΩ

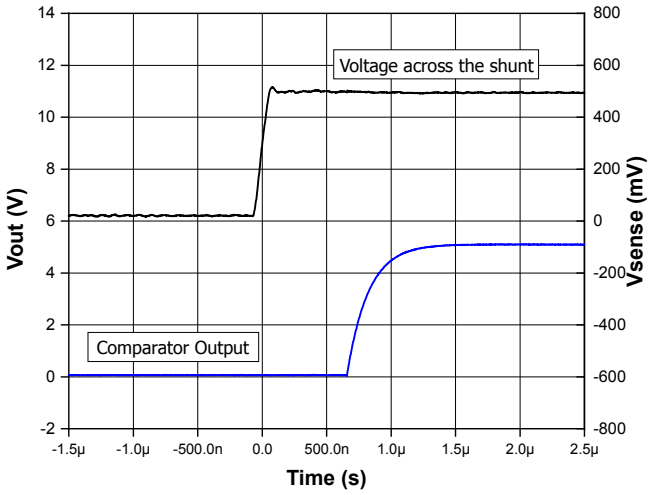
Figure 46. Typical OCP application



In the most critical case where low current (2 A) is flowing into the load, the output of the TSC200 is close to 400 mV, so the current sensing output would need 0.7 µs to pass from 400 mV to 5 V after the overcurrent event.

The comparator, due to its good propagation delay, requires only 300 ns to change its state from low to high level. So, after an overcurrent, the system takes, in a worst condition scenario (small current into the load), less than 1 µs to switch-off the PMOS, as described by Figure 47.

Figure 47. **TSC200 response time to an overcurrent event**



5.14 Comparator power-on reset

The TSC20x's comparator integrates a power-on reset, allowing it to have a defined output state.

The TSC20x comparator has an open drain output, so while the V_{CC} power supply is lower than 1.5 V, the output is ever equal to V_{CC}. When V_{CC} is above 1.5 V (typ.), the output is in a low state if the $COMP_{IN}$ voltage is lower than 0.6 V, as described by Figure 48, or a high state if the $COMP_{IN}$ voltage is higher than 0.6 V as described by Figure 49.

Figure 48. **CMP_{OUT} at startup when CMP_{IN} < 0.6 V**

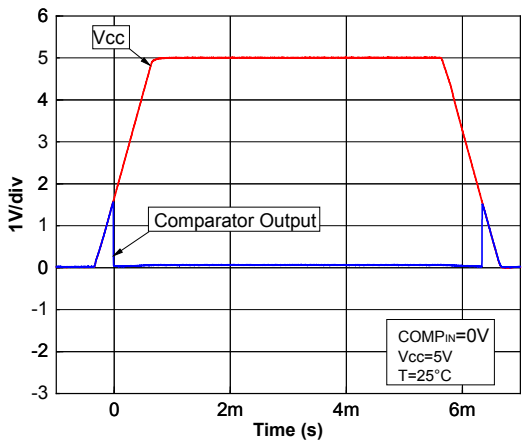
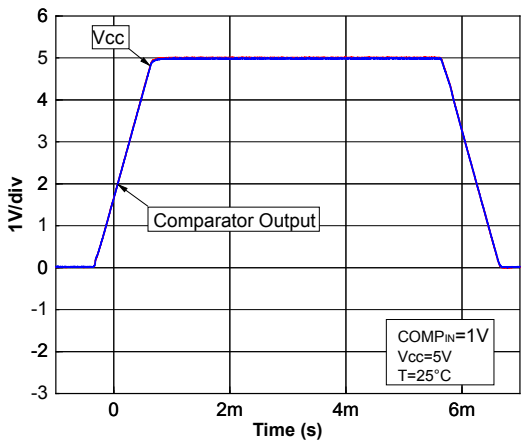


Figure 49. **CMP_{OUT} at startup when CMP_{IN} > 0.6 V**



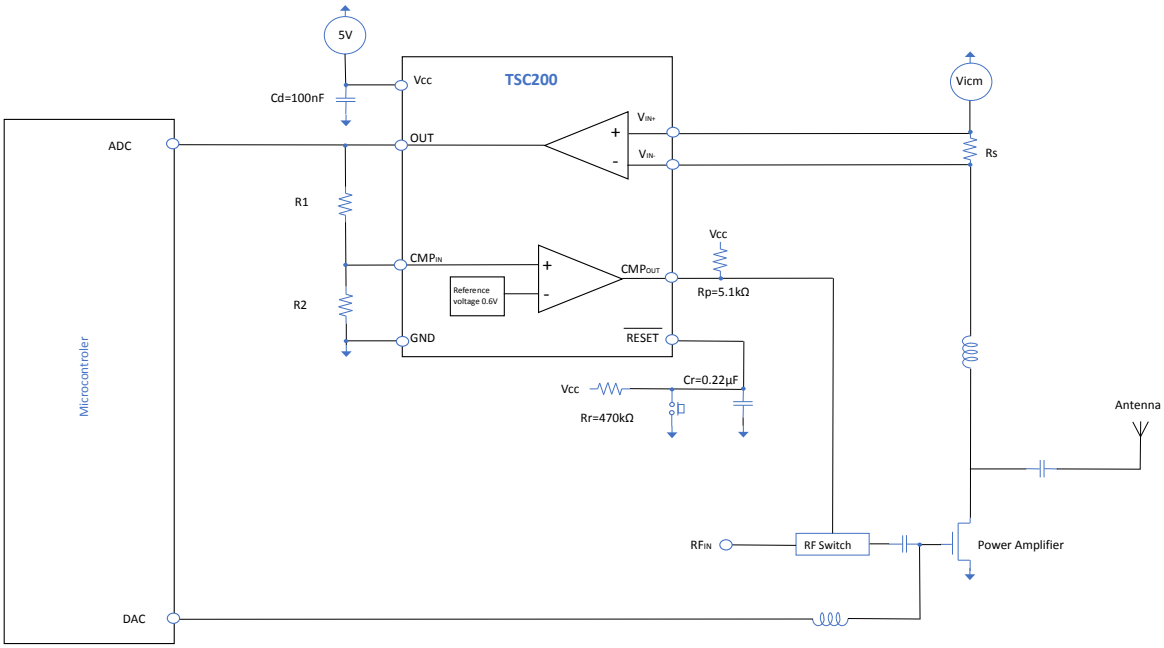
5.15 Application example

Control of power amplifier in wireless infrastructure

Current sensing is important in a power amplifier application from at least three main standpoints. Firstly, from a technical aspect, monitoring the performance of a power amplifier helps maximizing the output power allowing to achieve a good linearity and efficiency. Secondly, by reducing the overall energy consumption of base stations, the impact on the environment is limited as much as possible. Finally, by considering that roughly half of the total energy of a wireless infrastructure is consumed by the power amplifier, optimizing its efficiency also allows for a financial benefit.

The integrated comparator in the TSC200 device can be used as a protection. Effectively combined with an RF switch as shown in Figure 50, when a higher current appears in the power amplifier, due to a current spike, the comparator can toggle a control pin of the RF switch and cut the signal to the gate of the power amplifier to prevent any damage. This analog path is much faster than digital processing and offers better protection.

Figure 50. TSC200 used to drive and protect a power amplifier



6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SO8 package information

Figure 51. SO8 package outline

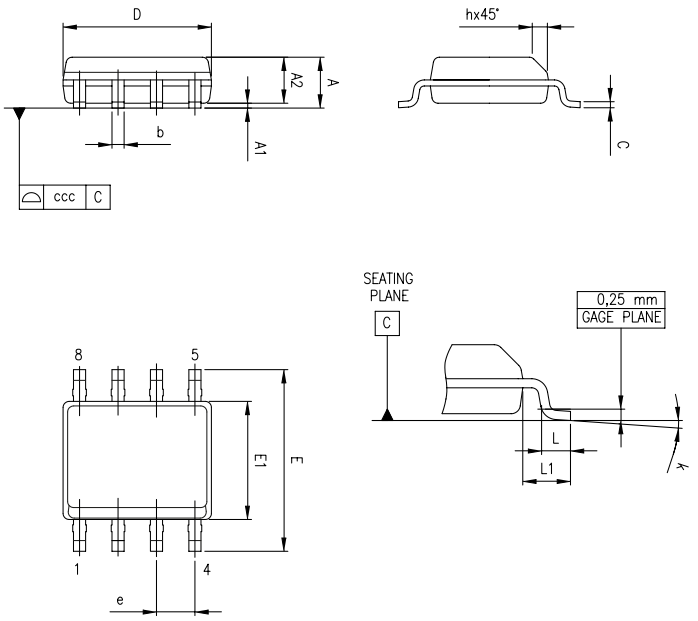


Table 7. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.04		0.010
A2	1.25			0.049		
b	0.28	0.40	0.48	0.011	0.016	0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40	0.635	1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

6.2 MiniSO8 package information

Figure 52. **MiniSO8 package outline**

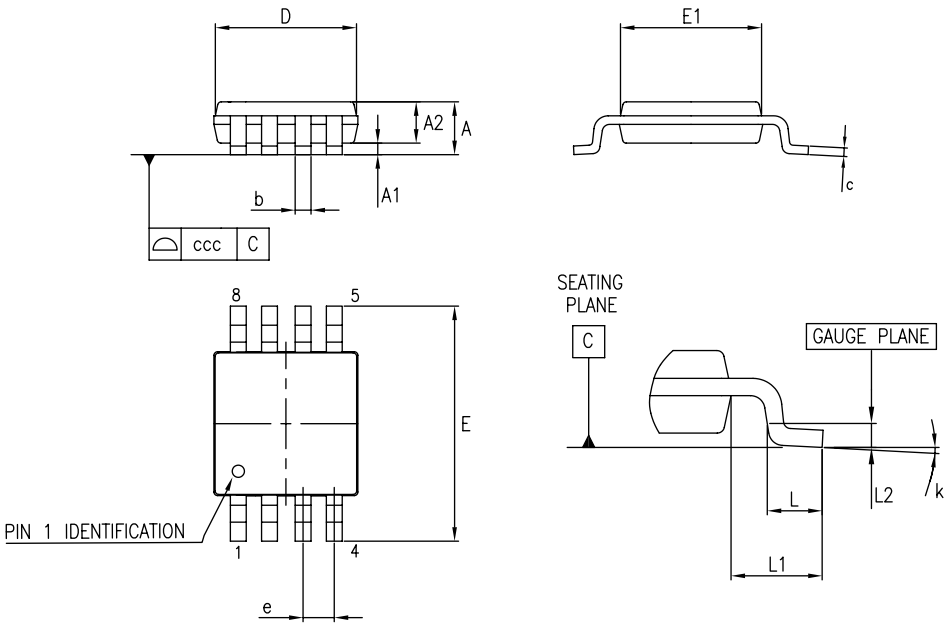


Table 8. **MiniSO8 mechanical data**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

7 Ordering information

Table 9. Order codes

Order code	Gain (V/V)	Package	Packaging	Marking
TSC200IDT	20	SO8	Tape and reel	TSC200I
TSC200IYDT(1)				TSC200IY
TSC200IST		MiniSO8		O123
TSC200IYST(1)				O126
TSC201IDT	50	SO8		TSC201I
TSC201IYDT (1)				TSC201IY
TSC201IST		MiniSO8		0124
TSC201IYST(1)				0127
TSC202IDT	100	SO8		TSC202I
TSC202IYDT (1)				TSC202IY
TSC202IST		MiniSO8		0125
TSC202IYST(1)				0128

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 10. **Document revision history**

Date	Version	Changes
24-Jan-2022	1	First release.
10-Nov-2023	2	Added new TSC201, TSC202 part numbers, Figure 18, Figure 19, Figure 20, Figure 21 and new Section 5.15 Application example. Updated features and description on the cover page, Figure 1, Figure 2, Table 4, Figure 15, Figure 16, Figure 17 and Table 9. Order codes. Minor text changes.
30-Sep-2025	3	Updated Section 5.12: Comparator.

Contents

1 **Block diagram and pin description** 2
2 **Absolute maximum ratings and operating conditions** 3
3 **Electrical characteristics** 4
4 **Typical performance characteristics** 7
5 **Application information** 12
5.1 Overview 12
5.2 Theory of operation 12
5.3 Rsense selection 16
5.4 Input offset voltage drift vs. temperature 16
5.5 Error calculation 16
5.6 Root sum square approximation 18
5.7 Stability 19
5.8 Power supply recommendation 19
5.9 PCB layout recommendations 20
5.10 EMI rejection ratio (EMIRR) 21
5.11 Overload recovery 21
5.12 Comparator 22
5.13 Overcurrent response time 23
5.14 Comparator power-on reset 24
5.15 Application example 25
6 **Package information** 26
6.1 SO8 package information 26
6.2 MiniSO8 package information 27
7 **Ordering information** 28
Revision history 29

List of tables

Table 1. Pin description . . . 2
Table 2. Absolute maximum ratings . . . 3
Table 3. Operating conditions . . . 3
Table 4. Electrical characteristics of the Current sense amplifier at V_{CC} = 12 V, V_{ICM} = 12 V, V_{Sense} = 100 mV, R_L = 10 kΩ to GND, $R_{pull-up}$ = 5.1 kΩ connected from CMP_{OUT} to V_{CC}, CMP_{IN} = GND, T = 25 °C (unless otherwise specified) . . . 4
Table 5. Electrical characteristics of the Comparator at V_{CC} = 12 V, V_{ICM} = 12 V, V_{Sense} = 100 mV, R_L = 10 kΩ to GND, $R_{pull-up}$ = 5.1 kΩ connected from CMP_{OUT} to V_{CC}, T = 25 °C (unless otherwise specified) . . . 6
Table 6. Error on output . . . 18
Table 7. SO8 package mechanical data . . . 26
Table 8. MiniSO8 mechanical data . . . 27
Table 9. Order codes . . . 28
Table 10. Document revision history . . . 29

List of figures

Figure 1. Block diagram . . . 2
Figure 2. Pin connections (top view) . . . 2
Figure 3. Typical comparator hysteresis. . . . 6
Figure 4. Gain vs. frequency (C_L = 1000 pF) . . . 7
Figure 5. Gain vs. frequency (C_L = 100 pF) . . . 7
Figure 6. Gain plot . . . 7
Figure 7. CMRR and PSRR vs. frequency . . . 7
Figure 8. Output error vs. V_{sense} . . . 8
Figure 9. Output error vs. common-mode voltage . . . 8
Figure 10. Output current vs. output voltage at V_{CC} = 2.7 V . . . 8
Figure 11. Output current vs. output voltage at V_{CC} = 12 V . . . 8
Figure 12. Quiescent current vs. output voltage . . . 8
Figure 13. Quiescent current vs. common-mode voltage . . . 8
Figure 14. Output short-circuit current vs. supply voltage . . . 9
Figure 15. Step response for 20 to 30 mV V_{sense} G = 20 . . . 9
Figure 16. Step response for 20 to 110 mV V_{sense} G = 20 . . . 9
Figure 17. Step response for 90 to 100 mV V_{sense} G = 20 . . . 9
Figure 18. Step response for 20 to 30 mV V_{sense} G = 50 . . . 9
Figure 19. Step response for 20 to 110 mV V_{sense} G = 50 . . . 9
Figure 20. Step response for 90 to 100 mV V_{sense} G = 50 . . . 10
Figure 21. Step response for 20 to 110 mV V_{sense} G = 100 . . . 10
Figure 22. Comparator V_{OL} vs. I_{SINK} . . . 10
Figure 23. Comparator trip points vs. V_{CC} . . . 10
Figure 24. Comparator trip points vs. temperature . . . 11
Figure 25. Comparator reset voltage vs. V_{CC} . . . 11
Figure 26. Comparator propagation delay vs. overdrive voltage . . . 11
Figure 27. Comparator propagation delay vs. temperature . . . 11
Figure 28. Comparator propagation delay . . . 11
Figure 29. Simplified diagram when V_{icm} > 40% V_{CC} . . . 12
Figure 30. Input bias current vs. V_{sense} for a V_{icm} = 80 V . . . 13
Figure 31. Simplified diagram when V_{icm} < 40% V_{CC} . . . 14
Figure 32. Input bias current vs. V_{sense} for a V_{icm} = -16 V . . . 14
Figure 33. V_{OUT} when V_{sense} = 0 V, V_{CC} = 5 V, V_{icm} = 0 V . . . 15
Figure 34. V_{OUT} when V_{sense} = 0 V, V_{CC} = 5 V, V_{icm} = 12 V . . . 15
Figure 35. Input voltage offset over V_{icm} and temperature . . . 15
Figure 36. Input referred noise vs. frequency . . . 17
Figure 37. Stability criteria with a serial resistor at V_{CC} = 5 V . . . 19
Figure 38. Startup time schematic . . . 20
Figure 39. Startup time with a decoupling capacitance of 100 nF . . . 20
Figure 40. Recommended layout . . . 21
Figure 41. EMIRR on pin+ . . . 21
Figure 42. EMIRR on pin- . . . 21
Figure 43. Negative overvoltage recovery V_{CC} = 5 V. . . . 22
Figure 44. Positive overvoltage recovery V_{CC} = 5 V . . . 22
Figure 45. Comparator latching capability . . . 22
Figure 46. Typical OCP application . . . 23
Figure 47. TSC200 response time to an overcurrent event . . . 24
Figure 48. CMP_{OUT} at startup when CMP_{IN} < 0.6 V . . . 24
Figure 49. CMP_{OUT} at startup when CMP_{IN} > 0.6 V . . . 24
Figure 50. TSC200 used to drive and protect a power amplifier . . . 25

Figure 51. SO8 package outline 26
Figure 52. MiniSO8 package outline 27

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