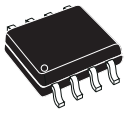
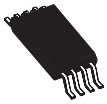
TSC240

Datasheet

High-side and low-side bidirectional zero-drift current sense amplifier with enhanced PWM rejection



SO8



TSSOP8

Maturity status link
TSC240

Features

- Enhanced PWM rejection
- Excellent CMRR: 132 dB DC CMRR
- Wide common-mode range: –4 V to 100 V
- Accuracy:
  - Gain:
    - Gain error: 0.20% (maximum)
    - Gain drift: 2.5 ppm/°C (maximum)
  - Offset:
    - Offset voltage: ±20 µV (maximum)
    - Offset drift: 150 nV/°C (maximum)
- Available gains: 20 V/V
- Quiescent current: 2.4 mA (maximum)
- SO8 and TSSOP8 packages
- AEC-Q100 qualified

Applications

- Motor controls
- Solenoid and valve controls
- Power management
- Industrial process control
- Telecom equipment
- Automotive

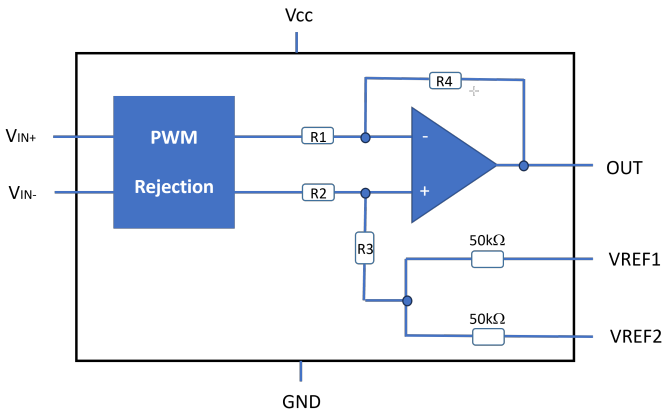
Description

The TSC240 is a high-precision current sense amplifier with enhanced PWM rejection. It can sense current via a shunt resistor over a wide range of common-mode voltages, from -4 to +100 V, regardless of the supply voltage. It is available with a preset gain of 20 V/V. Thanks to its high precision, it can sense very low drop voltages, minimizing measurement error.

The TSC240 is a current sense amplifier that can be used in various functions such as precision current measurement, overcurrent protection, current monitoring, and feedback loops. These devices fully operate over the broad supply voltage range of 2.7 to 5.5 V and over the industrial temperature range of -40 to +125 °C.

1 Block diagram and pin description

Figure 1. **Block diagram**



1.1 Pin description

Figure 2. **Pin connections (top view)**

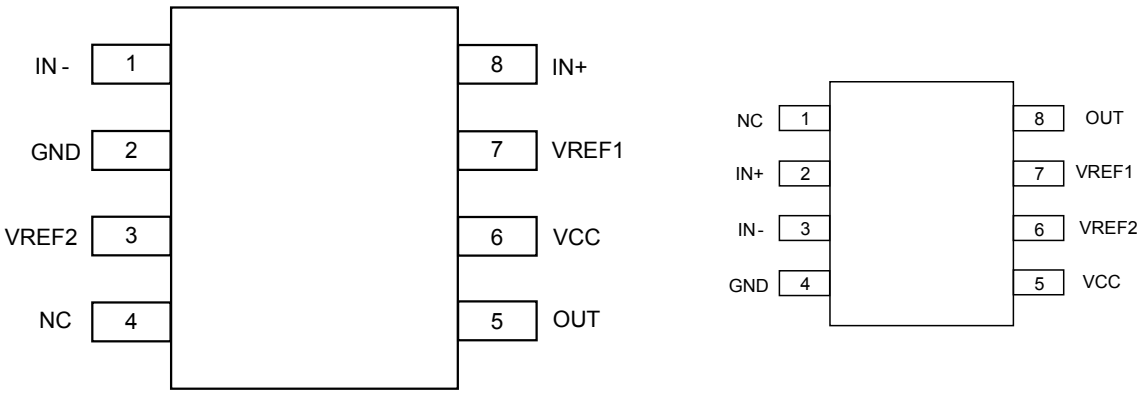


Table 1. **Pin description**

Pin name	Pin (TSSOP8)	Pin (SO8)	Description
IN-	3	1	Current sense amplifier, negative input
GND	4	2	Ground
REF2	6	3	Reference voltage 2
NC	1	4	Not connected
OUT	8	5	Current sense amplifier, output
VCC	5	6	Supply voltage
REF1	7	7	Reference voltage 1
IN+	2	8	Current sense amplifier, positive input

2 Maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN+}, V_{IN-}	Differential voltage (V_{IN+}) – (V_{IN-})	-100 to +100	
	Common-mode voltage on input pins	-10 to +110	
REF1, REF2	Voltage on pins REF1, REF2	GND -0.3 to V_{CC}+0.3	
OUT	Analog output	GND -0.3 to V_{CC} +0.3	
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature	-65 to +150	°C
ESD	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM) SO8 TSSOP8	 1000 750	
RTH_{JA}	Thermal resistance junction to ambient SO8 TSSOP8	 125 120	°C/W

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 5.5	V
V_{ICM}	Common-mode voltage on input pins	-4 to +100	V
REF	Reference input range	0 to V_{CC}	V
T	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

V_{CC} = 5 V, V_{ICM} = 12 V, V_{SENSE} = V_{IN+} - V_{IN-}, V_{REF1} = V_{REF2} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Table 4. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
I_{CC}	Current consumption	V_{ICM} = -4 to +100 V, V_{SENSE} = 0 mV, T_{min} < T < T_{max}		1.9	2.4 2.6	mA
INPUT						
$\|V_{os}\|$	Offset voltage, RTI	V_{ICM} = 12 V, V_{SENSE} = 0 mV		3	20	µV
		V_{ICM} = 48 V, V_{SENSE} = 0 mV		12	56	
$\|\Delta V_{os}/\Delta T\|$	Offset drift (RTI) vs. temperature (1)	V_{SENSE} = 0 mV, V_{ICM} = 12 and 48 V T_{min} < T < T_{max}		30	150	nV/°C
CMR	Common-mode rejection	V_{IN+} = -4 to +100 V, V_{SENSE} = 0 mV T_{min} < T < T_{max}	120 120	132		dB
		f = 50 kHz		75		
I_{IB}	Input bias current	V_{ICM} = 12 V, I_{IB+}, I_{IB-}, V_{SENSE} = 0 mV T_{min} < T < T_{max}		110	150 150	µA
		V_{ICM} = 48 V, I_{IB+}, I_{IB-}, V_{SENSE} = 0 mV T_{min} < T < T_{max}		210	250 250	
SVR	Supply voltage rejection	V_{CC} = 2.7 to 5.5 V, V_{SENSE} = 0 mV T_{min} < T < T_{max}	100	120		dB
$\|V_{SENSE}\|$	V_{sense} operating voltage with E_G ≤ 0.2% (2)	TSC240A1, T_{min} < T < T_{max}			239	mV
OUTPUT						
G	Gain	TSC240A1		20		V/V
E_G	Gain error	V_{ICM} = 12 and 48 V GND + 100 mV ≤ V_{OUT} ≤ V_{CC} - 100 mV T_{min} < T < T_{max}		±0.05	±0.20 ±0.20	%
$\Delta E_G/\Delta T$	Gain error vs. temperature	T_{min} < T < T_{max}		±0.5	±2.5	ppm/°C
NLE	Non-linearity error	GND + 10 mV ≤ V_{OUT} ≤ V_{CC} - 200 mV		±0.001		%
V_{CC} - V_{OH}	Output swing to the positive rail	RL = 10 kΩ to GND, T_{min} < T < T_{max}		30	200	mV
V_{OL}	Output swing to GND	RL = 10 kΩ to GND, V_{SENSE} = 0 mV, V_{REF1} = V_{REF2} = 0 V, T_{min} < T < T_{max}		4	10	
I_{OUT}	Output current	Sink mode, V_{ICM} = 12 and 48 V T_{min} < T < T_{max}	10 8	20	30 40	mA
		Source mode, V_{ICM} = 12 and 48 V T_{min} < T < T_{max}	20 10	26	40 50	
Reg load	Load regulation	I_{OUT} = -5 to +5 mA		0.4	1.5	mV/mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_L	Maximum capacitive load	No sustained oscillation		2.2		nF
OFFSET ADJUSTEMENT						
RT	Reference voltage rejection ratio, RTI (3)	TSC240A1		20		µV/V
Acc	Reference divider accuracy	V_{REF1} = V_{CC}, V_{REF2} = GND, V_{SENSE} = 0 mV T_{min} < T < T_{max}		0.02	0.1	%
Dynamic performances						
BW	C_L = 5 pF	-3dB bandwidth T_{min} < T < T_{max}	300 300	560		kHz
		0.5% THD-N		100		
SR	Slew rate	V_{ICM} = 12 and 48 V T_{min} < T < T_{max}	1.4 1.2	2		V/µs
T_S	Settling time	Up to 0.5% of final value		5		µs
	PWM rejection, settling time	V_{ICM} = [0, 48 V], rise/fall time = 20 ns Up to 0.5% of final value		2.5		µs
Noise, RTI						
En	Voltage noise density			50		nV/√Hz

1. *Guaranteed by design and characterization on a sample of parts, not tested in production.*
2. *V_{SENSE} = (V_{IN+}) – (V_{IN-}).*
3. *RTI stands for “Related to input”.*

4 Typical characteristics

TSC240A1 is used for typical characteristics, T_A = 25 °C, V_S = 5 V, V_{ICM} = 12 V and V_{REF} = V_{CC}/2 (unless otherwise specified).

Figure 3. Input offset production distribution

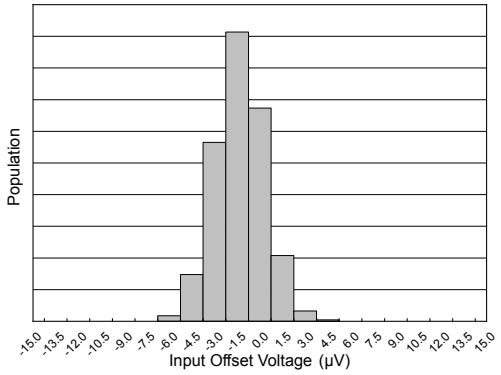


Figure 4. Gain error production distribution

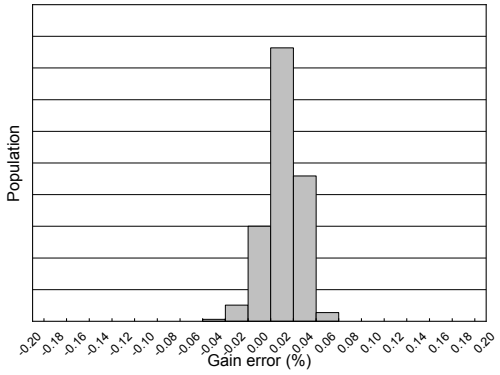


Figure 5. Common-mode rejection ratio production distribution

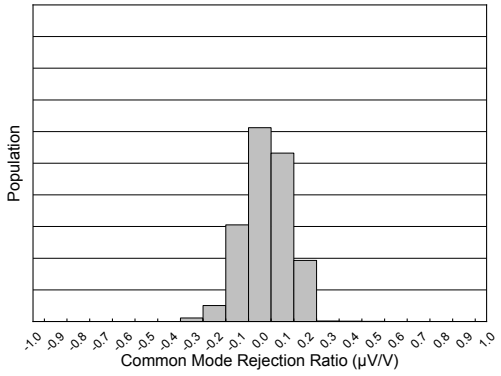


Figure 6. Supply current vs. supply voltage

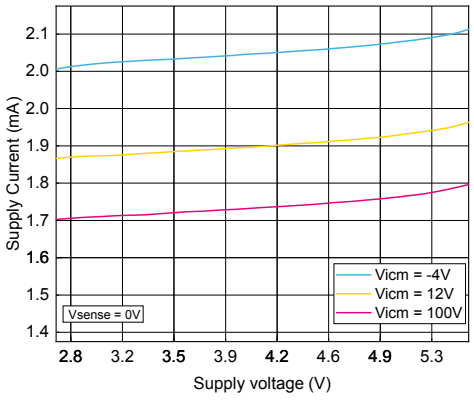


Figure 7. Supply current vs. input common-mode

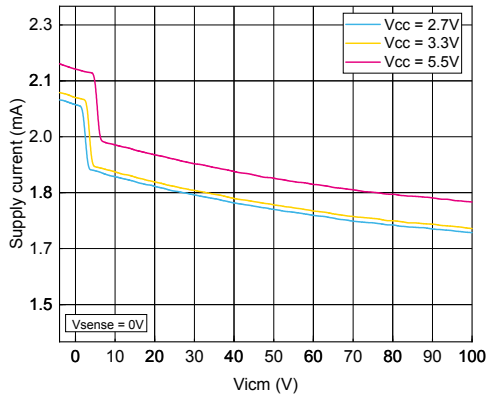


Figure 8. Supply current vs. temperature

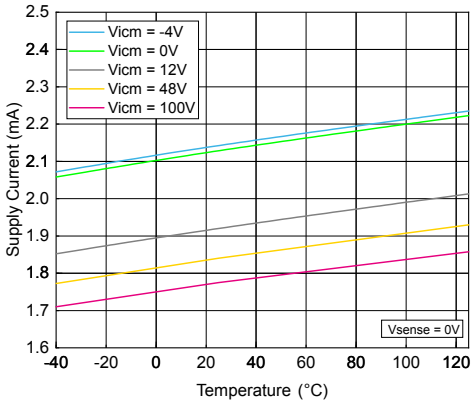


Figure 9. Input bias current vs. common-mode

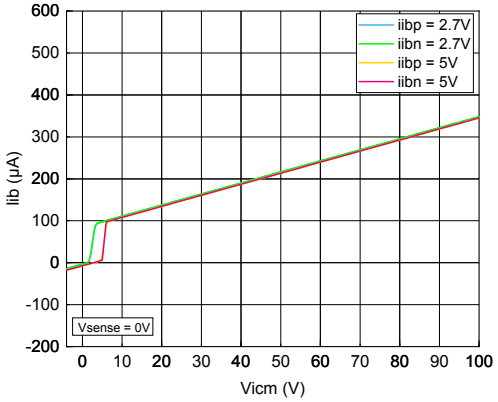


Figure 10. Input bias current vs. temperature

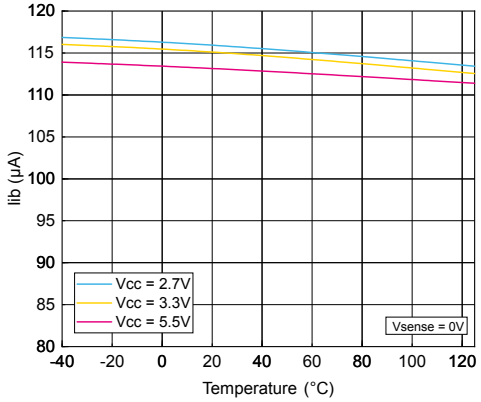


Figure 11. Input bias current vs. input common-mode voltage V_{CC} = 0 V

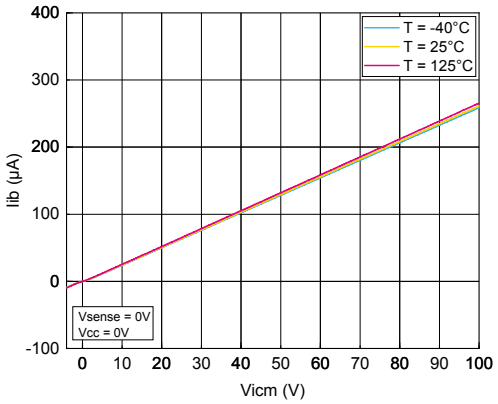


Figure 12. Input bias current vs. V_{SENSE}

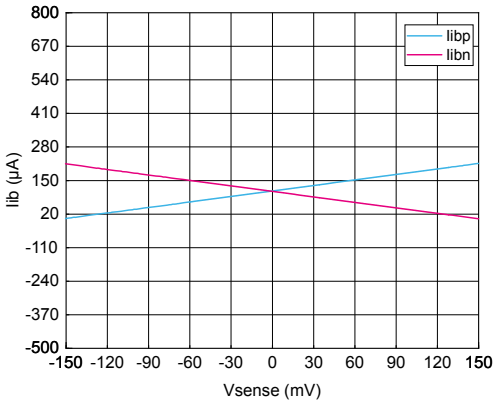


Figure 13. Input offset voltage vs. temperature

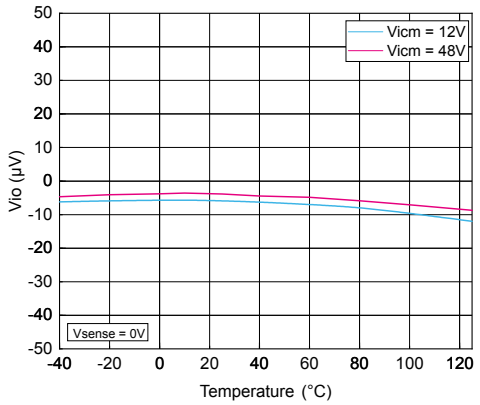


Figure 14. Input offset voltage vs. input common-mode with V_{CC} = 5 V

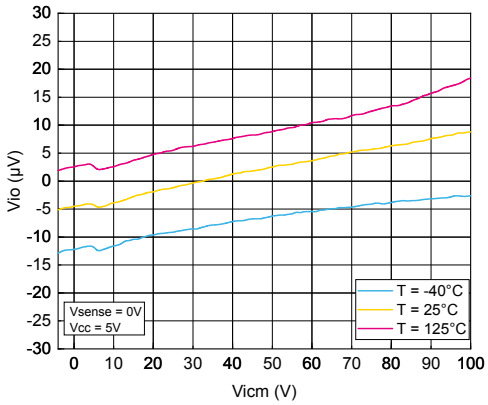


Figure 15. Input offset voltage vs. input common-mode with V_{CC} = 2.7 V

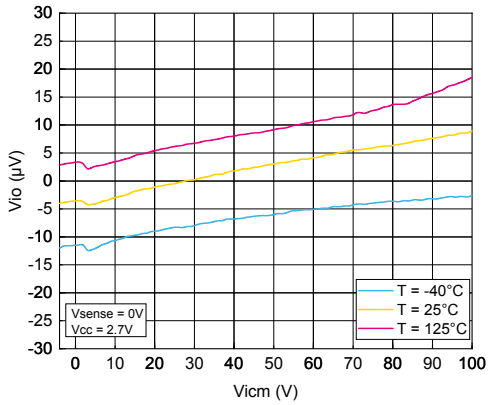


Figure 16. Input offset voltage vs. supply voltage

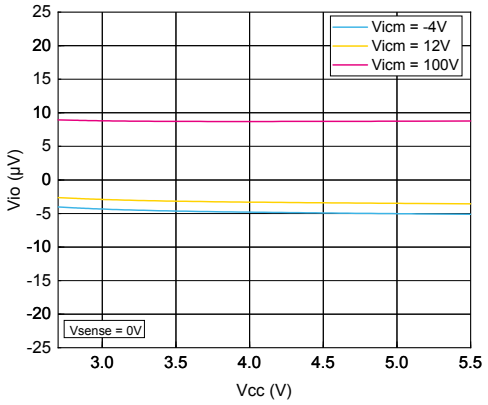


Figure 17. Output current vs. output voltage

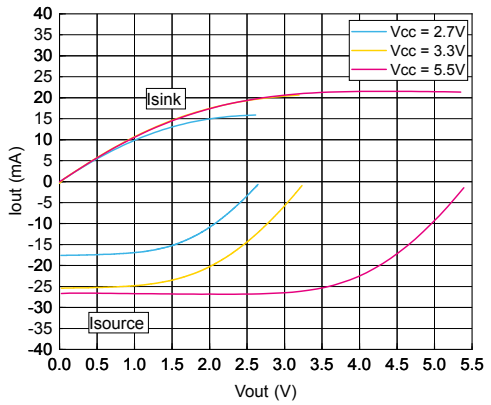


Figure 18. Output current vs. temperature with V_{CC} = 5 V

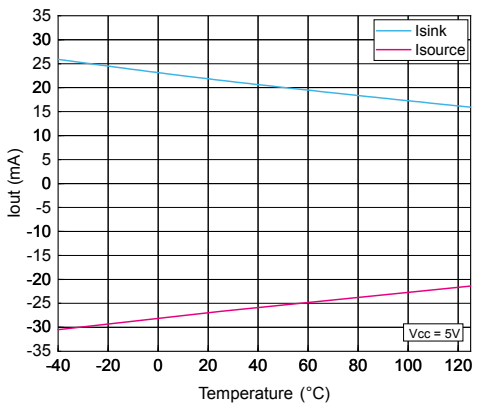


Figure 19. Output current vs. temperature with V_{CC} = 2.7 V

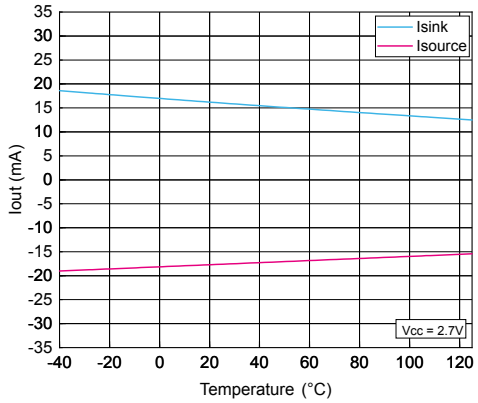


Figure 20. V_{OH} vs. temperature

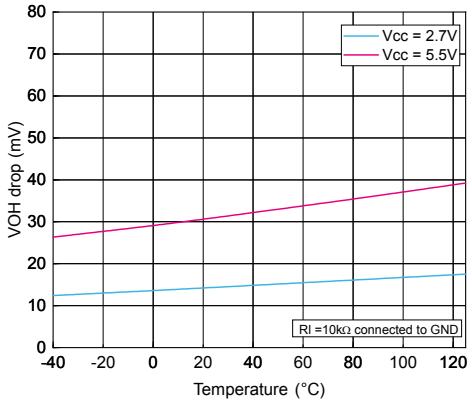


Figure 21. V_{OL} vs. temperature

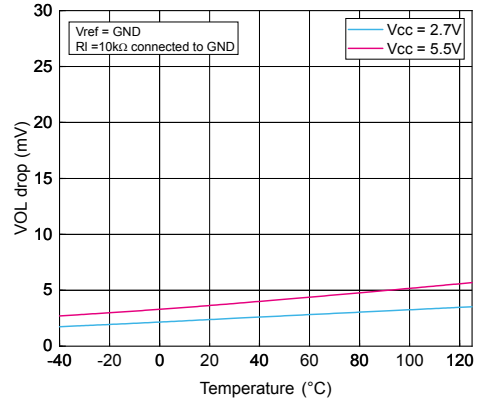


Figure 22. Linearity vs. V_{SENSE}

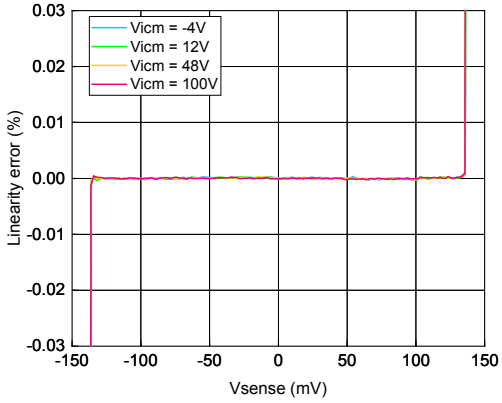


Figure 23. Linearity vs. V_{SENSE} and temperature

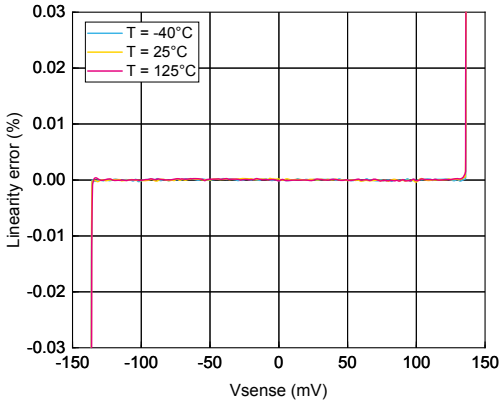


Figure 24. Gain error vs. input common-mode

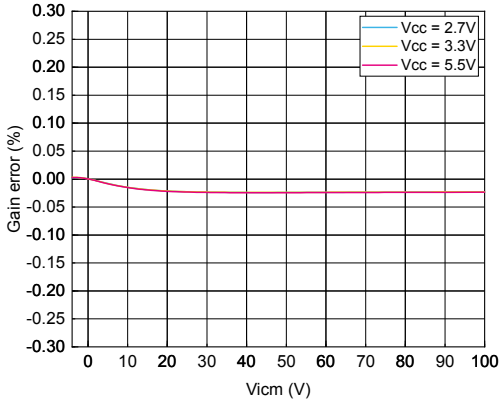


Figure 25. Gain error vs. V_{ICM} and temperature

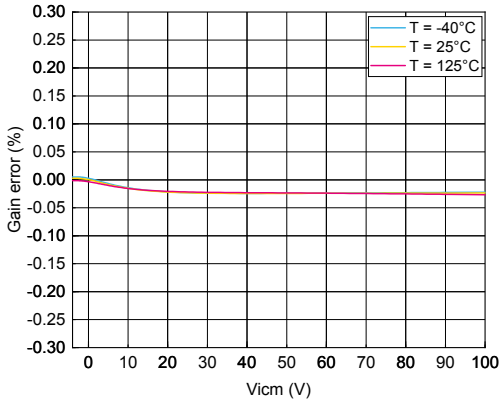


Figure 26. Load regulation

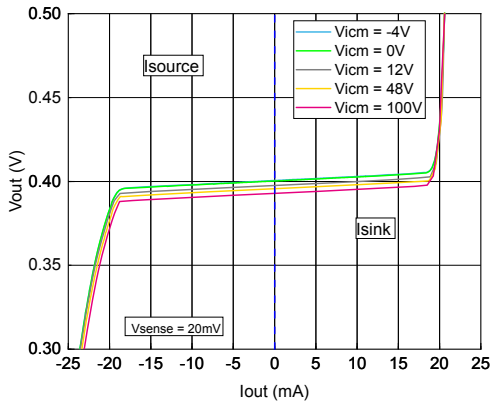


Figure 27. Gain vs. frequency

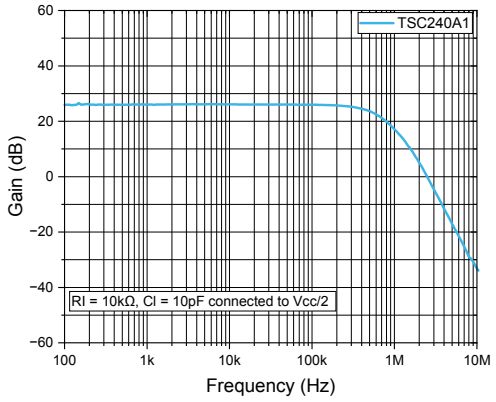


Figure 28. Gain vs. frequency with different capacitive load

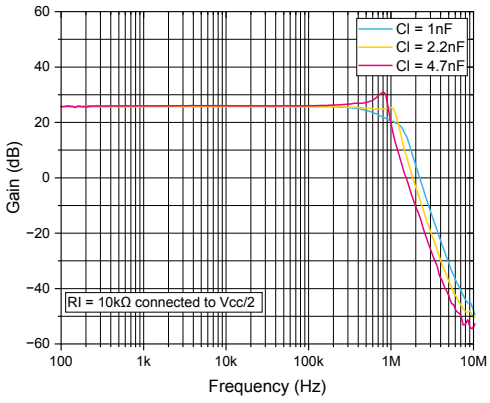


Figure 29. Bandwidth vs. input common-mode

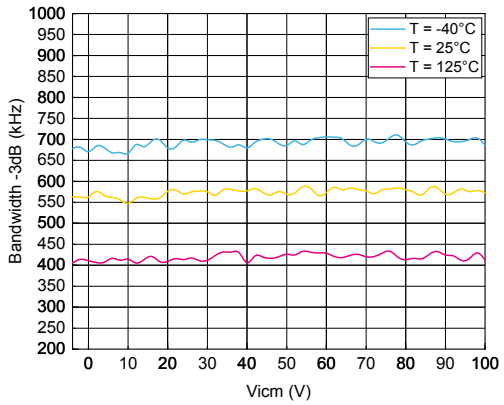


Figure 30. Overshoot vs. capacitive load

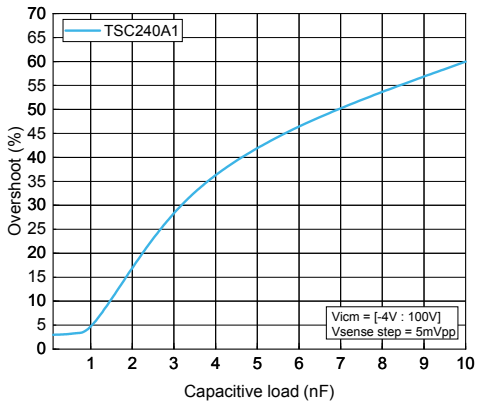


Figure 31. Small signal response

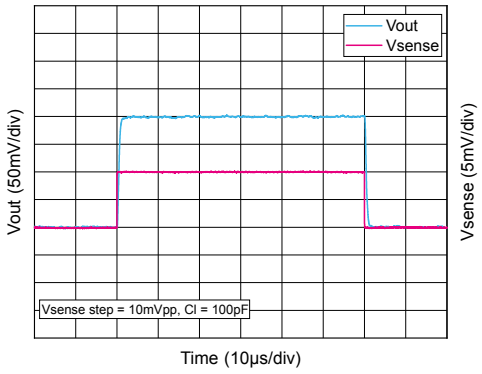


Figure 32. Large signal response

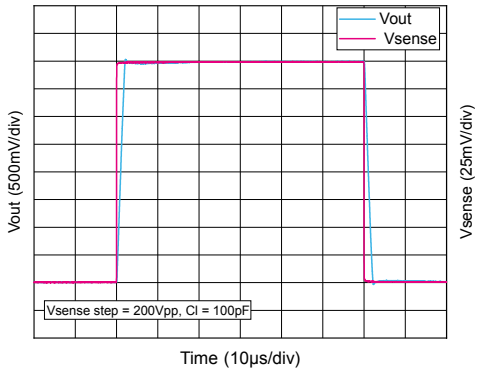


Figure 33. Positive settling time 0.5%

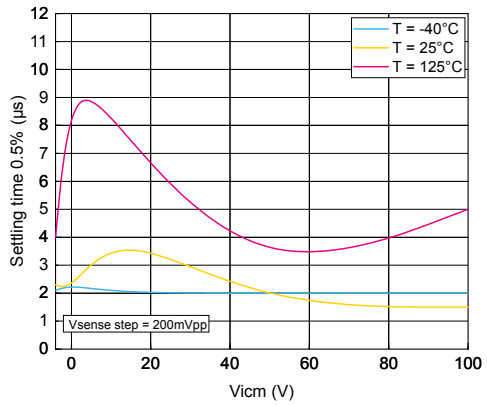


Figure 34. Negative settling time 0.5%

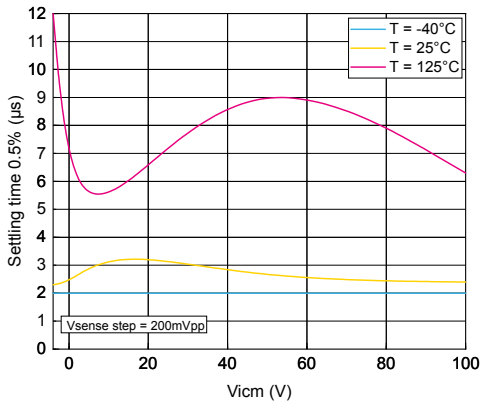


Figure 35. 12 V positive common-mode step response recovery

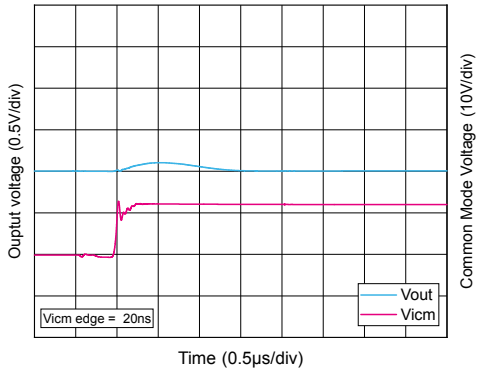


Figure 36. 12 V negative common-mode step response recovery

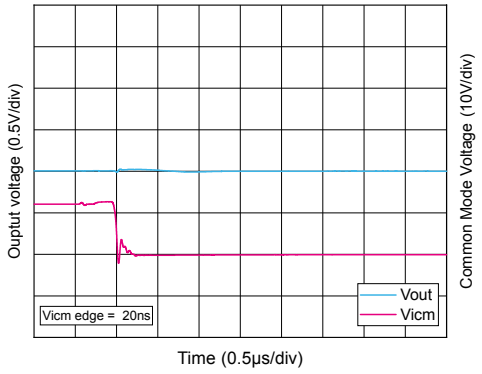


Figure 37. 48 V positive common-mode step response recovery

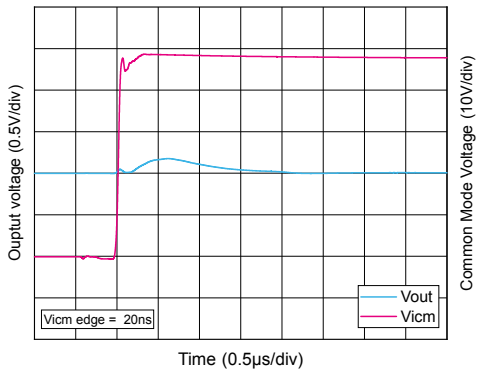


Figure 38. 48 V negative common-mode step response recovery

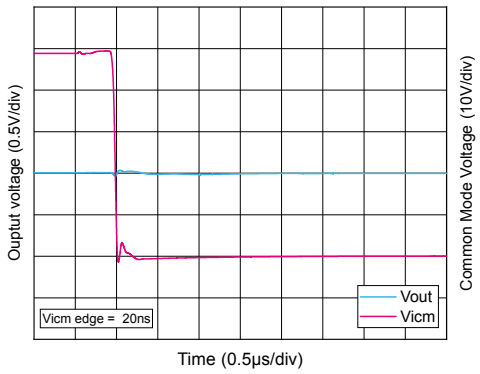


Figure 39. 100 V positive common-mode step response recovery

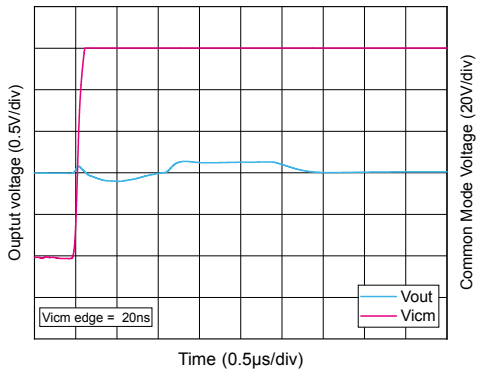


Figure 40. 100 V negative common-mode step response recovery

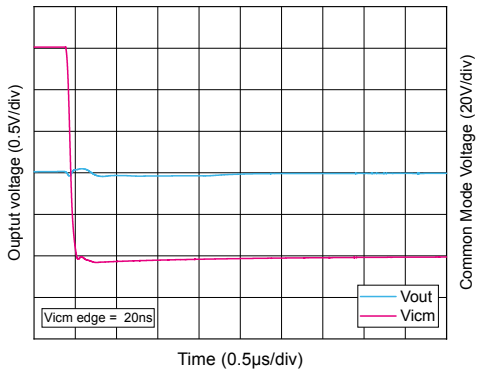


Figure 41. PSRR vs. frequency

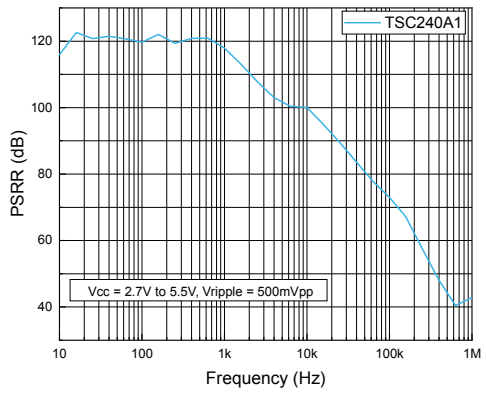


Figure 42. CMRR vs. frequency

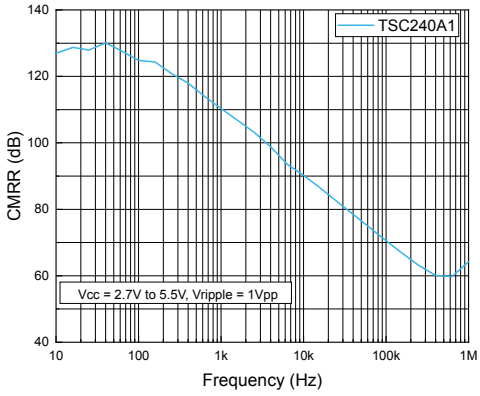


Figure 43. Positive overvoltage recovery

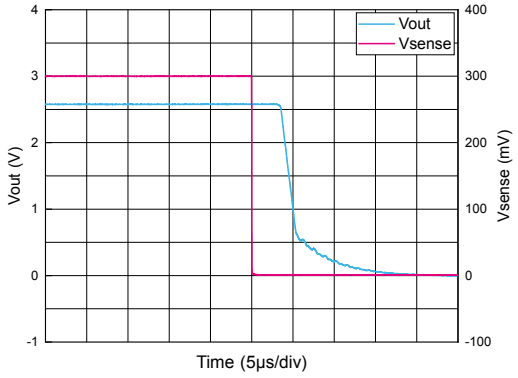


Figure 44. Negative overvoltage recovery

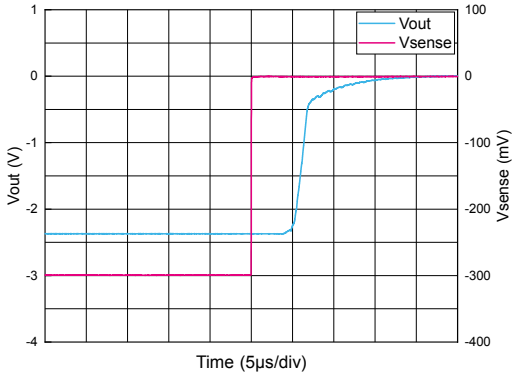


Figure 45. Overvoltage recovery vs. V_{ICM}

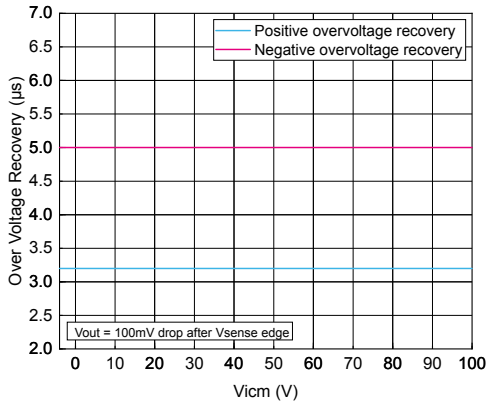


Figure 46. Noise vs. frequency

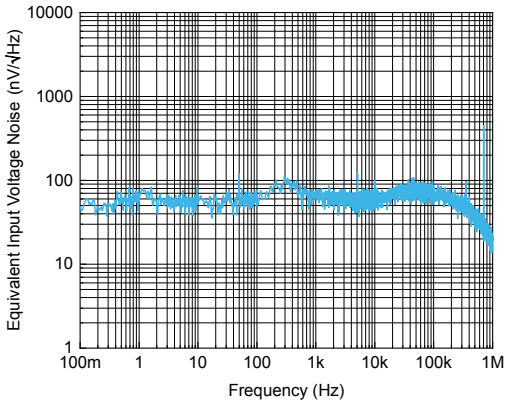


Figure 47. 0.1 Hz to 10 Hz voltage noise

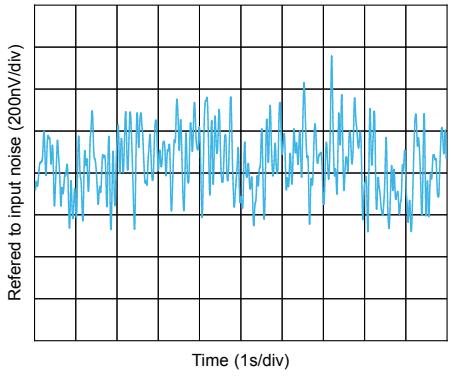


Figure 48. Power-up time delay

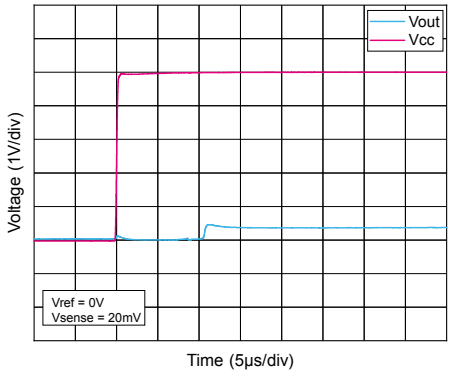
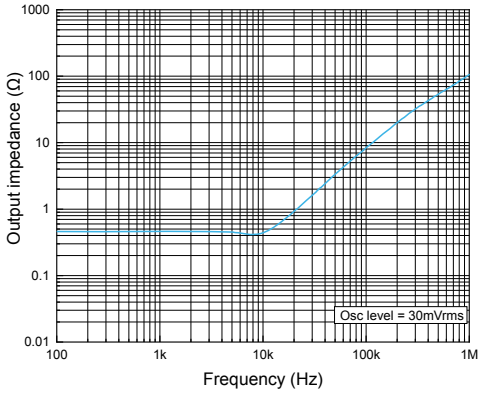


Figure 49. Output impedance vs. frequency



5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SO8 package information

Figure 50. SO8 package outline

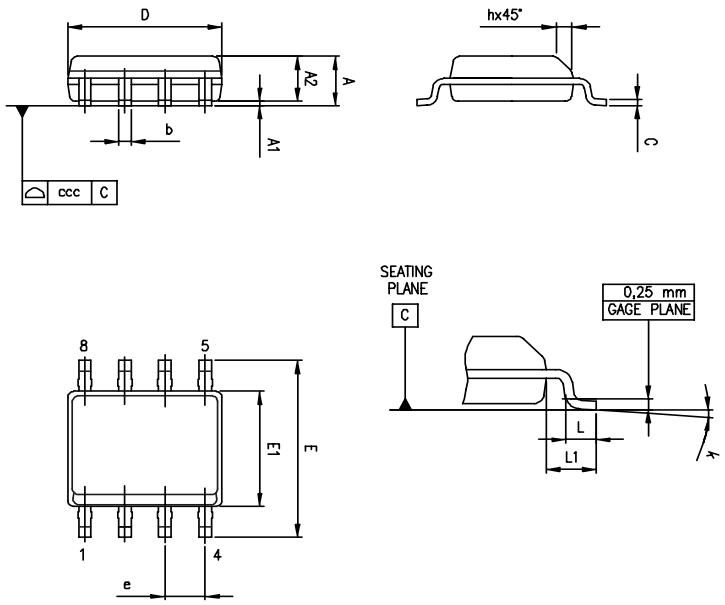


Table 5. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

5.2 TSSOP8 package information

Figure 51. **TSSOP8 package outline**

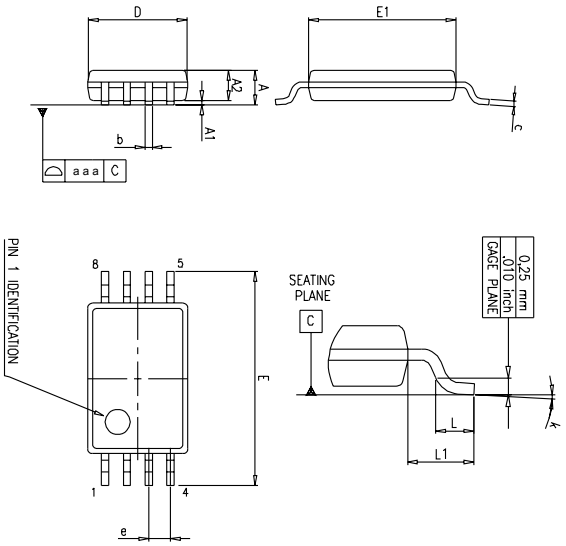


Table 6. **TSSOP8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.10			0.004	

6 Ordering information

Table 7. Order codes

Order code	Gain (V/V)	Temp. range	Package	Packaging	Marking
TSC240A1IDT	20	-40 to 125 °C	SO8	Tape & Reel	240A1I
TSC240A1IPT			TSSOP8		240A1
TSC240A1IYDT (1)			SO8		240A1IY
TSC240A1IYPT (1)			TSSOP8		40A1Y

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.*

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
23-Sep-2025	1	Initial release.
14-Oct-2025	2	Updated features and applications on the cover page.

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