Features

- 4 data-line protection
- Protects VBUS
- Very low capacitance: 3 pF typ.
- Peak pulse power (8/20 µs): 130 W typ.
- SOT23-6L package
- RoHS compliant

Benefits

- Very low capacitance between lines to GND for optimized data integrity and speed
- Low PCB space consumption, 9 mm² maximum footprint
- Enhanced ESD protection: IEC 61000-4-2 level 4 compliance guaranteed at device level, hence greater immunity at system level
- ESD protection of VBUS; allows ESD current flowing to ground when ESD event occurs on data line
- High reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

- USB 2.0 ports up to 480 Mb/s (high speed)
- Backwards compatible with USB 1.1 low and full speed
- Ethernet port: 10/100 Mb/s
- SIM card protection
- Video line protection
- Portable electronics

Description

The USBLC6-4 is a monolithic application specific device dedicated to ESD protection of high speed interfaces, such as USB 2.0, Ethernet links and video lines.

Its very low line capacitance secures a high level of signal integrity without compromising in protecting sensitive chips against the most stringent characterized ESD strikes.
1 Characteristics

Table 1. Absolute ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PP}$</td>
<td>Peak pulse voltage</td>
<td>IEC 61000-4-2 air discharge</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IEC 61000-4-2 contact discharge</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MIL STD883C-Method 3015-6</td>
<td>25</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage temperature range</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating junction temperature range</td>
<td>-40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_L$</td>
<td>Lead solder temperature (10 seconds duration)</td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

Table 2. Electrical characteristics ($T_{amb} = 25$ °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{RM}$</td>
<td>Leakage current</td>
<td>$V_{RM} = 5.25$ V</td>
<td>10</td>
<td>150</td>
</tr>
<tr>
<td>$V_{BR}$</td>
<td>Breakdown voltage between $V_{BUS}$ and GND</td>
<td>$I_R = 1$ mA</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td>$V_F$</td>
<td>Forward voltage</td>
<td>$I_F = 10$ mA</td>
<td>0.86</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CL}$</td>
<td>Clamping voltage</td>
<td>$I_{PP} = 1$ A, 8/20 μs Any I/O pin to GND</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{PP} = 5$ A, 8/20 μs Any I/O pin to GND</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>$C_{i/o-GND}$</td>
<td>Capacitance between I/O and GND</td>
<td>$V_R = 1.65$ V</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>$\Delta C_{i/o-GND}$</td>
<td></td>
<td></td>
<td>0.015</td>
<td></td>
</tr>
<tr>
<td>$C_{i/o-i/o}$</td>
<td>Capacitance between I/O</td>
<td>$V_R = 1.65$ V</td>
<td>1.85</td>
<td>2.7</td>
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<tr>
<td>$\Delta C_{i/o-i/o}$</td>
<td></td>
<td></td>
<td>0.04</td>
<td></td>
</tr>
</tbody>
</table>
**Figure 2. Capacitance versus voltage (typical values)**

![Capacitance versus voltage graph](image1)

- **Data line voltage (V)**: 0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0
- **C (pF)**: 0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0
- **F (MHz)**: 1, 10, 100, 1000
- **V = 30 mV**
- **T = 25°C**
- **OSC RMS**

**Figure 3. Line capacitance versus frequency (typical values)**

![Line capacitance versus frequency graph](image2)

- **Data line voltage (V)**: 0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0
- **C (pF)**: 0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0
- **F (MHz)**: 0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0
- **V = 30 mV**
- **T = 25°C**
- **OSC RMS**

**Figure 4. Relative variation of leakage current versus junction temperature (typical values)**

![Relative variation of leakage current graph](image3)

- **ln |I(Tj)| / ln |I(Tj) = 25°C|**
- **Tj (°C)**: 25, 50, 75, 100, 125
- **I(Tj)/I(Tj) = 25°C**

**Figure 5. Frequency response**

![Frequency response graph](image4)

- **S21 (dB)**: -20.00, -15.00, -10.00, -5.00, 0.00
- **F (MHz)**: 100.0kHz, 1.0MHz, 10.0MHz, 100.0MHz, 1.0GHz

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**USBLC6-4**

**Characteristics**

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**DocID11068 Rev 7**

3/13
2 Technical information

2.1 Surge protection

The USBLC6-4SC6 is particularly optimized to provide surge protection based on the rail to rail topology.

The clamping voltage \( V_{\text{CL}} \) can be calculated as follows:

\[
\begin{align*}
V_{\text{CL}+} &= V_{\text{TRANSIL}} + V_F \\
V_{\text{CL}-} &= -V_F
\end{align*}
\]

with: \( V_F = V_T + R_d I_p \)

\( V_F \) forward drop voltage, \( V_T \) forward drop threshold voltage

(\( V_F \) forward drop voltage, \( V_T \) forward drop threshold voltage)

Calculation example

We assume that the value of the dynamic resistance of the clamping diode is typically:

\( R_d = 0.5 \, \Omega \) and \( V_T = 1.1 \, \text{V} \).

For an IEC 61000-4-2 surge level 4 (Contact Discharge: \( V_g = 8 \, \text{kV, R_g = 330} \, \Omega \)), \( V_{\text{BUS}} = +5 \, \text{V} \), and if in a first approximation, we assume that:

\( I_p = \frac{V_g}{R_g} = 24 \, \text{A} \).

So, we find:

\[
\begin{align*}
V_{\text{CL}+} &= +31.2 \, \text{V} \\
V_{\text{CL}-} &= -13.1 \, \text{V}
\end{align*}
\]

Note: The calculations do not take into account phenomena due to parasitic inductances.

2.2 Surge protection application example

If we consider that the connections from the pin \( V_{\text{BUS}} \) to \( V_{\text{CC}} \), from I/O to data line and from GND to PCB GND plane are implemented as racks 10 mm long and 0.5 mm large, we can assume that the parasitic inductances \( L_{\text{VBUS}} \), \( L_{\text{I/O}} \) and \( L_{\text{GND}} \) of these tracks are about 6 nH.

So, when an IEC 61000-4-2 surge occurs, due to the rise time of this spike (\( t_r = 1 \, \text{ns} \)), the voltage \( V_{\text{CL}} \) has an extra value equal to \( L_{\text{I/O}} \cdot \frac{\text{d}I}{\text{d}t} + L_{\text{GND}} \cdot \frac{\text{d}I}{\text{d}t} \)

The \( \frac{\text{d}I}{\text{d}t} \) is calculated as:

\[
\frac{\text{d}I}{\text{d}t} = \frac{I_p}{t_r} = 24 \, \text{A/\text{ns}}
\]

The overvoltage due to the parasitic inductances is:

\[
L_{\text{I/O}} \cdot \frac{\text{d}I}{\text{d}t} + L_{\text{GND}} \cdot \frac{\text{d}I}{\text{d}t} = 6 \times 24 = 144 \, \text{V}
\]

By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

\[
\begin{align*}
V_{\text{CL}+} &= +31.2 + 144 + 144 = 319.2 \, \text{V} \\
V_{\text{CL}-} &= -13.1 - 144 -144 = -301.1 \, \text{V}
\end{align*}
\]

We can significantly reduce this phenomena with simple layout optimization. It is for this reason that some recommendations have to be followed (see 2.3: How to ensure good ESD protection).
2.3 How to ensure good ESD protection

While the USBLC6-4SC6 provides high immunity to ESD surge, efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from data lines to I/O pins, from VCC to the VBUS pin and from GND plane to GND pin must be as short as possible to avoid overvoltages due to parasitic phenomena (see Figure 7 and Figure 8 for layout considerations).

Figure 6. ESD behavior: parasitic phenomena due to unsuitable layout

![ESD behavior diagram](image)

\[
\begin{align*}
V_{CL+} &= V_{TRANSIL} + V_F + L_{I/O} \frac{di}{dt} + L_{GND} \frac{di}{dt} \\
V_{CL-} &= -V_{TRANSIL} - V_F - L_{I/O} \frac{di}{dt} - L_{GND} \frac{di}{dt}
\end{align*}
\]

\( t = 1 \text{ ns} \)

Figure 7. ESD behavior: optimized layout and addition of a capacitance of 100 nF

![Optimized layout diagram](image)

Figure 8. ESD behavior: measurement conditions (with coupling capacitance)

![Measurement conditions diagram](image)
Note: The measurements have been done with the USBLC6-4SC6 in open circuit.

Important:

A good precaution to take is to put the protection device as close as possible to the disturbance source (generally the connector).

2.4 Crosstalk behavior

2.4.1 Crosstalk phenomenon

The crosstalk phenomenon is due to the coupling between 2 lines. The coupling factor ($\beta_{12}$ or $\beta_{21}$) increases when the gap across lines decreases, particularly in silicon dice. In the above example the expected signal on load $R_{L2}$ is $\alpha_{2}V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21}V_{G1}$. This part of the $V_{G1}$ signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).
Figure 12. Analog crosstalk measurements

Figure 12. shows the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -55 dB (see Figure 13.).

Figure 13. Analog crosstalk results

As the USBLC6-4SC6 is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (Figure 5.) gives attenuation information and shows that the USBLC6-4SC6 is well suitable for data line transmission up to 480 Mbit/s while it works as a filter for undesirable signals like GSM (900 MHz) frequencies, for instance.
2.5 Application examples

Figure 14. USB 2.0 port application diagram using USBLC6-4SC6

<table>
<thead>
<tr>
<th>Mode</th>
<th>SW1</th>
<th>SW2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low Speed LS</td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>Full Speed FS</td>
<td>Closed</td>
<td>Open</td>
</tr>
<tr>
<td>High Speed HS</td>
<td>Closed then open</td>
<td>Open</td>
</tr>
</tbody>
</table>

Figure 15. T1/E1/Ethernet protection
2.6 PSPICE model

*Figure 16.* shows the PSPICE model of one USBLC6-4SC6 cell. In this model, the diodes are defined by the PSPICE parameters given in *Figure 17.*

![PSPICE model](image)

*Note:* This simulation model is available only for an ambient temperature of 27 °C.

<table>
<thead>
<tr>
<th></th>
<th>Dlow</th>
<th>Dhigh</th>
<th>Dzener</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV</td>
<td>50</td>
<td>50</td>
<td>7.3</td>
</tr>
<tr>
<td>CJ0</td>
<td>2.4p</td>
<td>2.4p</td>
<td>20p</td>
</tr>
<tr>
<td>IBV</td>
<td>1m</td>
<td>1m</td>
<td>1m</td>
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<tr>
<td>IKF</td>
<td>0.008</td>
<td>0.018</td>
<td>2.42</td>
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<td>IS</td>
<td>55.2p</td>
<td>2.27f</td>
<td>3.21p</td>
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<td>ISR</td>
<td>100p</td>
<td>100p</td>
<td>100p</td>
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<tr>
<td>N</td>
<td>1.62</td>
<td>1.13</td>
<td>1.24</td>
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<tr>
<td>M</td>
<td>0.3333</td>
<td>0.3333</td>
<td>0.3333</td>
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<tr>
<td>RS</td>
<td>0.26</td>
<td>0.63</td>
<td>0.42</td>
</tr>
<tr>
<td>VJ</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>TT</td>
<td>0.1u</td>
<td>0.1u</td>
<td>0.1u</td>
</tr>
</tbody>
</table>

![PSPICE parameters](image)
3 Ordering information scheme

Figure 19. Ordering information scheme

Product Designation
Low capacitance
Breakdown Voltage
6 = 6 Volts
Number of lines protected
4 = 4 lines
Package
SC6 = SOT23-6L
4 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. SOT23-6L package dimensions

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Dimensions</th>
<th>Millimeters</th>
<th>Inches</th>
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<tbody>
<tr>
<td>A</td>
<td>0.90</td>
<td>1.45</td>
<td>0.035</td>
</tr>
<tr>
<td>A1</td>
<td>0</td>
<td>0.10</td>
<td>0</td>
</tr>
<tr>
<td>A2</td>
<td>0.90</td>
<td>1.30</td>
<td>0.035</td>
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<tr>
<td>b</td>
<td>0.35</td>
<td>0.50</td>
<td>0.014</td>
</tr>
<tr>
<td>C</td>
<td>0.09</td>
<td>0.20</td>
<td>0.004</td>
</tr>
<tr>
<td>D</td>
<td>2.80</td>
<td>3.05</td>
<td>0.110</td>
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<tr>
<td>E</td>
<td>1.50</td>
<td>1.75</td>
<td>0.059</td>
</tr>
<tr>
<td>e</td>
<td>0.95</td>
<td></td>
<td>0.037</td>
</tr>
<tr>
<td>H</td>
<td>2.60</td>
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<td>0.102</td>
</tr>
<tr>
<td>L</td>
<td>0.10</td>
<td>0.60</td>
<td>0.004</td>
</tr>
<tr>
<td>ϑ</td>
<td>0°</td>
<td>10°</td>
<td>0°</td>
</tr>
</tbody>
</table>

Figure 20. SOT23-6L footprint (mm)  Figure 21. SOT23-6L marking
5 Ordering information

Table 4. Ordering information

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Weight</th>
<th>Base qty</th>
<th>Delivery mode</th>
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</thead>
<tbody>
<tr>
<td>USBLC6-4SC6</td>
<td>UL46</td>
<td>SOT23-6L</td>
<td>16.7 mg</td>
<td>3000</td>
<td>Tape and reel</td>
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</table>

6 Revision history

Table 5. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<td>1</td>
<td>First issue.</td>
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<tr>
<td>28-Feb-2005</td>
<td>2</td>
<td>Minor layout update. No content change.</td>
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<tr>
<td>04-Feb-2008</td>
<td>3</td>
<td>Updated operating junction temperature range in absolute ratings, page 2. Updated Section 2: Technical information. Updated marking illustration Figure 21. Reformatted to current standard.</td>
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<tr>
<td>23-Sep-2011</td>
<td>4</td>
<td>Updated leakage current at ( V_{\text{RM}} = 5.25 ) V as specified in USB standard. Updated marking illustration Figure 21.</td>
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<tr>
<td>13-Oct-2015</td>
<td>5</td>
<td>Updated features in cover page and Table 2.</td>
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<tr>
<td>26-Oct-2015</td>
<td>6</td>
<td>Updated features in cover page.</td>
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<tr>
<td>03-Nov-2015</td>
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<td>Minor text changes.</td>
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