



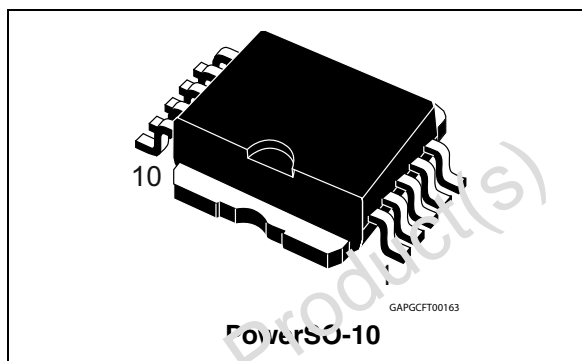
VB125ASPTR-E

High voltage ignition coil driver power integrated circuit

Type	V _{cl}	I _{cl}	I _{cc}
VB125ASPTR-E	340 V	11.1 A	200 mA

Features

- ECOPACK[®]: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Primary coil voltage internally set
- Coil current limit internally set
- Logic level compatible input
- Battery operation
- Single flag-on coil current
- Temperature compensated high voltage clamp



Description

The VB125ASPTR-E is a high voltage power integrated circuit made using the STMicroelectronics™ VIPower™ M1-2 technology, with vertical current flow power darlington and logic level compatible driving circuit.

The VB125ASPTR-E can be directly biased by using the 12 V battery voltage, thus avoiding to use a low voltage regulator. It has built-in protection circuit for coil current limiting and collector voltage clamping. It is suitable as smart, high voltage, high current interface in advanced electronic ignition system.

Table 1. Device summary

Package	Order code	
	Tube	Tape and reel
PowerSO-10	—	VB125ASPTR-E

Contents

1	Block diagram and pins description	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	7
2.3	Electrical characteristics	8
3	Package and packing information	13
3.1	ECOPACK®	13
3.2	PowerSO-10 mechanical data	13
3.3	PowerSO-10 packing information	15
4	Revision history	16

Obsolete Product(s) - Obsolete Product(s)

List of tables

Table 1.	Device summary	1
Table 2.	Pin function	5
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data	7
Table 5.	Electrical characteristics	8
Table 6.	PowerSO-10 mechanical data	14
Table 7.	Document revision history	16

Obsolete Product(s) - Obsolete Product(s)

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	5
Figure 3.	Temperature compensated high voltage clamp	9
Figure 4.	Electrical characteristic of the circuit shown in <i>Figure 3</i>	10
Figure 5.	V_{cl} with load $L \cong 4$ mH.	10
Figure 6.	Output current waveform after thermal protection activation	11
Figure 7.	Waveform	11
Figure 8.	Threshold collector current vs temperature	12
Figure 9.	Application circuit	12
Figure 10.	PowerSO-10 package dimensions	13
Figure 11.	PowerSO-10 suggested PAD layout.	15
Figure 12.	PowerSO-10 tube shipment (no suffix)	15
Figure 13.	PowerSO-10 tape and reel shipment (suffix "13TR")	15

1 Block diagram and pins description

Figure 1. Block diagram

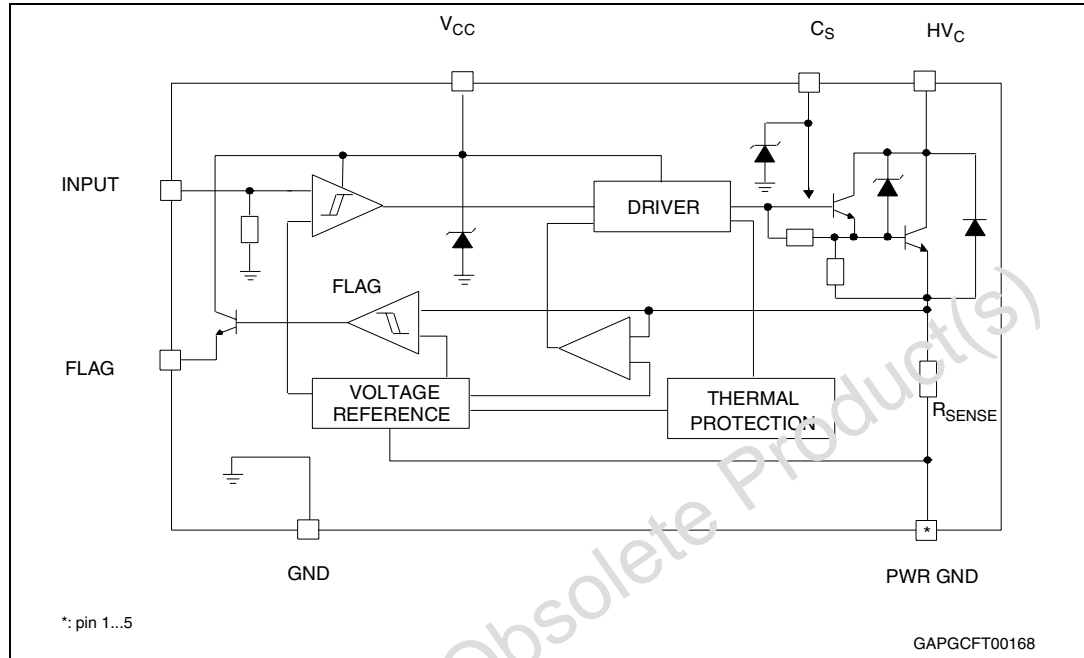


Figure 2. Configuration diagram (top view)

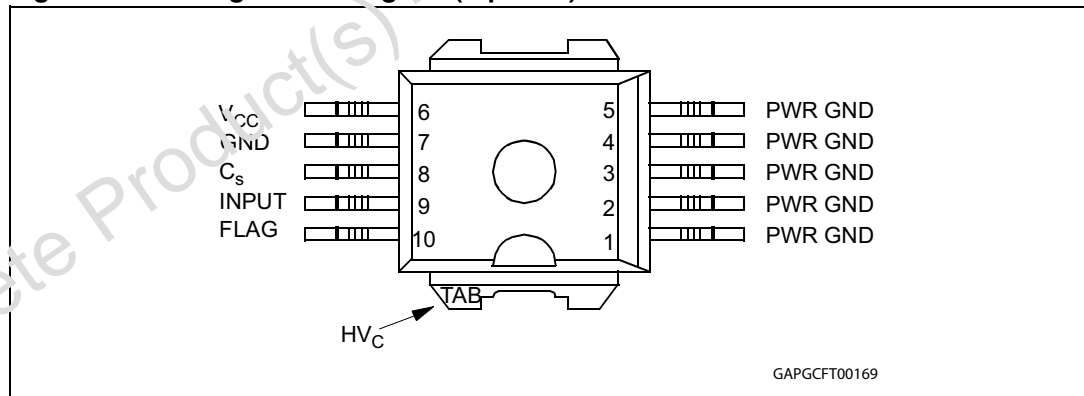


Table 2. Pin function

Pin number	Name	Function
1÷5	PWR GND	Emitter power ground
6	V _{CC}	Logic supply voltage
7	GND	Control ground ⁽¹⁾
8	C _s	Logic level supply voltage filter capacitor
9	INPUT	Logic input channel

Table 2. Pin function (continued)

Pin number	Name	Function
10	FLAG	Diagnostic output signal
TAB	HV _C	Primary coil output signal

1. Pin 7 must be connected to pins 1,5 externally.

Obsolete Product(s) - Obsolete Product(s)

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
HV_C	Collector voltage (internally limited)	-0.3 to V_{CC}	V
I_C	Collector current (internally limited)	11.1	A
V_{CC}	Driving stage supply voltage	-0.2 to 40	V
I_{CC}	Driving circuit supply current	400	mA
I_S	Logic circuit supply current	100	mA
V_{IN}	Input voltage	-0.3 to 6	V
P_{tot}	Power dissipation at $T_C \leq 25\text{ }^\circ\text{C}$	100	W
V_{ESD}	ESD voltage (HV_C pin)	-4 to 4	KV
V_{ESD}	ESD voltage (other pin)	-2 to 2	KV
T_j	Junction operating temperature	-40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	1.2	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	62.5	$^\circ\text{C}/\text{W}$

2.3 Electrical characteristics

$V_{CC} = 6$ to 24 V; -40 °C $< T_j < 125$ °C; $R_{coil} = 400$ to 700 mΩ; $L_{coil} = 2$ to 6 mH unless otherwise specified^(a).

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{cl}	High voltage clamp	$I_C = 7$ A ⁽¹⁾	340	370	400	V
		$I_C = 2$ A; Switching off from 7 A	300		400	V
$V_{cg(sat)}$	Power stage saturation voltage	$I_C = 6$ A; $V_{CC} = 14$ V; $V_{IN} = 4$ V			2	V
		$I_C = 7$ A; $V_{CC} = 14$ V; $V_{IN} = 4$ V ⁽²⁾			3	V
$I_{CC(off)}$	Power-off supply current	$V_{IN} = 0.4$ V; $V_{CC} = 14$ V			20	mA
		$V_{IN} = 0.4$ V; $V_{CC} = 24$ V ^{(3) (4)}			80	mA
$I_{CC(on)}$	Power-on supply current	$V_{IN} = 4$ V; $V_{CC} < 14$ V; $I_C = 4$ A			200	mA
		$V_{IN} = 4$ V; $V_{CC} = 24$ V; $I_C = 4$ A ^{(3) (4)}			300	mA
I_{cl}	Collector current limit	$V_{IN} = 4$ V; 10 V $< V_{CC} < 19$ V ⁽⁵⁾ (6)	8.8		11.1	A
V_{INH}	High level input voltage		4			V
V_{INL}	Low level input voltage				0.8	V
$V_{IN(hyst)}$	Hysteresis input voltage		0.4			V
I_{INH}	High level input current	$V_{IN} = 4$ V	10		150	μA
I_{INL}	Low level input current	$V_{IN} = 0.8$ V	0		30	μA
V_{diagH}	High level diagnostic output voltage	$R_{EXT} = 22$ KΩ; $C_{EXT} = 1$ nF ⁽⁷⁾	3.5		5.5	V
V_{diagL}	Low level diagnostic output voltage	$R_{EXT} = 22$ KΩ; $C_{EXT} = 1$ nF ⁽⁷⁾			0.5	V
$I_{C(diag)}$	Threshold level collector current ⁽⁶⁾⁽⁸⁾ see Figure 7	$T_j = -40$ °C; 10 V $< V_{CC} < 19$ V	5.45		6.8	A
		$T_j = 25$ °C; 10 V $< V_{CC} < 19$ V	5.55		6.35	A
		$T_j = 125$ °C; 10 V $< V_{CC} < 19$ V	5.5		6.35	A
		$T_j = -40$ °C; $V_{CC} = 7$ V	5.9		6.6	A
		$T_j = 25$ °C; $V_{CC} = 7$ V	5.7		6.3	A
		$T_j = 125$ °C; $V_{CC} = 7$ V	5.5		6.3	A
I_{diag}	High level flag output current	$I_C > I_{C(diag)}$ ⁽⁶⁾	0.5			mA
$I_{diag(leak)}$	Leakage current on flag output	$V_{IN} = \text{low}$			10	μA
V_f	Diode forward voltage	$I_f = 10$ A			3.5	V
$E_{s/b}$	Single pulse avalanche energy		300			mJ

a. Only functionality is guaranteed with 6 V $< V_{CC} < 10$ V and $V_{CC} > 24$ V and not parameter values.

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_j	Thermal output current control	IN = ON ⁽⁹⁾	150			°C
$t_{d(on)}$	Turn-on delay time of output current	See ⁽¹⁰⁾		1		µs
$t_{d(off)}$	Turn-off delay time of output current	See ⁽¹¹⁾	7		60	µs

- In the high voltage clamping structure of this device a temperature compensation has been implemented. The circuit schematic is shown in *Figure 3*. The KVbe cell takes care of the temperature compensation. The whole electrical characteristic of the new circuit is shown in *Figure 4*. Up to $V_{CE} = nV_Z$ no current flows into the collector (just the leakage current of the power stage); for $nV_Z < V_{CE} < V_{cl}$ a current begins to flow across the resistances of the KVbe compensation circuit (typical slope $\approx 20\text{ K}\Omega$) as soon as the V_{cl} reached the dynamic resistance drop to $\sim 4\ \Omega$ to protect the device against overvoltage (See *Figure 5*).
- The saturation voltage of the Power stage includes the drop on the sensing resistor.
- Considering the different ways of operation of the device (with or without spark, etc...) there are some short periods of time in which the output terminal (HVC) is pulled below ground by a negative current due to leakage inductances and stray capacitances of the ignition coil. With VIPower devices if no corrective action is taken, these negative currents can cause parasitic glitches on the diagnostic output. To kill this potential problem, a circuit that avoids the possibility for the HVC to be pulled under ground, by sending the required negative current from the battery is implemented in the VB125ASPTR-E. For this reason there are some short periods in which a current exceeding 220 mA flows in the VCC pin.
- A zener protection of 16 V (typical) is placed on the supply pin (V_{CC}) of the chip to protect the internal circuitry. For this reason, when the battery voltage exceeds that value, the current flowing into V_{CC} pin can be greater than the maximum current specified at $V_{CC} = 14\text{ V}$ (both in power on and power off conditions): it will be limited by an internal resistor.
- The primary coil current value I_{cl} must be measured 1 ms after desaturation of the power stage.
- These limits apply with regard to the minimum battery voltage and resistive drop on the coil and cables that permit to reach the limitation or diagnostic level.
- No internal pull-down.
- When I_C gets over $I_{C(diag)}$, the diagnostic output voltage rises to the high level and so it remains until the end of the input signal.
- $T_{jmin} = 150\text{ }^\circ\text{C}$ means that the behavior of the device will not be affected for junction temperature lower than $150\text{ }^\circ\text{C}$. For higher temperature, the thermal protection circuit begins its action reducing the I_{cl} limit according with the power dissipation. Chip temperature is a function of the R_{th} of the whole system in which the device will be operating (See *Figure 6*).
- Turn on delay time measured from 90% of input voltage rising edge to 10% of output voltage falling edge.
- Turn off delay time is defined as the time between the 90% of input pulse falling edge and the point where the HVC reaches 200 V.

Figure 3. Temperature compensated high voltage clamp

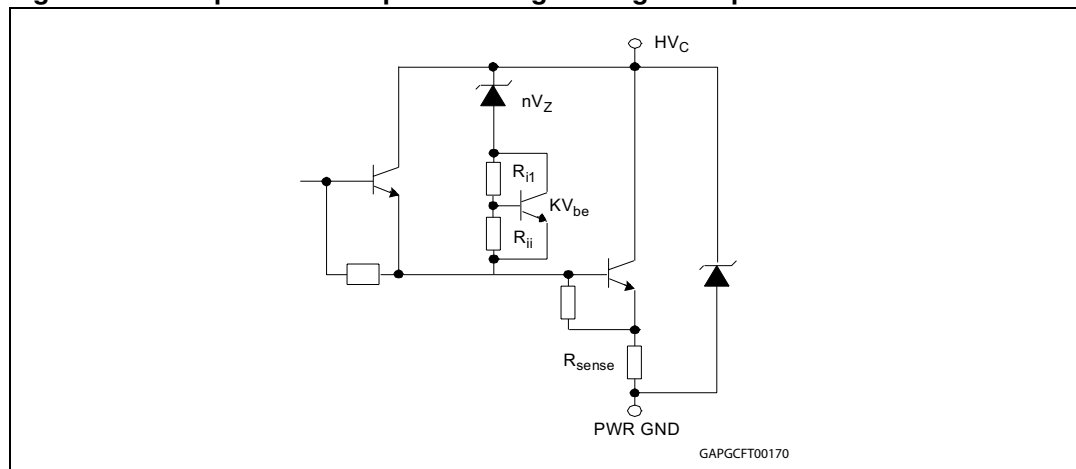


Figure 4. Electrical characteristic of the circuit shown in *Figure 3*

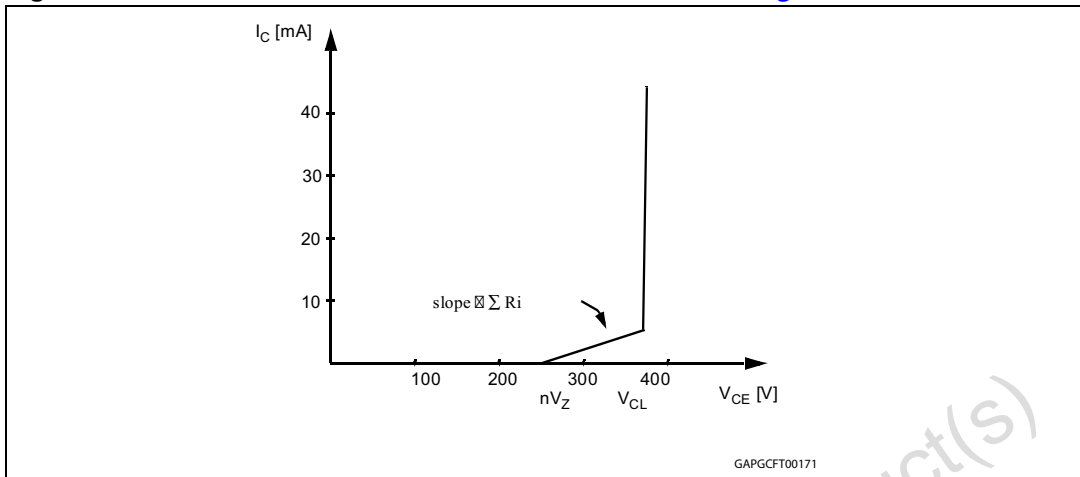


Figure 5. V_{cl} with load $L \cong 4 \text{ mH}$

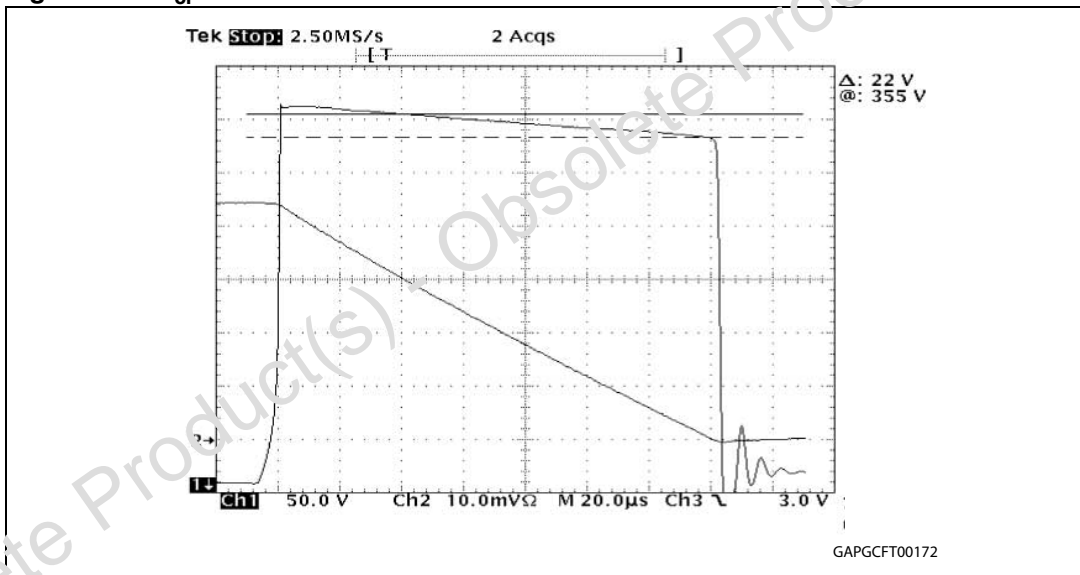


Figure 6. Output current waveform after thermal protection activation

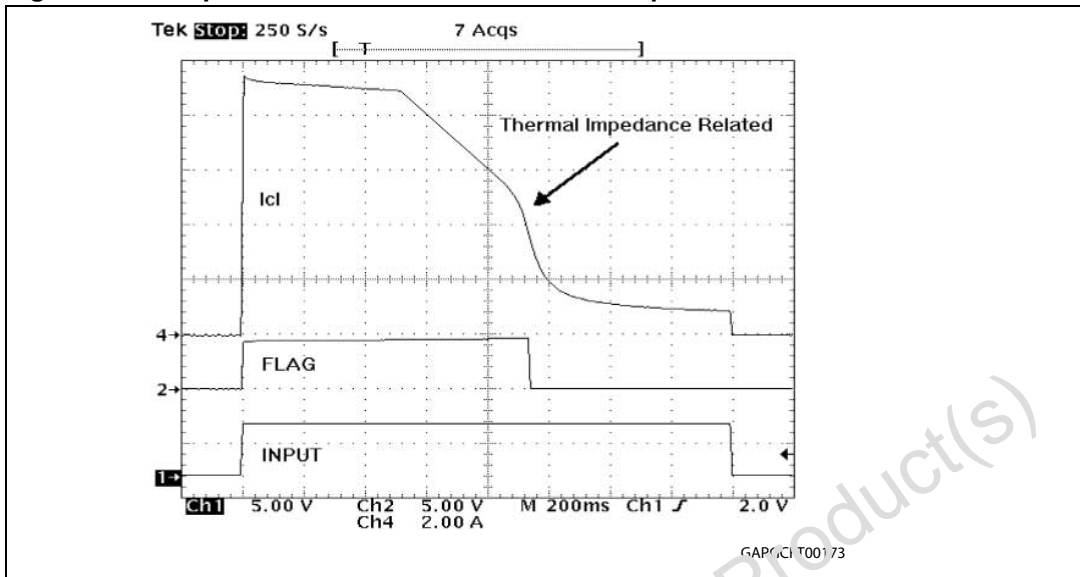


Figure 7. Waveform

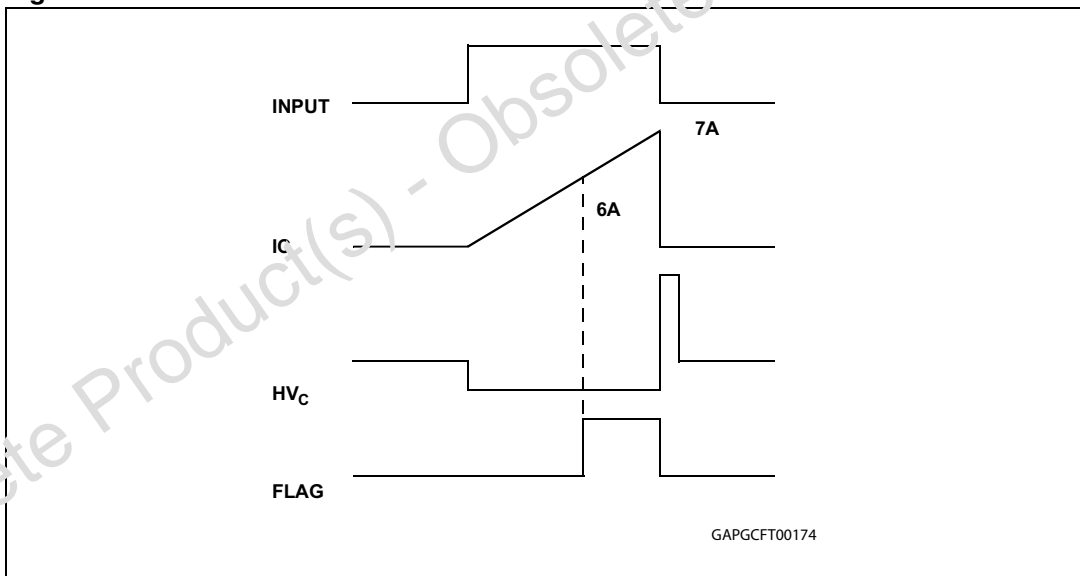


Figure 8. Threshold collector current vs temperature

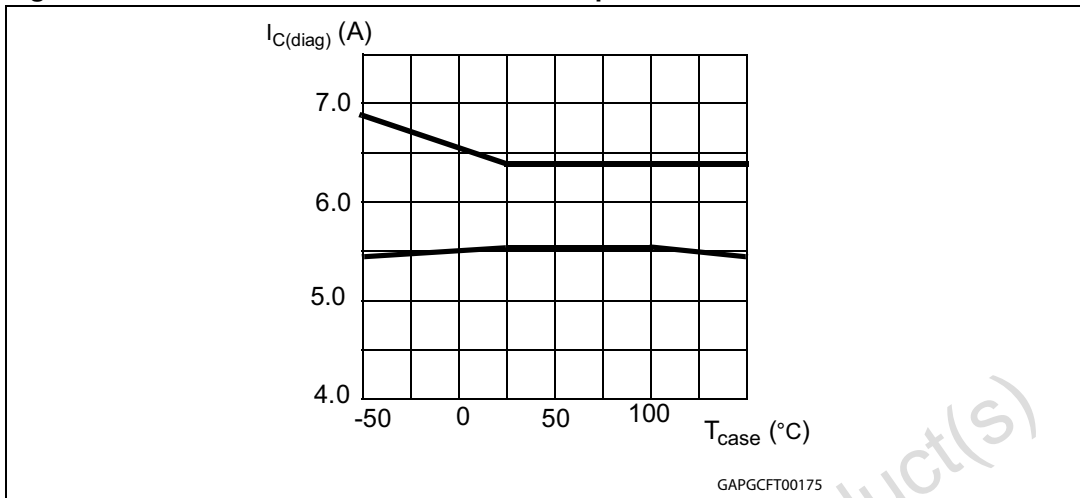
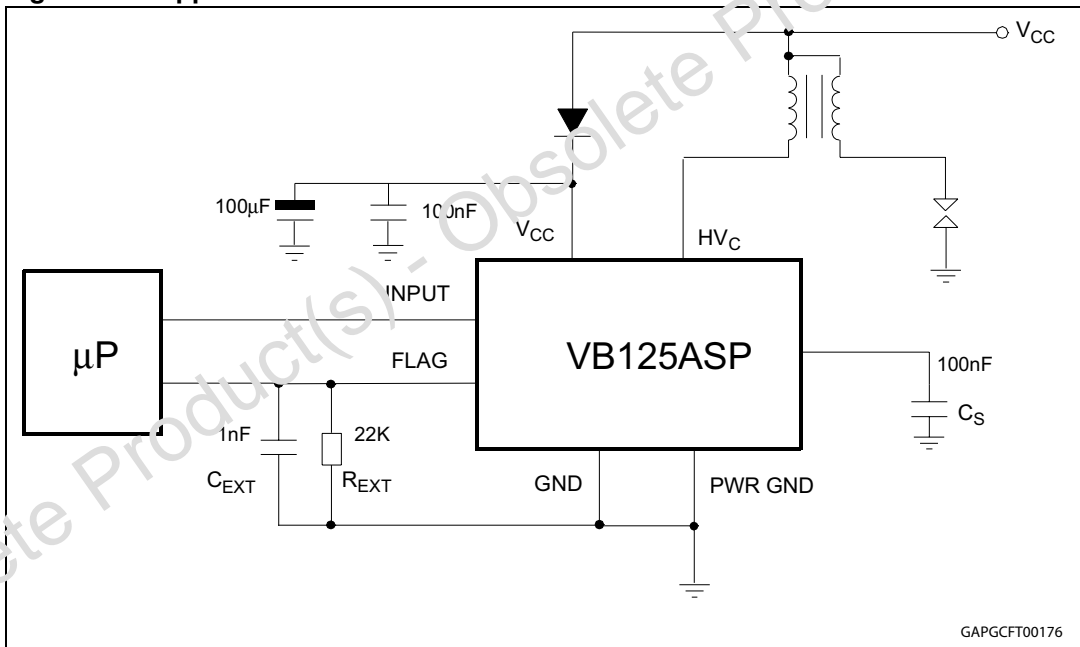


Figure 9. Application circuit



3 Package and packing information

3.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

3.2 PowerSO-10 mechanical data

Figure 10. PowerSO-10 package dimensions

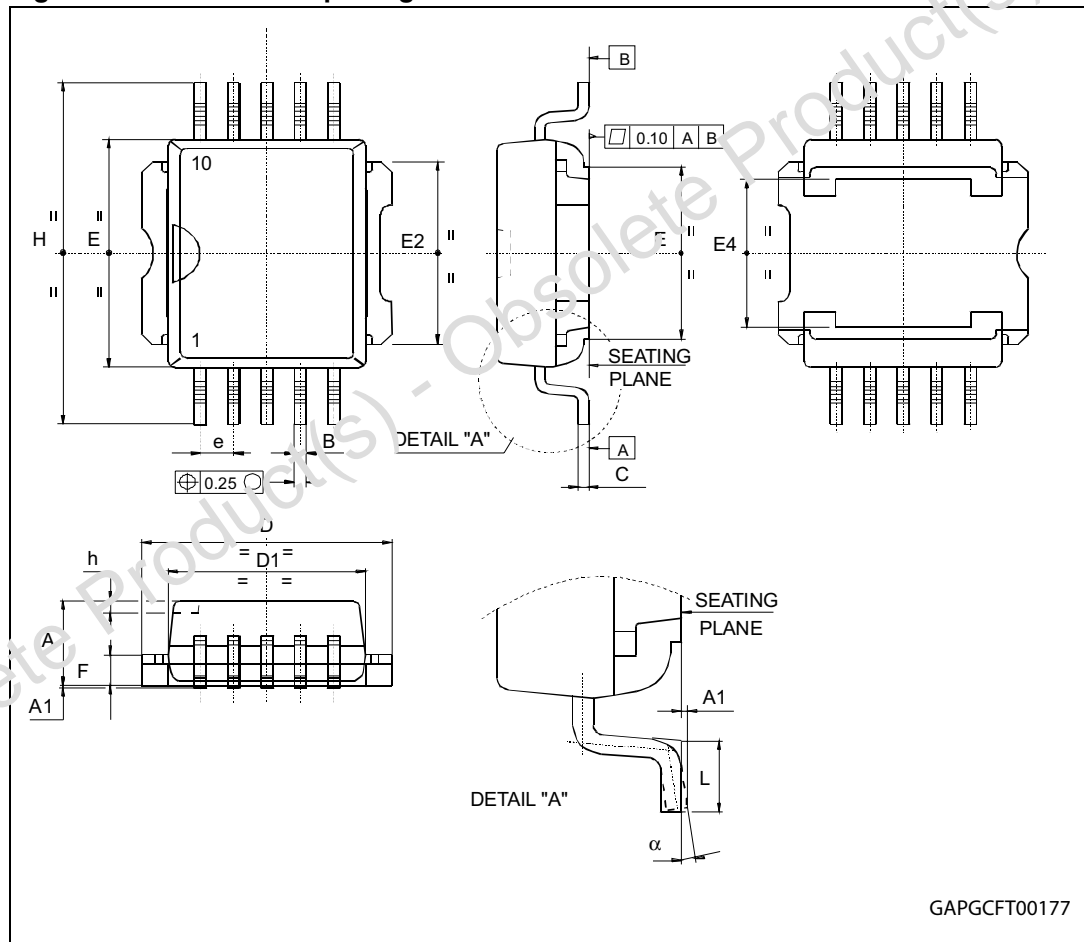


Table 6. PowerSO-10 mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	3.35		3.65	0.132		0.144
A ⁽¹⁾	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B ⁽¹⁾	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C ⁽¹⁾	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		0.299
E2 ⁽¹⁾	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 ⁽¹⁾	5.90		6.50	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F ⁽¹⁾	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H ⁽¹⁾	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L ⁽¹⁾	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α ⁽¹⁾	2°		8°	2°		8°

1. Muar only POA P013P.

3.3 PowerSO-10 packing information

Figure 11. PowerSO-10 suggested PAD layout

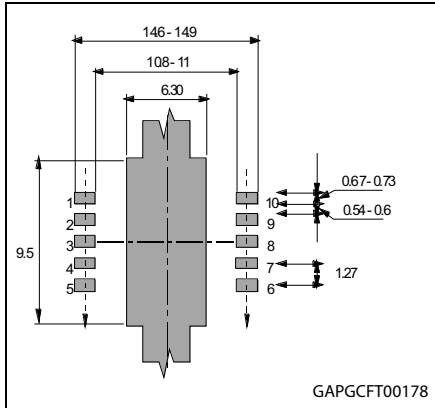


Figure 12. PowerSO-10 tube shipment (no suffix)

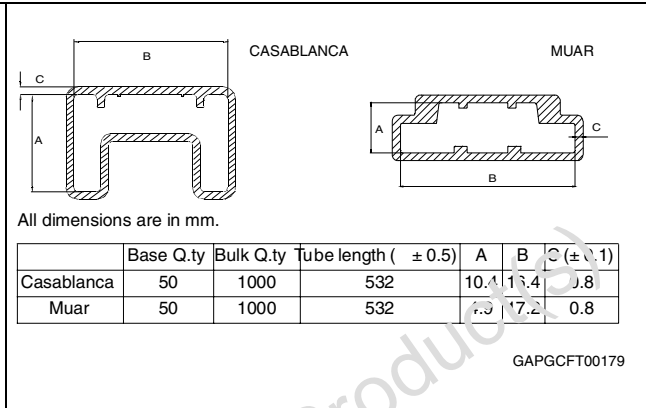
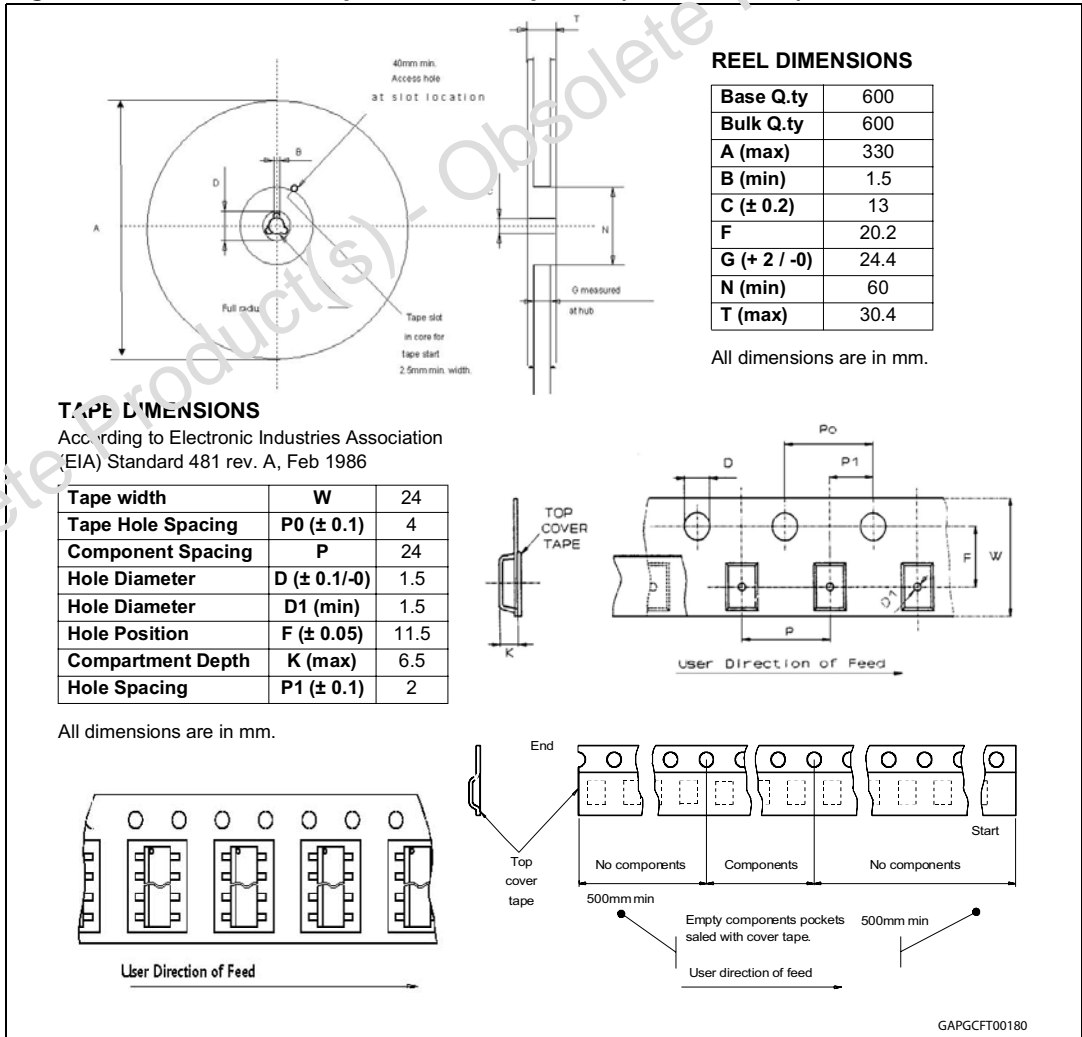


Figure 13. PowerSO-10 tape and reel shipment (suffix “-TR”)



4 Revision history

Table 7. Document revision history

Date	Revision	Changes
13-May-2011	1	Initial release.

Obsolete Product(s) - Obsolete Product(s)

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