



# VND5E050ACJ-E VND5E050ACK-E

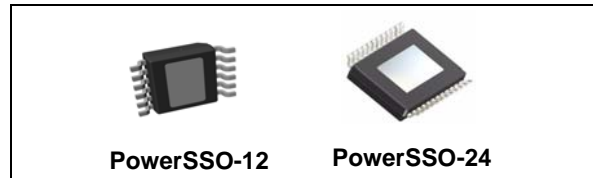
## Double channel high-side driver with analog current sense for automotive applications

### Features

Max transient supply voltage	$V_{CC}$	41 V
Operating voltage range	$V_{CC}$	4.5 to 28 V
Max On-state resistance (per ch.)	$R_{ON}$	50 m $\Omega$
Current limitation (typ)	$I_{LIMH}$	27 A
Off-state supply current	$I_S$	2 $\mu$ A <sup>(1)</sup>

1. Typical value with all loads connected.

- General
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Compliance with European directive 2002/95/EC
  - Very low current sense leakage
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide currents range
  - Current sense disable
  - Off-state open load detection
  - Output short to  $V_{CC}$  detection
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of  $V_{CC}$
  - Overtemperature shutdown with auto restart (thermal shutdown)



- Reverse battery protected
- Electrostatic discharge protection

### Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

### Description

The VND5E050ACJ-E and VND5E050ACK-E are double channel high-side drivers manufactured using ST proprietary VIPower<sup>®</sup> M0-5 technology and housed in PowerSSO-12 and PowerSSO-24 packages. The devices are designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. They also implement a 3 V and 5 V CMOS-compatible interface for use with any microcontroller.

The devices integrate advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, overtemperature indication, short-circuit to  $V_{CC}$  diagnosis on-state and off-state open-load detection.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS\_DIS pin high to share the external sense resistor with similar devices.

# Contents

<b>1</b>	<b>Block diagram and pin description</b>	<b>6</b>
<b>2</b>	<b>Electrical specifications</b>	<b>8</b>
2.1	Absolute maximum ratings	8
2.2	Thermal data	9
2.3	Electrical characteristics	9
2.4	Waveforms	18
2.5	Electrical characteristics curves	21
<b>3</b>	<b>Application information</b>	<b>24</b>
3.1	GND protection network against reverse battery	24
3.1.1	Solution 1: resistor in the ground line (RGND only)	24
3.1.2	Solution 2: diode (DGND) in the ground line	25
3.2	Load dump protection	25
3.3	MCU I/Os protection	25
3.4	Current sense and diagnostic	25
3.4.1	Short to VCC and off-state open-load detection	26
3.5	Maximum demagnetization energy (VCC = 13.5V)	28
<b>4</b>	<b>Package and PCB thermal data</b>	<b>29</b>
4.1	PowerSSO-12 thermal data	29
4.2	PowerSSO-24 thermal data	31
<b>5</b>	<b>Package and packing information</b>	<b>35</b>
5.1	ECOPACK®	35
5.2	PowerSSO-12 package information	35
5.3	PowerSSO-24 package information	37
5.4	PowerSSO-12 packing information	39
5.5	PowerSSO-24 packing information	40
<b>6</b>	<b>Order codes</b>	<b>41</b>
<b>7</b>	<b>Revision history</b>	<b>42</b>

## List of tables

Table 1.	Pin function . . . . .	6
Table 2.	Suggested connections for unused and not connected pins . . . . .	7
Table 3.	Absolute maximum ratings . . . . .	8
Table 4.	Thermal data . . . . .	9
Table 5.	Power section . . . . .	9
Table 6.	Switching ( $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$ ) . . . . .	10
Table 7.	Logic inputs . . . . .	10
Table 8.	Protections and diagnostics . . . . .	11
Table 9.	Current sense ( $8 V < V_{CC} < 18 V$ ) . . . . .	11
Table 10.	Open load detection ( $8V < V_{CC} < 18V$ ) . . . . .	13
Table 11.	Truth table . . . . .	16
Table 12.	Electrical transient requirements (part 1) . . . . .	17
Table 13.	Electrical transient requirements (part 2) . . . . .	17
Table 14.	Electrical transient requirements (part 3) . . . . .	17
Table 15.	Thermal parameters . . . . .	31
Table 16.	Thermal parameters . . . . .	34
Table 17.	PowerSSO-12 mechanical data . . . . .	36
Table 18.	PowerSSO-24 mechanical data . . . . .	38
Table 19.	Device summary . . . . .	41
Table 20.	Document revision history . . . . .	42

## List of figures

Figure 1.	Block diagram . . . . .	6
Figure 2.	Configuration diagram (top view) . . . . .	7
Figure 3.	Current and voltage conventions . . . . .	8
Figure 4.	Current sense delay characteristics . . . . .	13
Figure 5.	Open load off-state delay timing . . . . .	13
Figure 6.	Switching characteristics . . . . .	14
Figure 7.	Delay response time between rising edge of output current and rising edge of current sense (CS enabled) . . . . .	14
Figure 8.	Output voltage drop limitation . . . . .	15
Figure 9.	$I_{OUT}/I_{SENSE}$ vs $I_{OUT}$ . . . . .	15
Figure 10.	Maximum current sense ratio drift vs load current . . . . .	16
Figure 11.	Normal operation . . . . .	18
Figure 12.	Overload or short to GND . . . . .	18
Figure 13.	Intermittent overload . . . . .	19
Figure 14.	Off-state open load with external circuitry . . . . .	19
Figure 15.	Short to $V_{CC}$ . . . . .	20
Figure 16.	$T_J$ evolution in overload or short to GND . . . . .	20
Figure 17.	Off-state output current . . . . .	21
Figure 18.	High level input current . . . . .	21
Figure 19.	Input clamp voltage . . . . .	21
Figure 20.	Input low level . . . . .	21
Figure 21.	Input high level . . . . .	21
Figure 22.	Input hysteresis voltage . . . . .	21
Figure 23.	On-state resistance vs $T_{case}$ . . . . .	22
Figure 24.	On-state resistance vs $V_{CC}$ . . . . .	22
Figure 25.	Undervoltage shutdown . . . . .	22
Figure 26.	Turn-on voltage slope . . . . .	22
Figure 27.	$I_{LIMH}$ vs $T_{case}$ . . . . .	22
Figure 28.	Turn-off voltage slope . . . . .	22
Figure 29.	CS_DIS high level voltage . . . . .	23
Figure 30.	CS_DIS clamp voltage . . . . .	23
Figure 31.	CS_DIS low level voltage . . . . .	23
Figure 32.	Application schematic . . . . .	24
Figure 33.	Current sense and diagnostic . . . . .	26
Figure 34.	Maximum turn-off current versus inductance (for each channel) . . . . .	28
Figure 35.	PowerSSO-12 PC board . . . . .	29
Figure 36.	$R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON) . . . . .	29
Figure 37.	PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON) . . . . .	30
Figure 38.	Thermal fitting model of a double channel HSD in PowerSSO-12 . . . . .	30
Figure 39.	PowerSSO-24 PC board . . . . .	31
Figure 40.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON) . . . . .	32
Figure 41.	PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON) . . . . .	33
Figure 42.	Thermal fitting model of a double channel HSD in PowerSSO-24 . . . . .	33
Figure 43.	PowerSSO-12 package dimensions . . . . .	35
Figure 44.	PowerSSO-24 package dimensions . . . . .	37
Figure 45.	PowerSSO-12 tube shipment (no suffix) . . . . .	39
Figure 46.	PowerSSO-12 tape and reel shipment (suffix "TR") . . . . .	39
Figure 47.	PowerSSO-24 tube shipment (no suffix) . . . . .	40

Figure 48. PowerSSO-24 tape and reel shipment (suffix “TR”) . . . . . 40

# 1 Block diagram and pin description

Figure 1. Block diagram

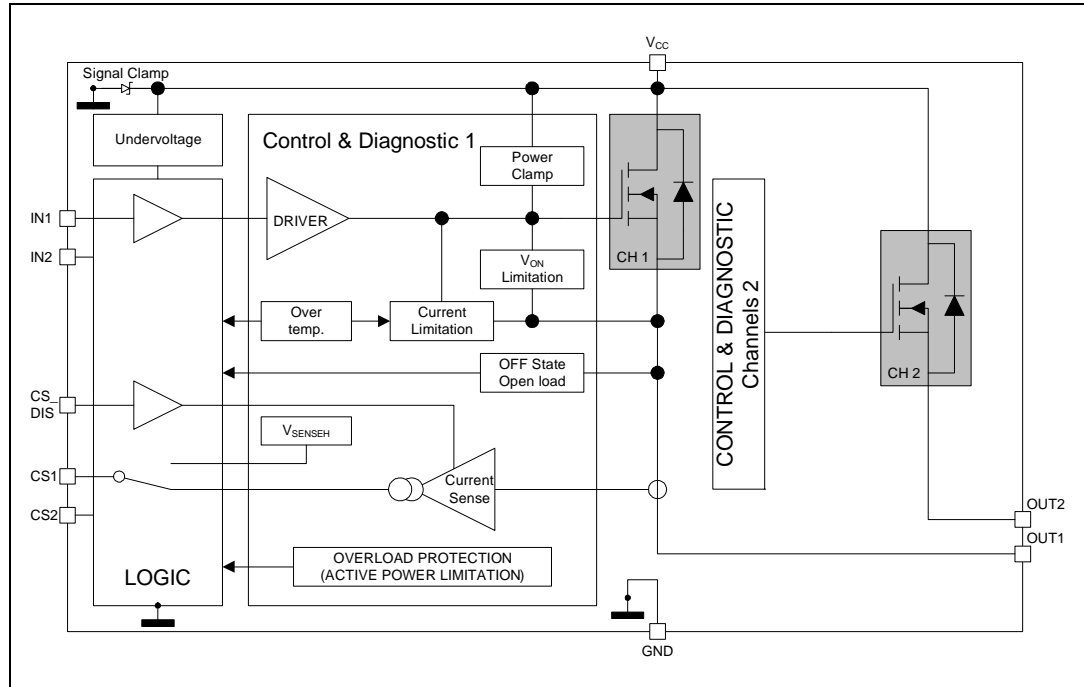


Table 1. Pin function

Name	Function
V <sub>CC</sub>	Battery connection.
OUTPUT <sub>1,2</sub>	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT <sub>1,2</sub>	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE <sub>1,2</sub>	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

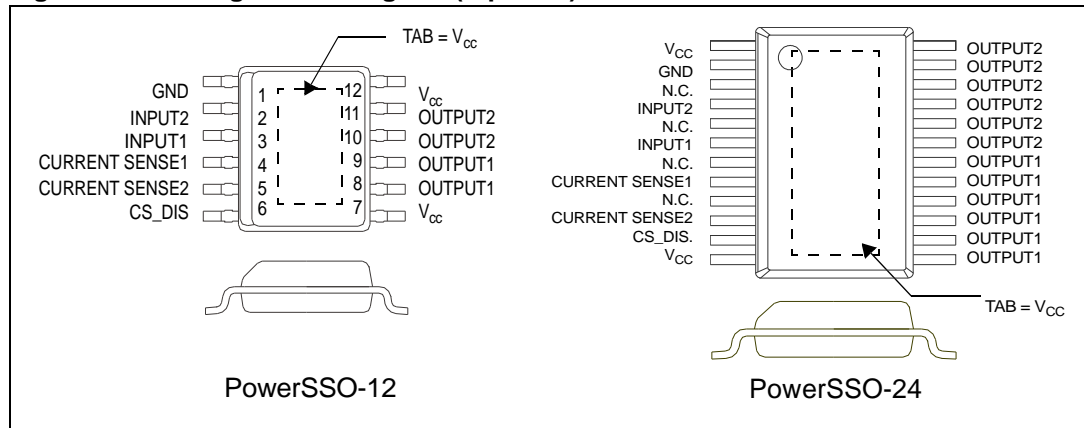
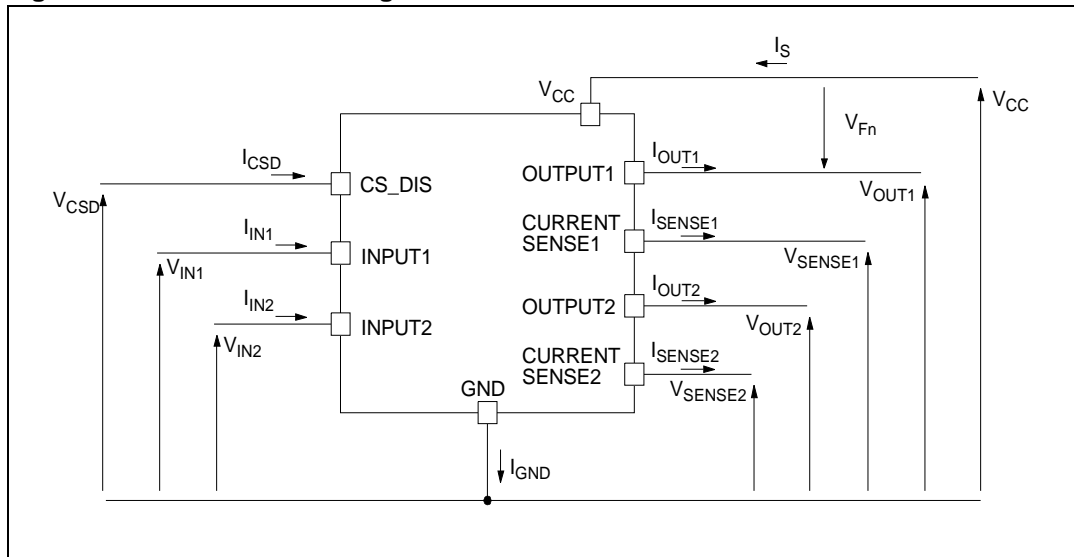


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Through 22 KΩ resistor	Through 10 KΩ resistor	Through 10 KΩ resistor

## 2 Electrical specifications

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in the table for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CSD}$	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
$V_{CSENSE}$	Current sense maximum voltage	$V_{CC} - 41$ to $+V_{CC}$	V



**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
$E_{MAX}$	Maximum switching energy (single pulse) ( $L = 3\text{mH}$ ; $R_L = 0\Omega$ ; $V_{bat} = 13.5\text{V}$ ; $T_{jstart} = 150^\circ\text{C}$ ; $I_{OUT}$ )	104	mJ
$V_{ESD}$	Electrostatic discharge (human body model: $R = 1.5\text{K}\Omega$ ; $C = 100\text{pF}$ )		
	– Input	4000	V
	– Current sense	2000	V
	– CS_DIS	4000	V
	– Output	5000	V
	– $V_{CC}$	5000	V
$V_{ESD}$	Charge device model (CDM-AEC-Q100-011)	750	V
$T_j$	Junction operating temperature	-40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Max value		Unit
		PowerSSO-12	PowerSSO-24	
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	2.7	2.7	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	See <a href="#">Figure 36</a>	See <a href="#">Figure 40</a>	$^\circ\text{C}/\text{W}$

## 2.3 Electrical characteristics

Values specified in this section are for  $8\text{ V} < V_{CC} < 28\text{ V}$ ;  $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$ , unless otherwise stated.

**Table 5. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	28	V
$V_{USD}$	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
$R_{ON}$	On-state resistance <sup>(1)</sup>	$I_{OUT} = 2\text{ A}$ ; $T_j = 25^\circ\text{C}$			50	m $\Omega$
		$I_{OUT} = 2\text{ A}$ ; $T_j = 150^\circ\text{C}$			100	
		$I_{OUT} = 2\text{ A}$ ; $V_{CC} = 5\text{ V}$ ; $T_j = 25^\circ\text{C}$			65	
$V_{clamp}$	Clamp voltage	$I_S = 20\text{ mA}$	41	46	52	V

**Table 5. Power section (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_S$	Supply current	Off-state; $V_{CC} = 13\text{ V}$ ; $T_j = 25^\circ\text{C}$ ; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$		2 <sup>(2)</sup>	5 <sup>(2)</sup>	$\mu\text{A}$
		On-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = 5\text{ V}$ ; $I_{OUT} = 0\text{ A}$		3	6	$\text{mA}$
$I_{L(off1)}$	Off-state output current (1)	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 25^\circ\text{C}$	0	0.01	3	$\mu\text{A}$
		$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125^\circ\text{C}$	0		5	
$V_F$	Output - $V_{CC}$ diode voltage <sup>(1)</sup>	$-I_{OUT} = 4\text{ A}$ ; $T_j = 150^\circ\text{C}$			0.7	$\text{V}$

1. For each channel.

2. PowerMOS leakage included.

**Table 6. Switching ( $V_{CC} = 13\text{V}$ ;  $T_j = 25^\circ\text{C}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> )	—	20	—	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> )	—	45	—	$\mu\text{s}$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5\ \Omega$	—	See <a href="#">Figure 26</a>	—	$\text{V}/\mu\text{s}$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5\ \Omega$	—	See <a href="#">Figure 28</a>	—	$\text{V}/\mu\text{s}$
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> )	—	0.15	—	$\text{mJ}$
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L = 6.5\ \Omega$ (see <a href="#">Figure 6</a> )	—	0.3	—	$\text{mJ}$

**Table 7. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.9	$\text{V}$
$I_{IL}$	Low level input current	$V_{IN} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level voltage		2.1			$\text{V}$
$I_{IH}$	High level input current	$V_{IN} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			$\text{V}$
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	$\text{V}$
		$I_{IN} = -1\text{ mA}$		-0.7		
$V_{CSDL}$	CS_DIS low level voltage				0.9	$\text{V}$
$I_{CSDL}$	Low level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{CSDH}$	CS_DIS high level voltage		2.1			$\text{V}$

**Table 7. Logic inputs (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{CSDH}$	High level CS_DIS current	$V_{CSD} = 2.1 \text{ V}$			10	$\mu\text{A}$
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
$V_{CSCL}$	CS_DIS clamp voltage	$I_{CSD} = 1 \text{ mA}$	5.5		7	V
		$I_{CSD} = -1 \text{ mA}$		-0.7		

**Table 8. Protections and diagnostics (1)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC short circuit current	$V_{CC} = 13 \text{ V}$	19	27	38	A
		$5 \text{ V} < V_{CC} < 28 \text{ V}$			38	A
$I_{limL}$	Short circuit current during thermal cycling	$V_{CC} = 13 \text{ V};$ $T_R < T_j < T_{TSD}$		7		A
$T_{TSD}$	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
$T_R$	Reset temperature		$T_{RS}+1$	$T_{RS}+5$		$^{\circ}\text{C}$
$T_{RS}$	Thermal reset of status		135			$^{\circ}\text{C}$
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		$^{\circ}\text{C}$
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT} = 2 \text{ A}; V_{IN} = 0;$ $L = 6 \text{ mH}$	$V_{CC}-41$	$V_{CC}-46$	$V_{CC}-52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 0.1 \text{ A};$ $T_j = -40^{\circ}\text{C} \dots +150^{\circ}\text{C}$ (see <a href="#">Figure 8</a> )		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 9. Current sense (8 V <  $V_{CC}$  < 18 V)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_0$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 0.05 \text{ A};$ $V_{SENSE} = 0.5 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = -40^{\circ}\text{C} \dots 150^{\circ}\text{C}$	1440	2250	3630	
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 1 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = -40^{\circ}\text{C} \dots 150^{\circ}\text{C}$	1740	2070	2820	
		$T_j = 25^{\circ}\text{C} \dots 150^{\circ}\text{C}$	1750	2070	2562	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 1 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	-15		15	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 2 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = -40^{\circ}\text{C} \dots 150^{\circ}\text{C}$	1900	2000	2395	
		$T_j = 25^{\circ}\text{C} \dots 150^{\circ}\text{C}$	1899	2000	2282	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 2 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	-9		9	%

Table 9. Current sense (8 V < V<sub>CC</sub> < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 4 A; V <sub>SENSE</sub> = 4 V; V <sub>CSD</sub> = 0 V; T <sub>J</sub> = -40°C...150°C T <sub>J</sub> = 25°C...150°C	1969 1950	1990 1990	2210 2153	
dK <sub>3</sub> /K <sub>3</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 4 A; V <sub>SENSE</sub> = 4 V; V <sub>CSD</sub> = 0 V; T <sub>J</sub> = -40 °C to 150 °C	-6		6	%
I <sub>SENSE0</sub>	Analog sense leakage current	I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 5 V; V <sub>IN</sub> = 0 V; T <sub>J</sub> = -40°C...150°C	0		1	μA
		I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 0 V; V <sub>IN</sub> = 5 V; T <sub>J</sub> = -40°C...150°C	0		2	
		I <sub>OUT</sub> = 2 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 5 V; V <sub>IN</sub> = 5 V; T <sub>J</sub> = -40°C...150°C	0		1	
I <sub>OL</sub>	Open load on-state current detection threshold	V <sub>IN</sub> = 5 V; 8 V < V <sub>CC</sub> < 18 V; I <sub>SENSE</sub> = 5 μA	4		20	mA
V <sub>SENSE</sub>	Max analog sense output voltage	I <sub>OUT</sub> = 4 A; V <sub>CSD</sub> = 0 V	5			V
V <sub>SENSEH</sub>	Analog sense output voltage in fault condition <sup>(2)</sup>	V <sub>CC</sub> = 13 V; R <sub>SENSE</sub> = 3.9 KΩ		8		V
I <sub>SENSEH</sub>	Analog sense output current in fault condition <sup>(2)</sup>	V <sub>CC</sub> = 13 V; V <sub>SENSE</sub> = 5 V		9		mA
t <sub>DSENSE1H</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )		40	100	μs
t <sub>DSENSE1L</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )		5	20	μs
t <sub>DSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )		80	250	μs
Δt <sub>DSENSE2H</sub>	Delay response time between rising edge of output current and rising edge of current sense	V <sub>SENSE</sub> < 4V; I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> , I <sub>OUT</sub> = 90% of I <sub>OUTMAX</sub> I <sub>OUTMAX</sub> = 2A (see <a href="#">Figure 7</a> )			40	μs
t <sub>DSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> < 4 V; 0.5 A < I <sub>OUT</sub> < 4 A; I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see <a href="#">Figure 4</a> )		80	250	μs

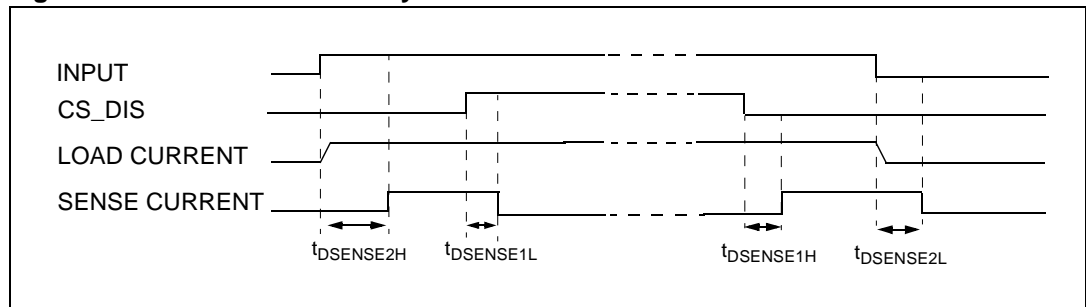
1. Parameter guaranteed by design; it is not tested.

2. Fault condition includes: power limitation, over temperature and open load off-state detection.

**Table 10. Open load detection ( $8V < V_{CC} < 18V$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OL}$	Open load off-state voltage detection threshold	$V_{IN} = 0 V$	2	See <a href="#">Figure 5</a>	4	V
$t_{DSTKON}$	Output short circuit to $V_{CC}$ detection delay at turn-off	See <a href="#">Figure 5</a>	180		1200	$\mu s$
$I_{L(off2)r}$	Off-state output current at $V_{OUT} = 4V$	$V_{IN} = 0 V$ ; $V_{SENSE} = 0 V$ ; $V_{OUT}$ rising from 0 V to 4 V	-120		0	$\mu A$
$I_{L(off2)f}$	Off-state output current at $V_{OUT} = 2V$	$V_{IN} = 0 V$ ; $V_{SENSE} = V_{SENSEH}$ ; $V_{OUT}$ falling from $V_{CC}$ to 2 V	-50		90	$\mu A$
$td\_vol$	Delay response from output rising edge to $V_{SENSE}$ rising edge in open load	$V_{OUT} = 4 V$ ; $V_{IN} = 0 V$ ; $V_{SENSE} = 90\%$ of $V_{SENSEH}$			20	$\mu s$

**Figure 4. Current sense delay characteristics**



**Figure 5. Open load off-state delay timing**

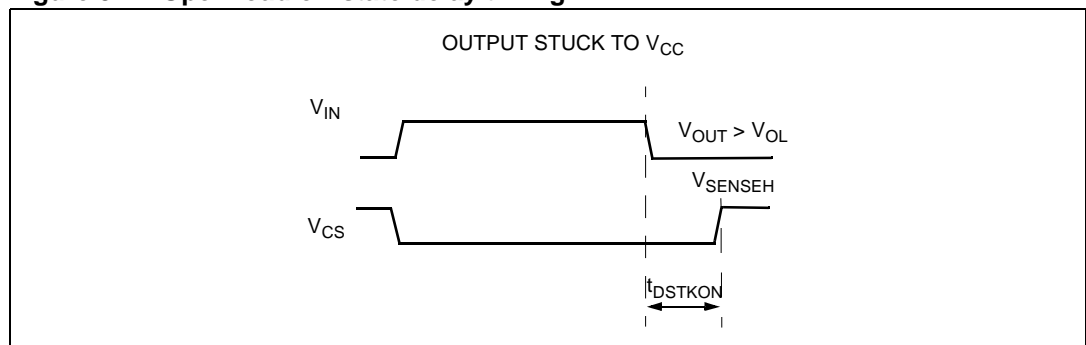


Figure 6. Switching characteristics

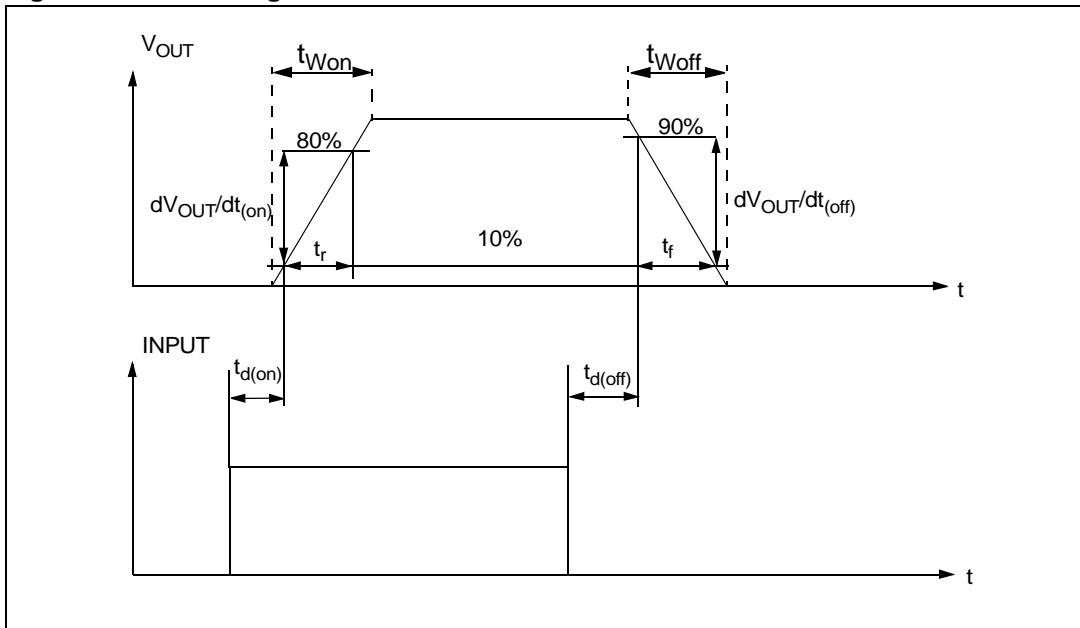


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

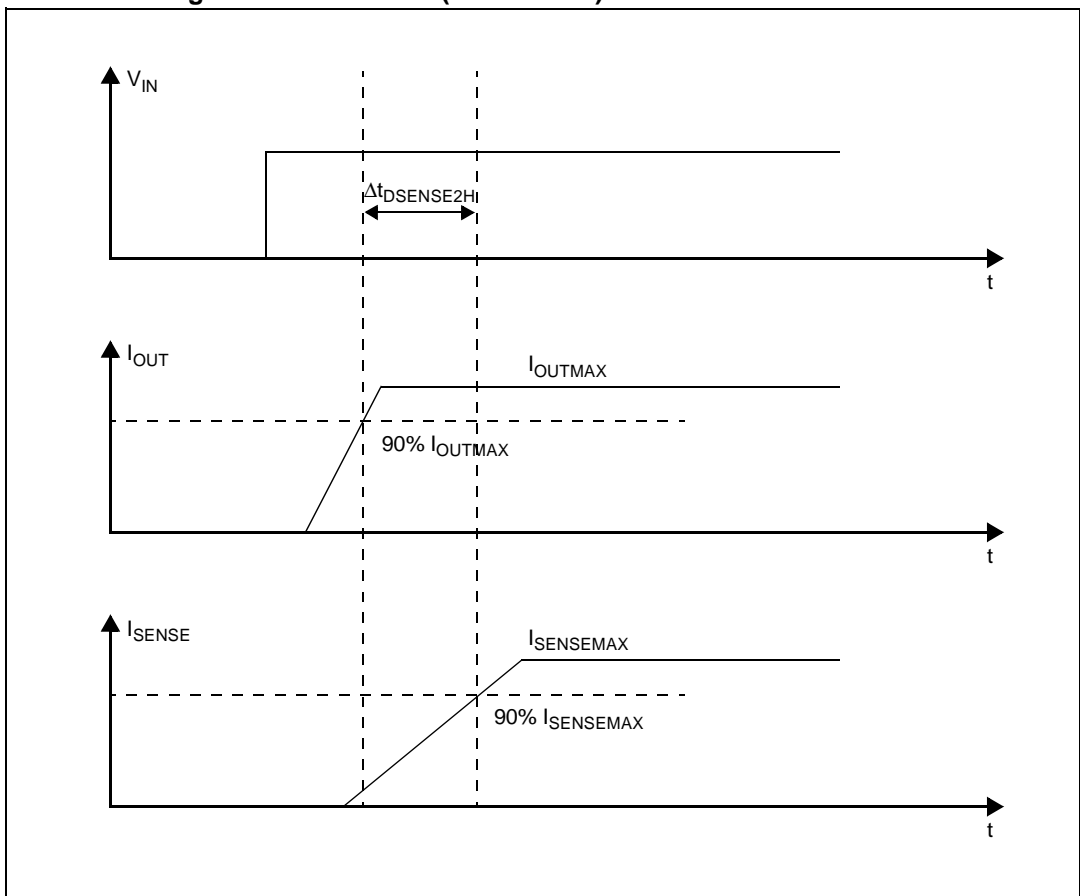


Figure 8. Output voltage drop limitation

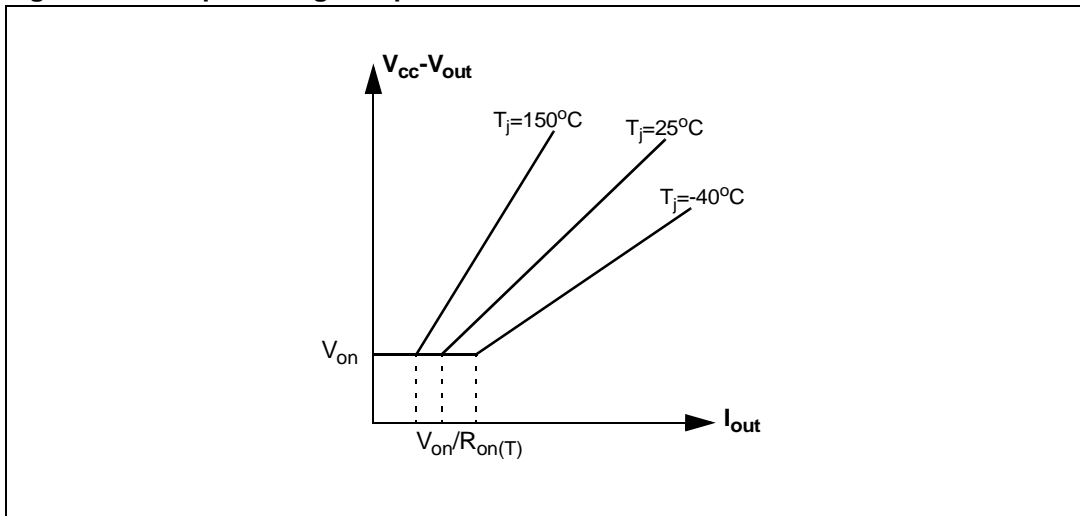


Figure 9.  $I_{out} / I_{sense}$  vs  $I_{out}$

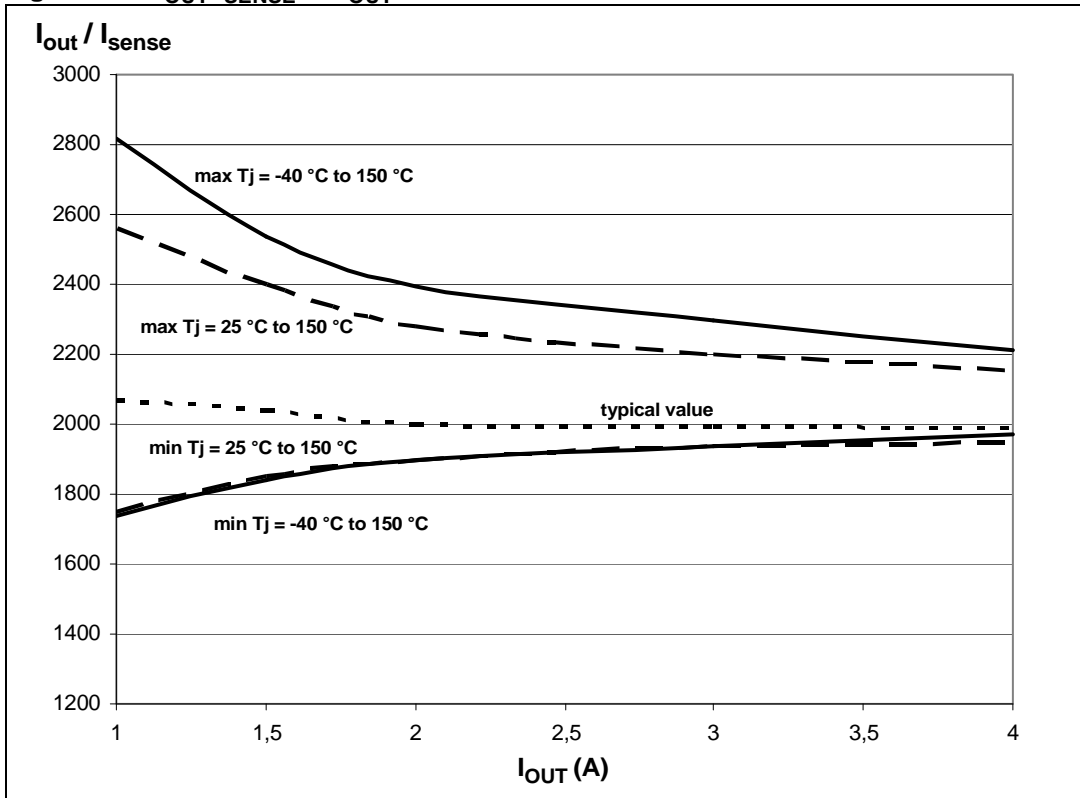
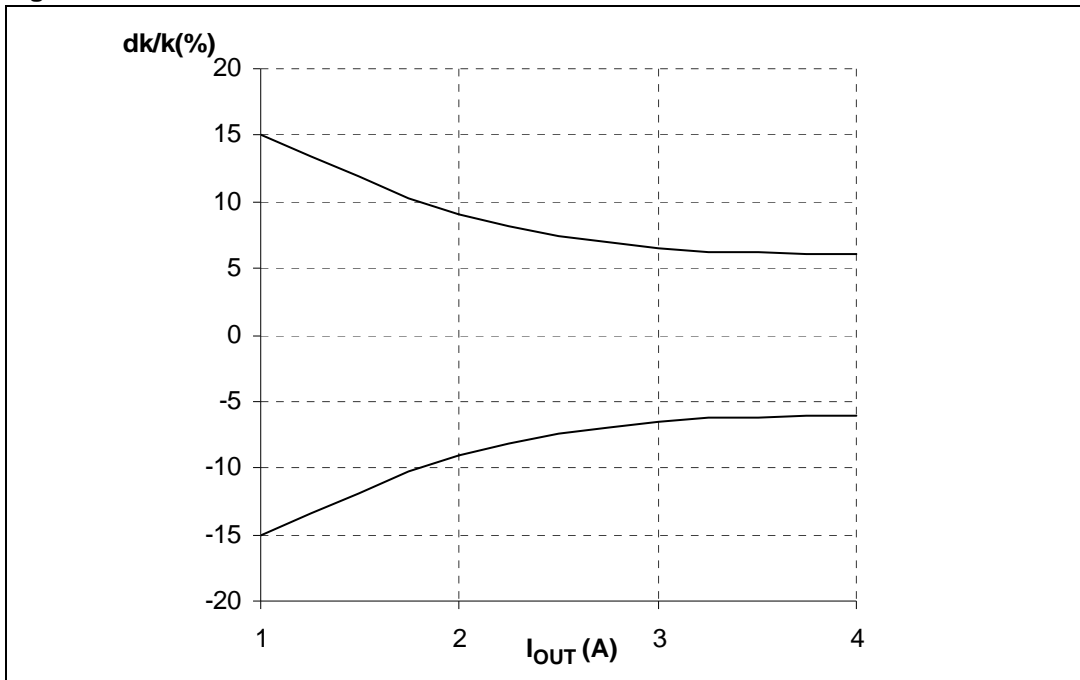


Figure 10. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense ( $V_{CSD} = 0\text{ V}$ ) <sup>(1)</sup>
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	$V_{SENSEH}$
Short circuit to GND (power limitation)	L	L	0
	H	L	$V_{SENSEH}$
Open load off-state (with external pull-up)	L	H	$V_{SENSEH}$
Short circuit to $V_{CC}$ (external pull-up disconnected)	L	H	$V_{SENSEH}$
	H	H	$V_{SENSEH}$ < Nominal
Negative output voltage clamp	L	L	0

1. If the  $V_{CSD}$  is high, the SENSE output is at high impedance; its potential depends on leakage currents and external circuits.



Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) test pulse	Test levels <sup>(1)</sup>		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b <sup>(2)</sup>	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to  $V_{CC} = 13.5V$  except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004E test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b <sup>(1)</sup>	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

## 2.4 Waveforms

Figure 11. Normal operation

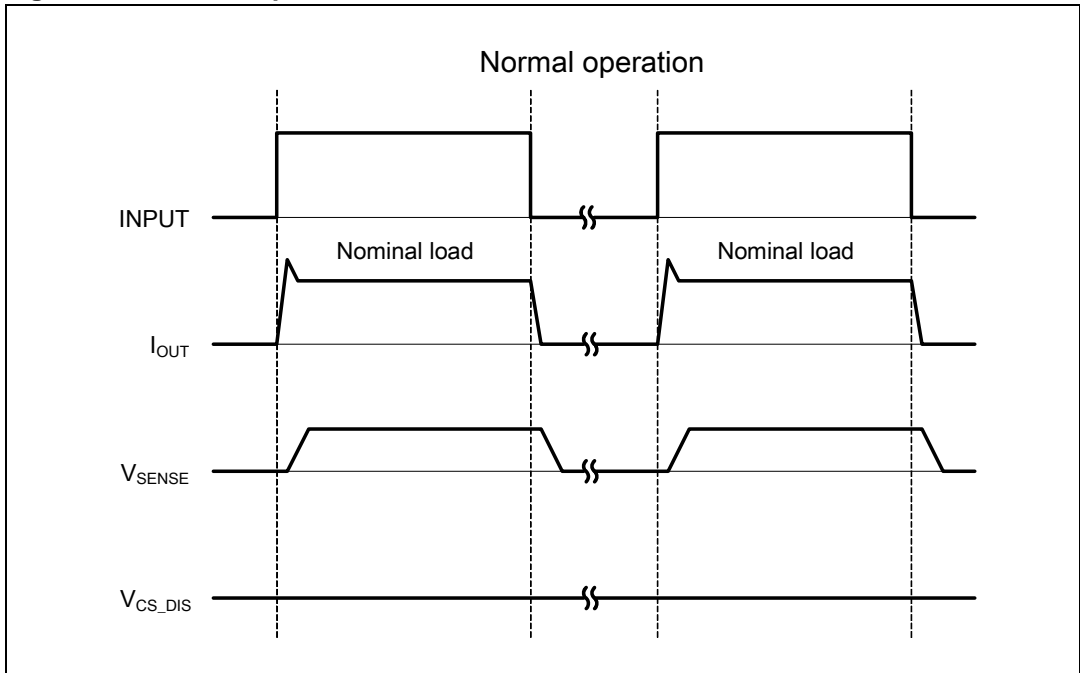


Figure 12. Overload or short to GND

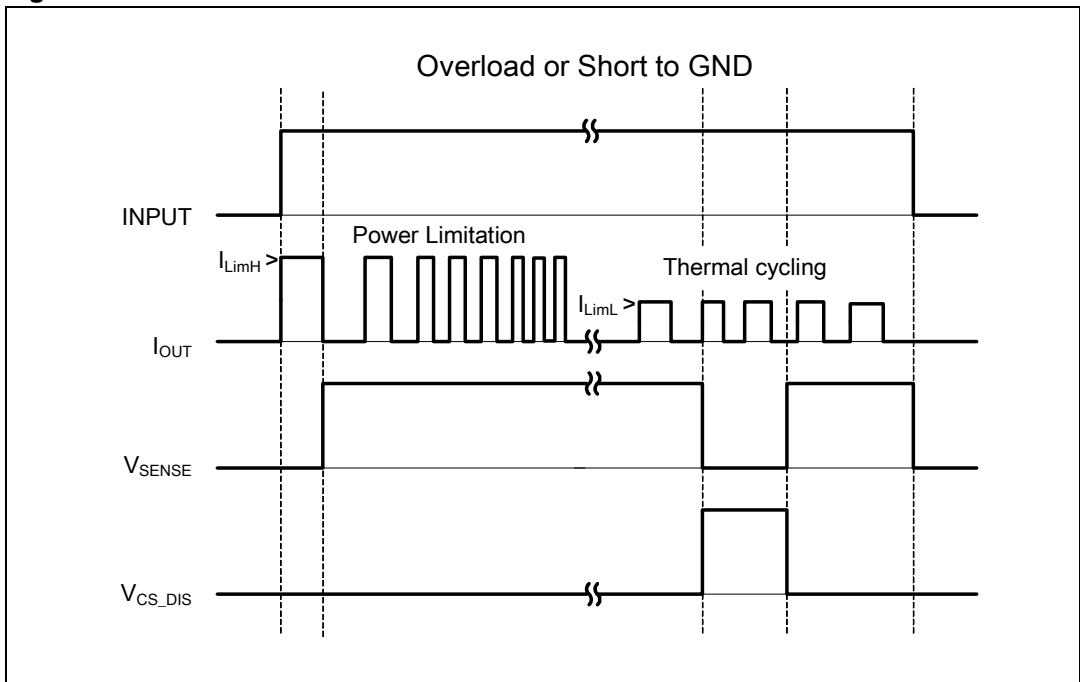


Figure 13. Intermittent overload



Figure 14. Off-state open load with external circuitry

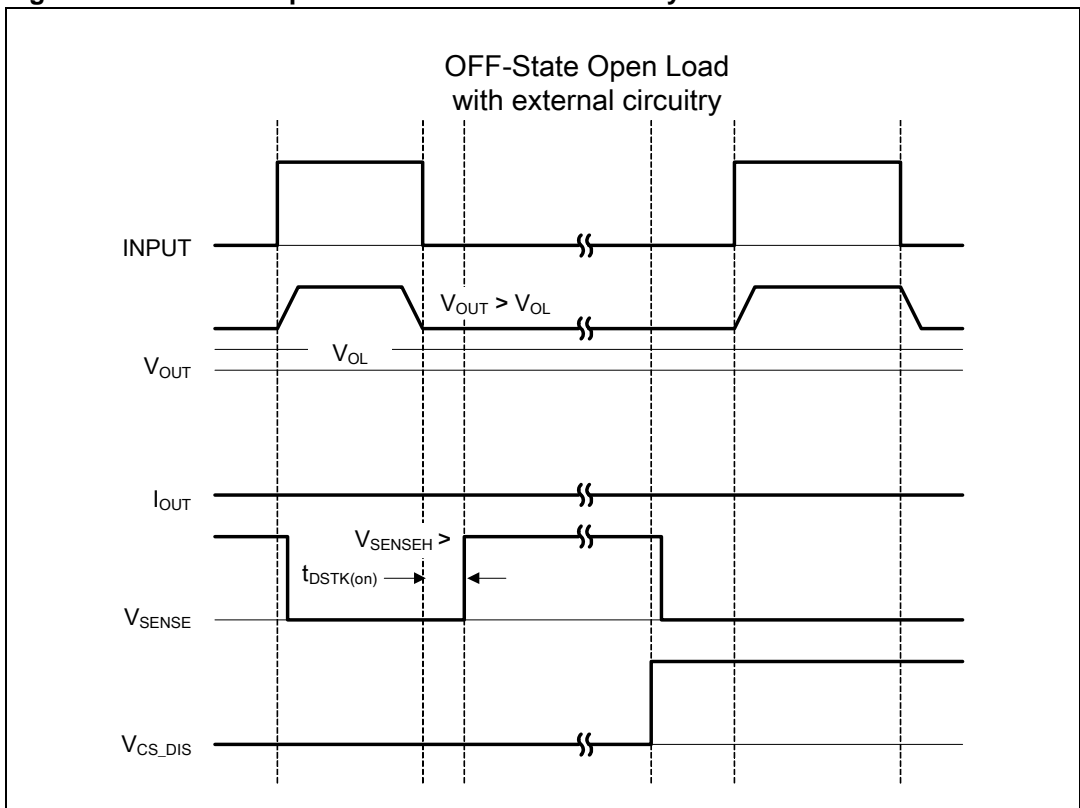


Figure 15. Short to  $V_{CC}$



Figure 16.  $T_J$  evolution in overload or short to GND



## 2.5 Electrical characteristics curves

Figure 17. Off-state output current

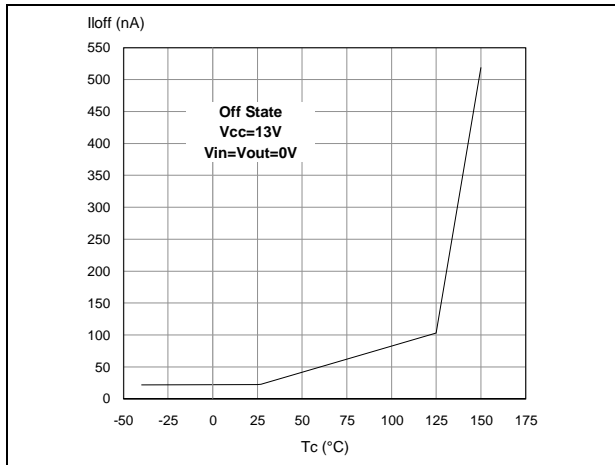


Figure 18. High level input current

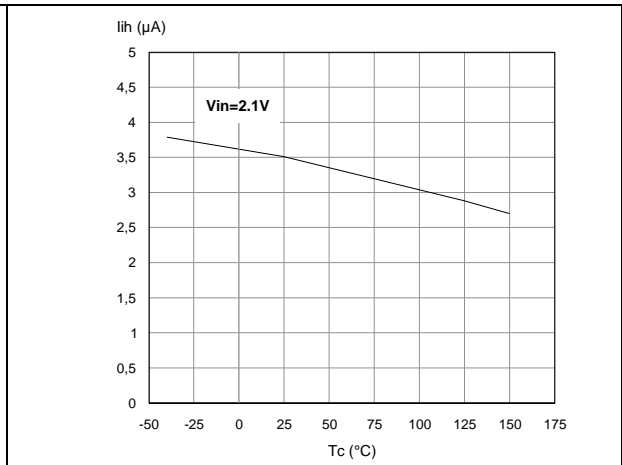


Figure 19. Input clamp voltage

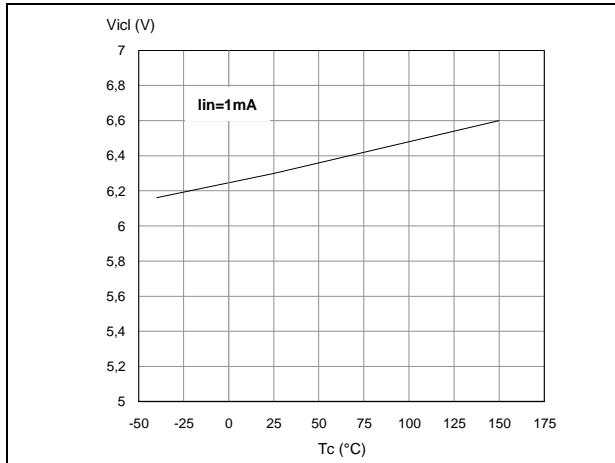


Figure 20. Input low level

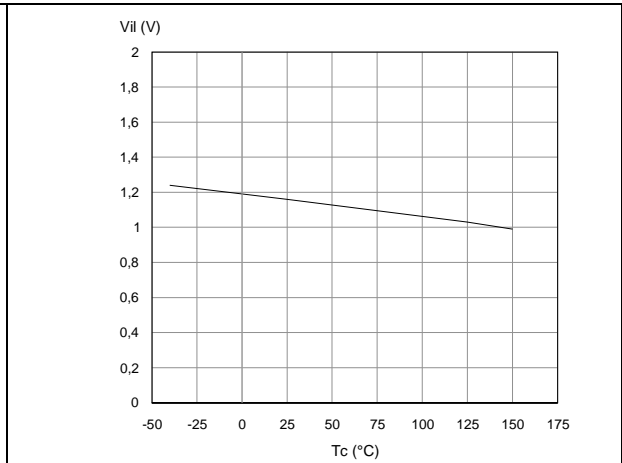


Figure 21. Input high level

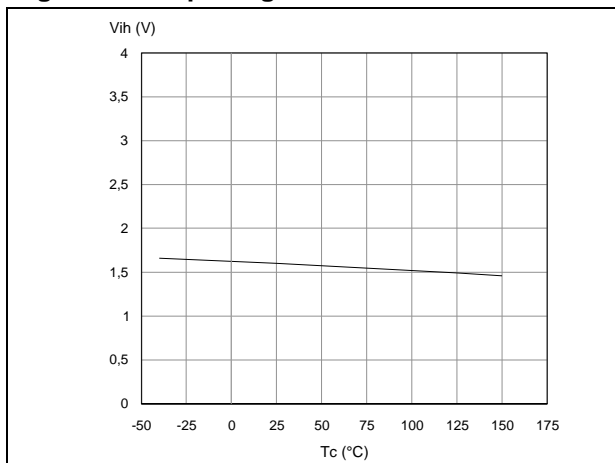


Figure 22. Input hysteresis voltage

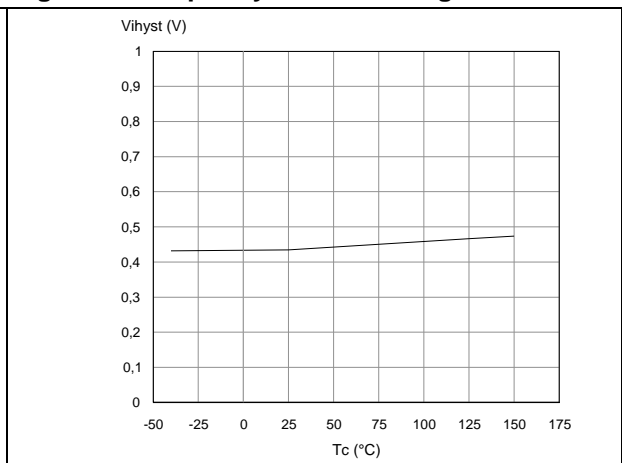


Figure 23. On-state resistance vs  $T_{case}$



Figure 24. On-state resistance vs  $V_{CC}$

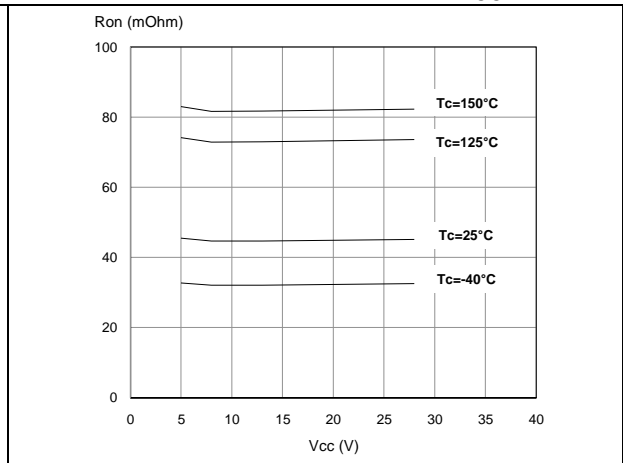


Figure 25. Undervoltage shutdown

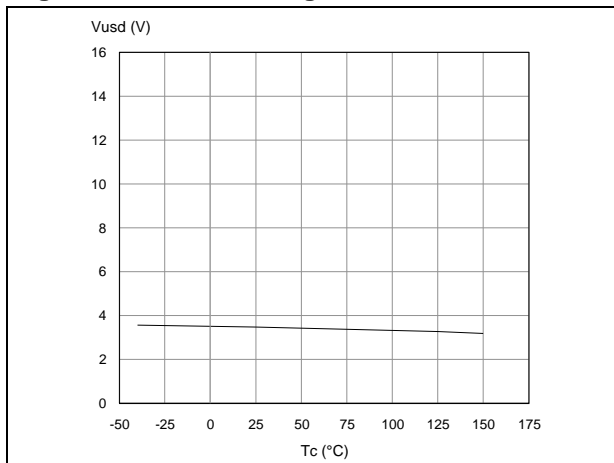


Figure 26. Turn-on voltage slope

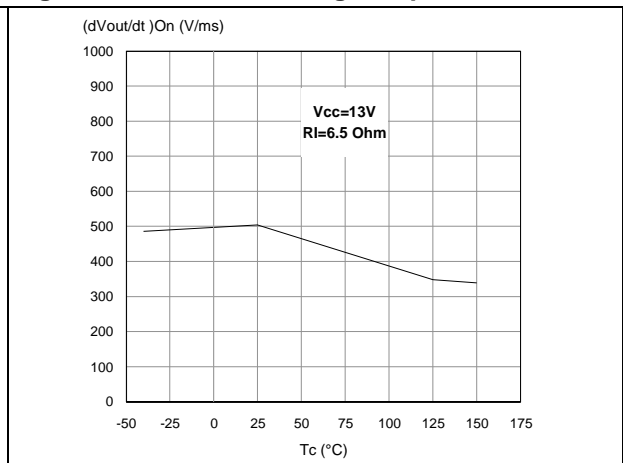


Figure 27.  $I_{LIMH}$  vs  $T_{case}$

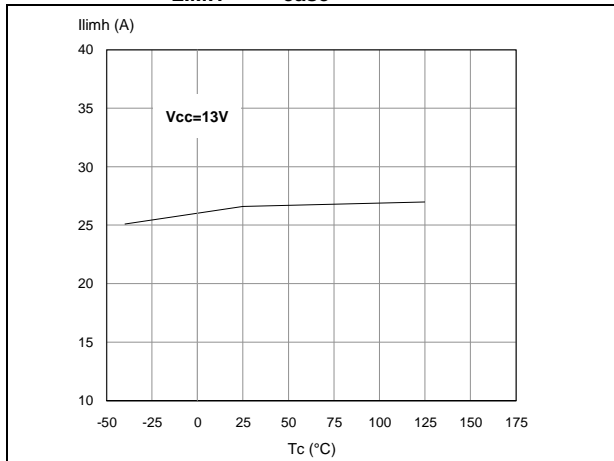
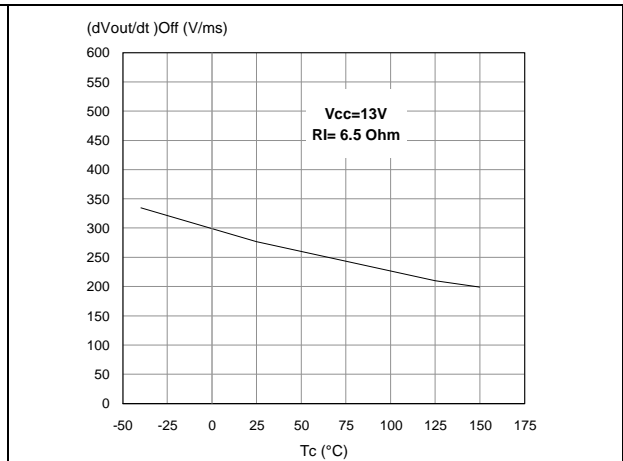
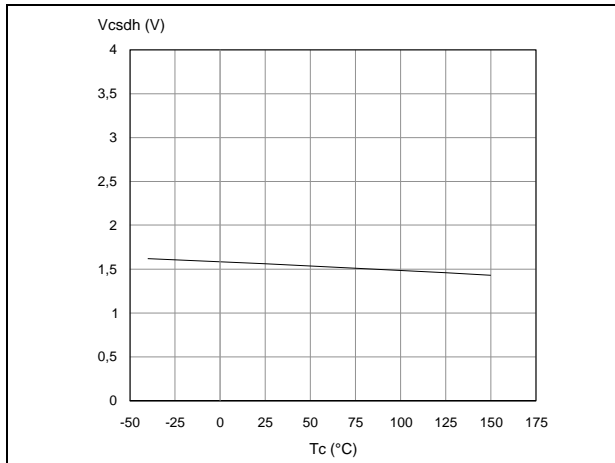


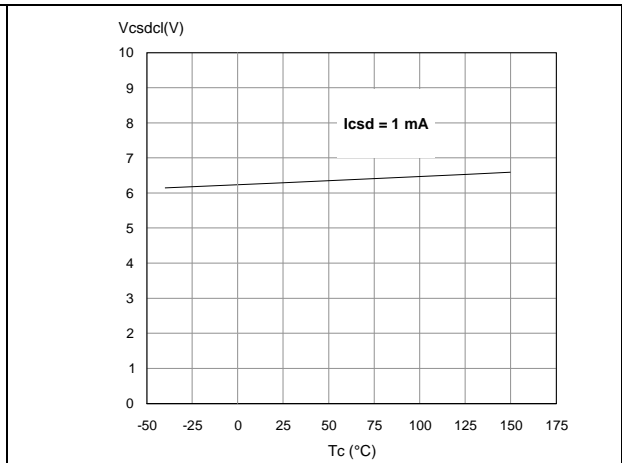
Figure 28. Turn-off voltage slope



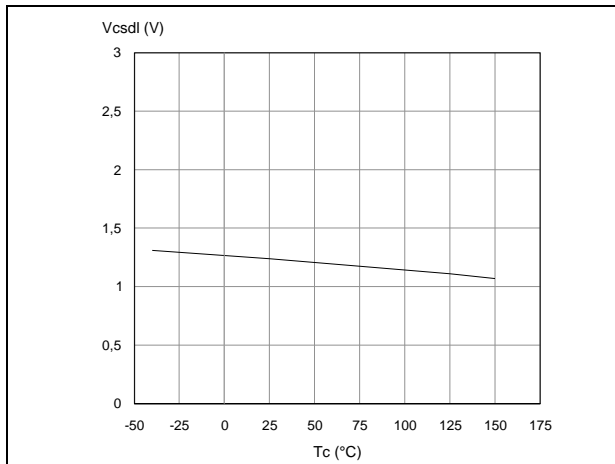
**Figure 29. CS\_DIS high level voltage**



**Figure 30. CS\_DIS clamp voltage**

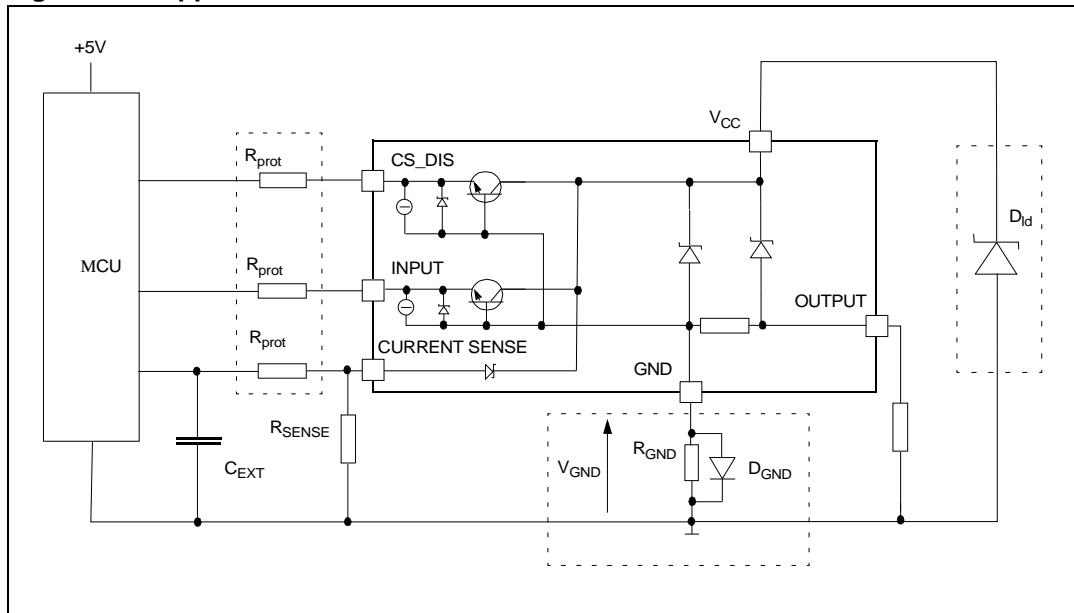


**Figure 31. CS\_DIS low level voltage**



### 3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1: resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following is an indication on how to resize the R<sub>GND</sub> resistor.

1.  $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R<sub>GND</sub> (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R<sub>GND</sub> produces a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift varies depending on how many devices are on in case of several high side drivers sharing the same R<sub>GND</sub>.



If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize [Section 3.1.2: Solution 2: diode \(DGND\) in the ground line](#).

### 3.1.2 Solution 2: diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ( $\approx 600\text{mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins are pulled negative.

ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -100\text{V}$  and  $I_{latchup} \geq 20\text{mA}$ ;  $V_{OH\mu C} \geq 4.5\text{V}$

$$5\text{k}\Omega \leq R_{prot} \leq 180\text{k}\Omega$$

Recommended values:  $R_{prot} = 10\text{k}\Omega$ ,  $C_{EXT} = 10\text{nF}$ .

## 3.4 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 33: Current sense and diagnostic](#)):

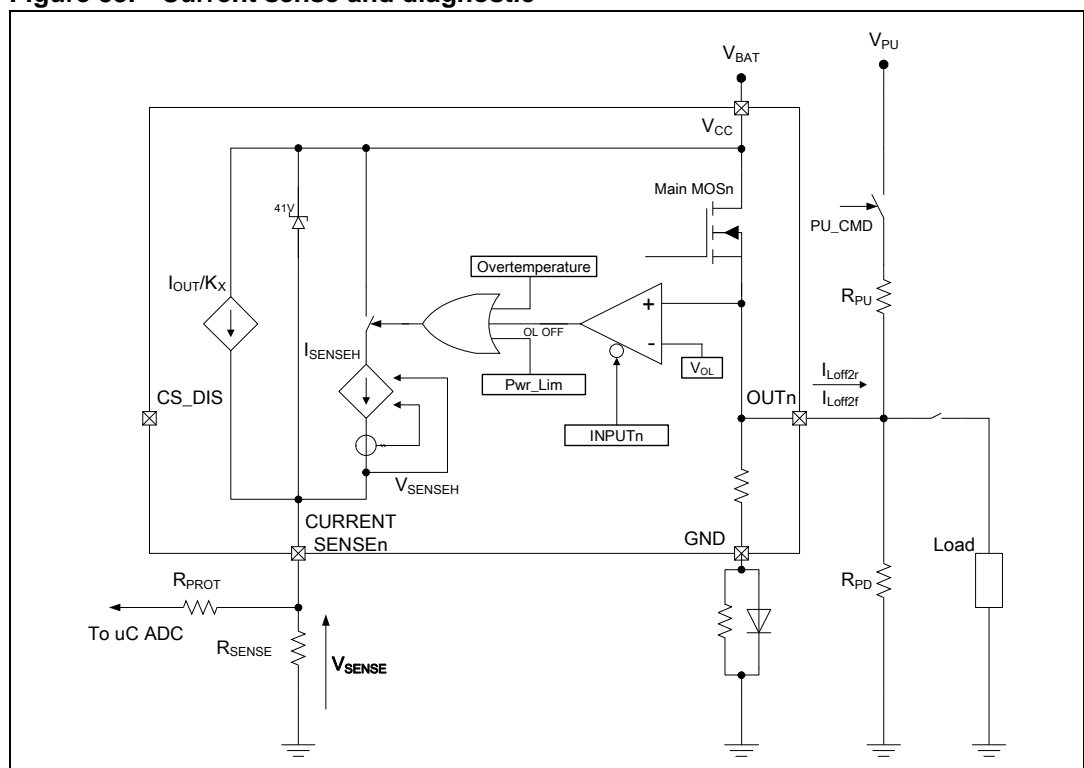
- **Current mirror of the load current in normal operation**, delivering a current proportional to the load current according to a known ratio  $K_X$ .  
The current  $I_{SENSE}$  can be easily converted to a voltage  $V_{SENSE}$  by means of an external resistor  $R_{SENSE}$ . Linearity between  $I_{OUT}$  and  $V_{SENSE}$  is ensured up to 5V minimum (see parameter  $V_{SENSE}$  in [Table 9: Current sense \(8 V <  \$V\_{CC}\$  < 18 V\)](#)). The current sense accuracy depends on the output current (refer to current sense electrical

characteristics [Table 9: Current sense \(8 V < V<sub>CC</sub> < 18 V\)](#)).

- **Diagnostic flag in fault conditions**, delivering a fixed voltage V<sub>SENSEH</sub> up to a maximum current I<sub>SENSEH</sub> in case of the following fault conditions (refer to [Table 11: Truth table](#)):
  - Power limitation activation
  - Overtemperature
  - Short to V<sub>CC</sub> in off-state
  - Open-load in off-state with additional external components.

A logic level high on the CS\_DIS pin simultaneously sets all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing the sense resistance and ADC line among different devices.

**Figure 33. Current sense and diagnostic**



### 3.4.1 Short to V<sub>CC</sub> and off-state open-load detection

#### Short to V<sub>CC</sub>

A short circuit between V<sub>CC</sub> and output is indicated by the relevant current sense pin set to V<sub>SENSEH</sub> during the device off-state. Little or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

#### Off-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor (R<sub>PU</sub>) connecting the output to a positive supply voltage (V<sub>PU</sub>).

It is preferable that  $V_{PU}$  is switched off during the module standby mode to avoid an increase in overall standby current consumption in normal conditions, that is, when the load is connected.

An external pull-down resistor ( $R_{PD}$ ) connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see [Figure 33: Current sense and diagnostic](#)).

$R_{PD}$  must be selected in order to ensure  $V_{OUT} < V_{OLmin}$  unless pulled up by the external circuitry:

$$V_{OUT}|_{Pull-up\_OFF} = R_{PD} \cdot I_{L(off)2f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22 \text{ K}\Omega$  is recommended.

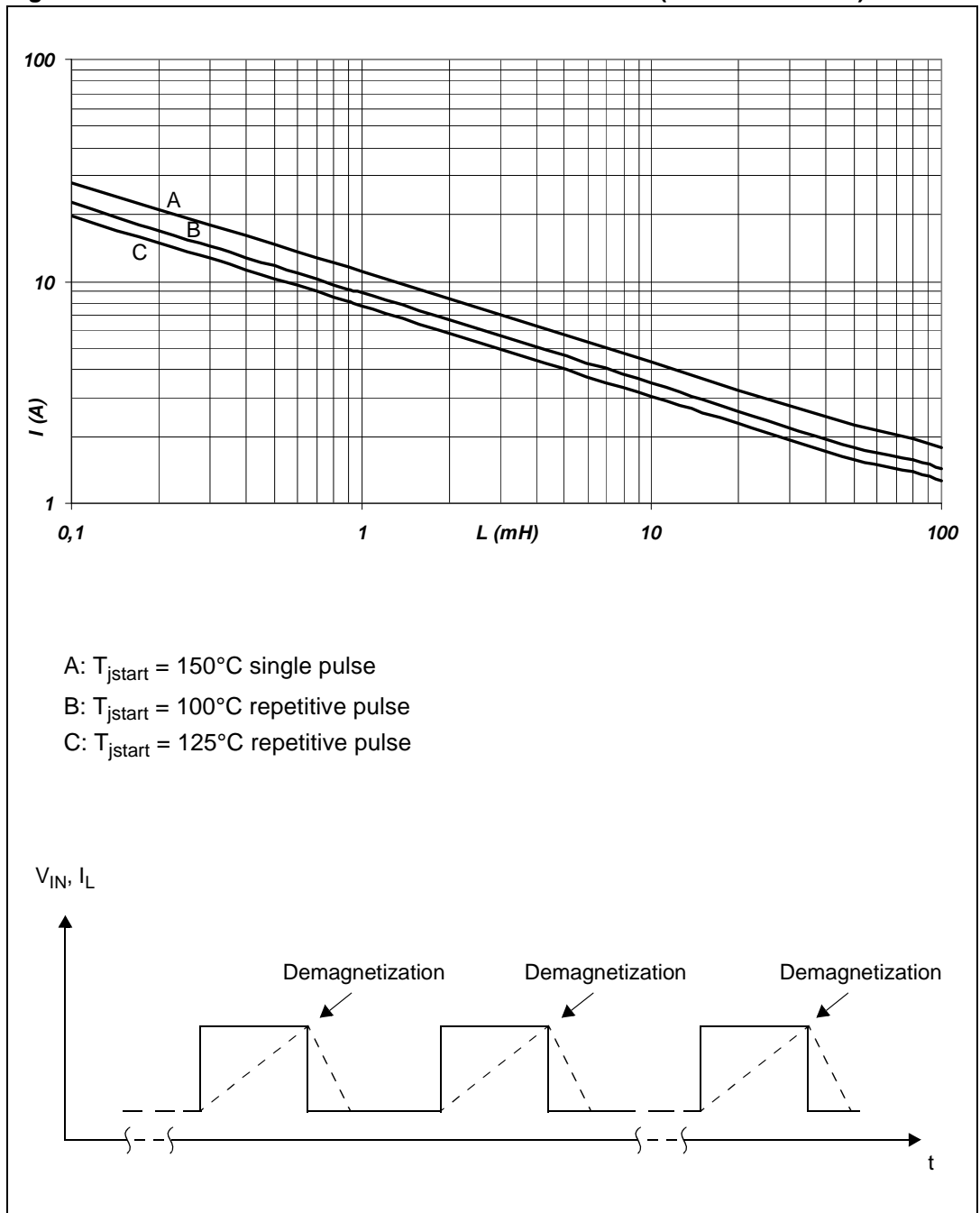
For proper open load detection in off-state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}|_{Pull-up\_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off)2r}}{R_{PU} + R_{PD}} > V_{OLmax} = 4V$$

For the values of  $V_{OLmin}$ ,  $V_{OLmax}$ ,  $I_{L(off)2r}$  and  $I_{L(off)2f}$  see [Table 10: Open load detection \( \$8V < V\_{CC} < 18V\$ \)](#).

### 3.5 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 34. Maximum turn-off current versus inductance (for each channel)

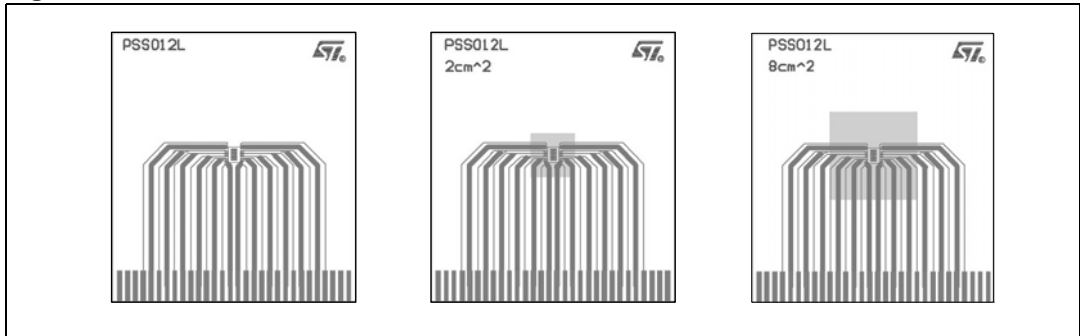


Note: Values are generated with  $R_L = 0 \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

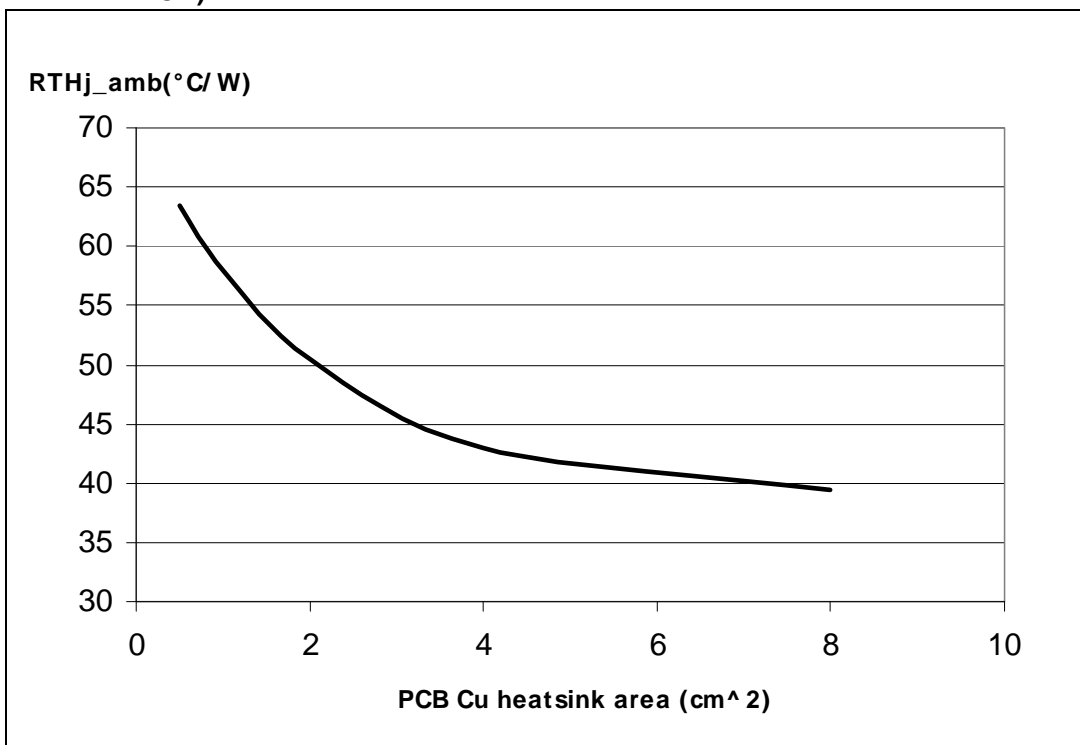
### 4.1 PowerSSO-12 thermal data

Figure 35. PowerSSO-12 PC board

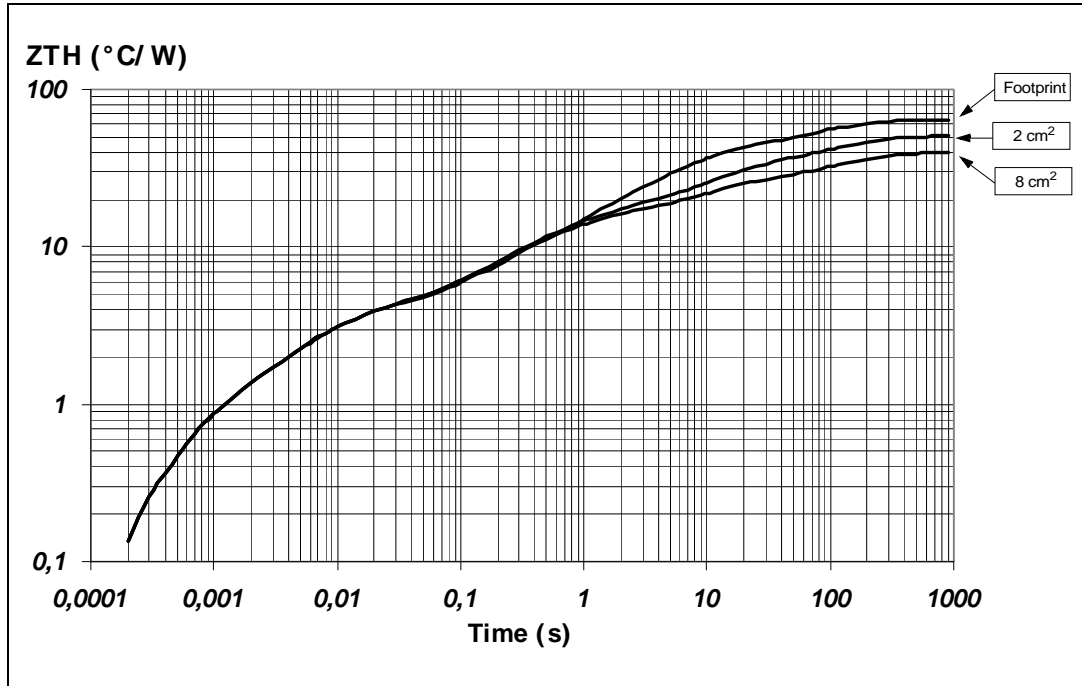


Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 $\mu$ m (front and back side), copper areas: from minimum pad lay-out to 8cm<sup>2</sup>).

Figure 36.  $R_{thj-amb}$  Vs. PCB copper area in open box free air condition (one channel ON)



**Figure 37. PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON)**

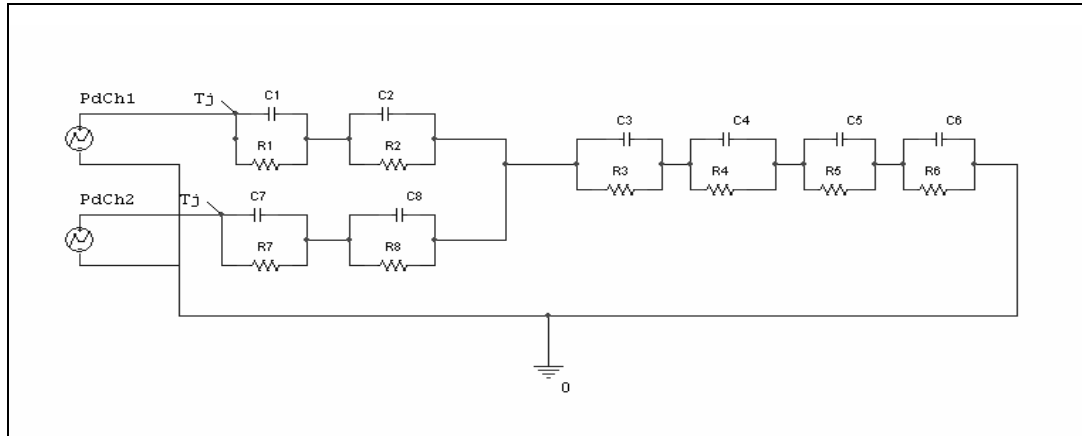


**Equation 1: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

**Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-12**



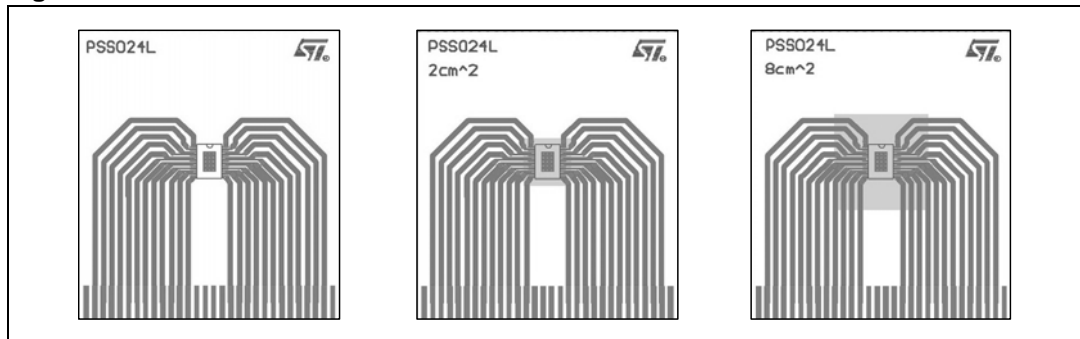
1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1=R7 (°C/W)	0.7		
R2=R8 (°C/W)	2.8		
R3 (°C/W)	4		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

## 4.2 PowerSSO-24 thermal data

Figure 39. PowerSSO-24 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 $\mu$ m (front and back side), copper areas: from minimum pad lay-out to 8cm<sup>2</sup>).

Figure 40.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel ON)

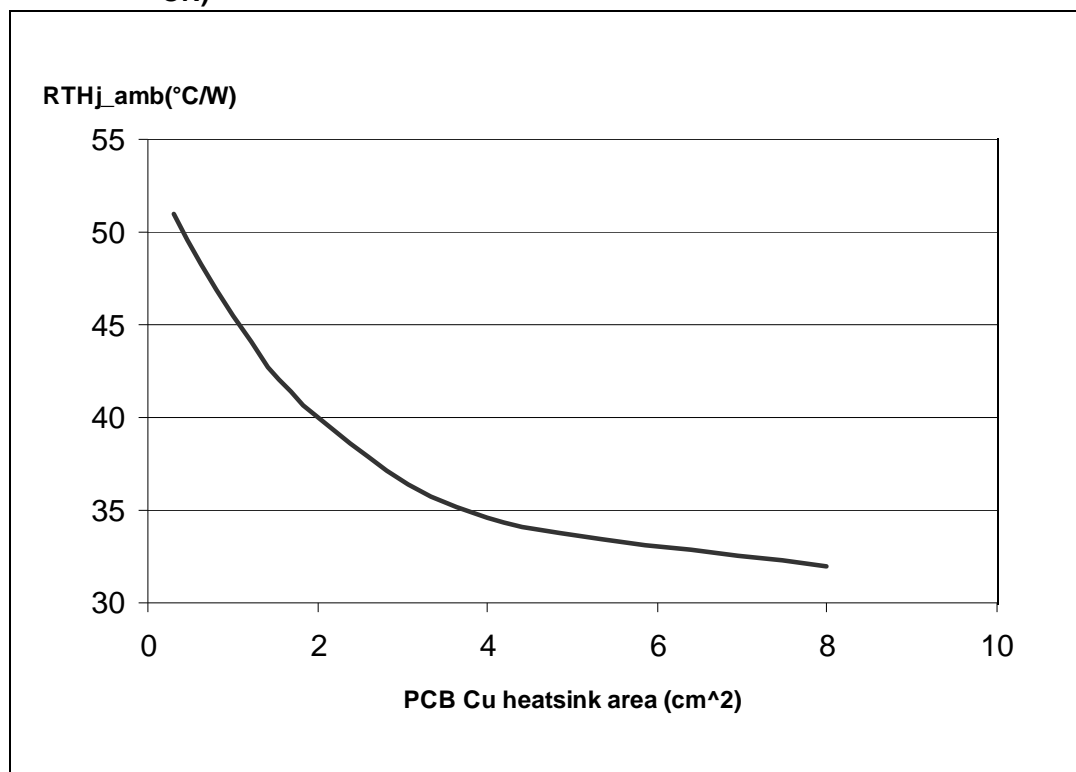
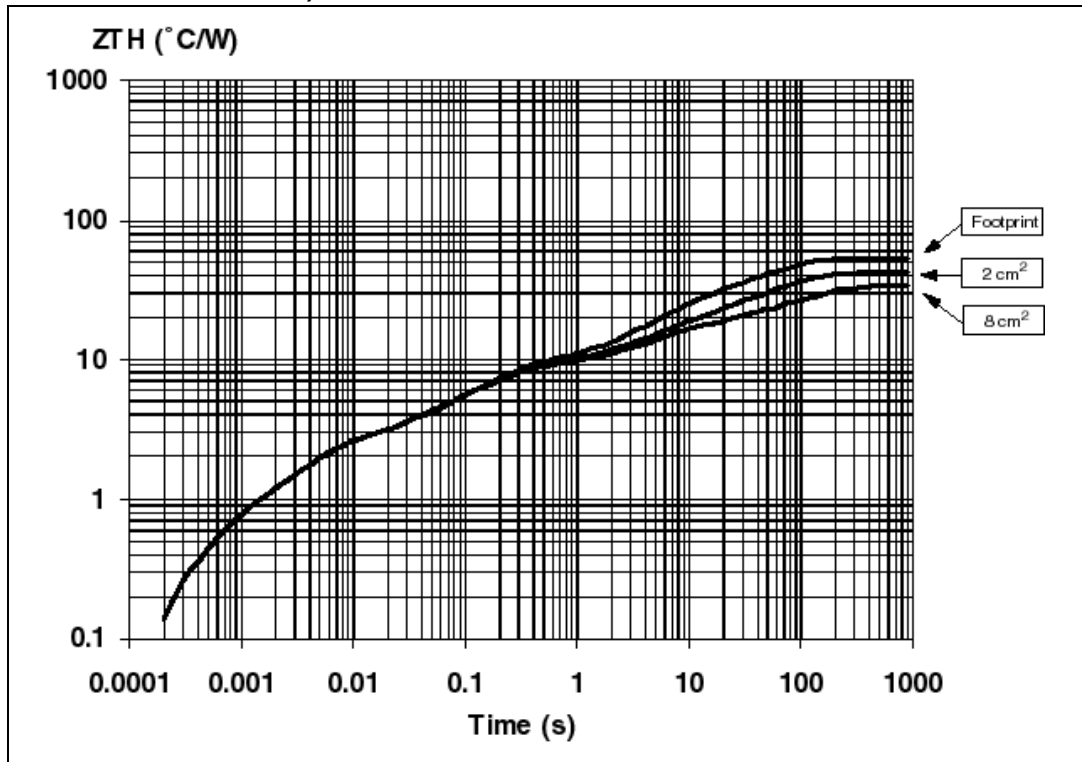




Figure 41. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

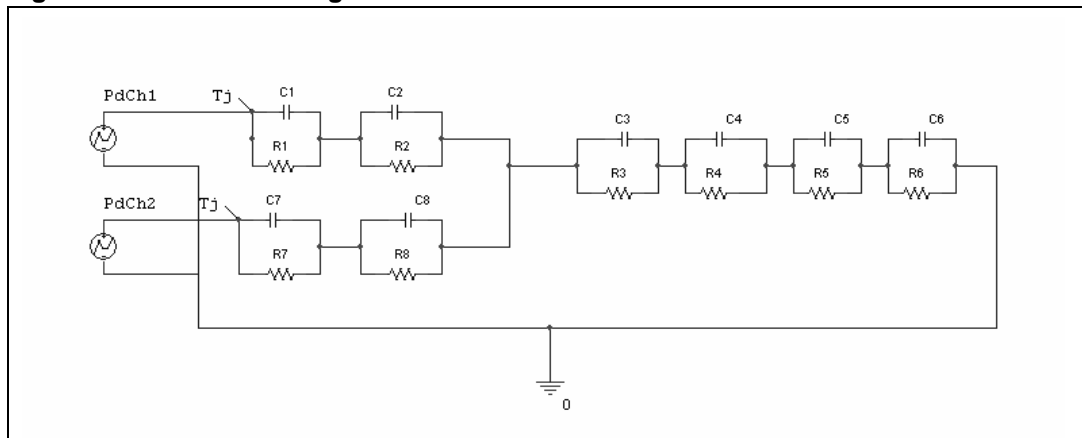


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 42. Thermal fitting model of a double channel HSD in PowerSSO-24



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. Thermal parameters

Area / island (cm <sup>2</sup> )	Footprint	2	8
R1 = R7 (°C/W)	0.4		
R2 = R8 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 = C7 (W.s/°C)	0.001		
C2 = C8 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

## 5 Package and packing information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 5.2 PowerSSO-12 package information

Figure 43. PowerSSO-12 package dimensions

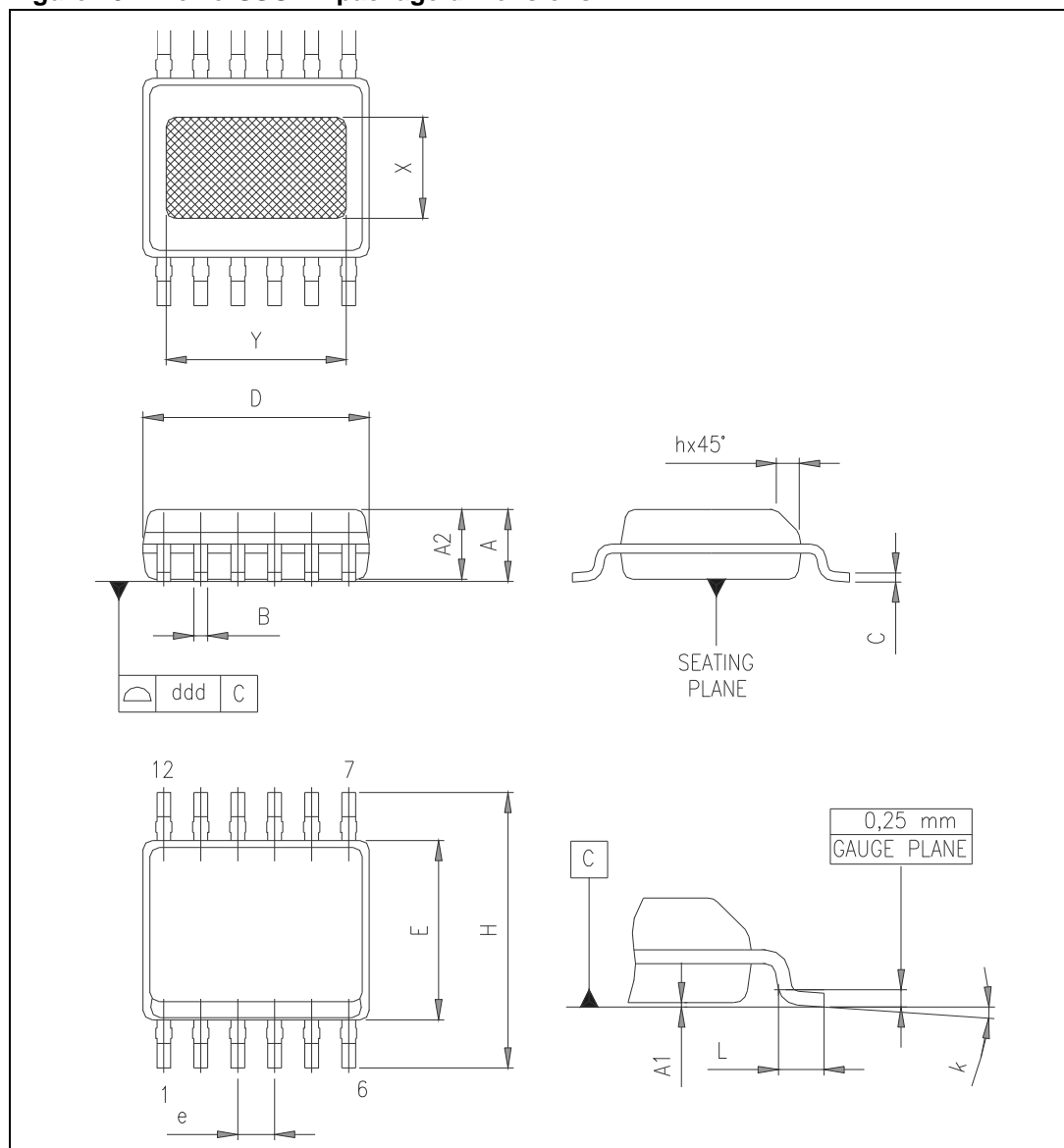


Table 17. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.62
A1	0		0.1
A2	1.10		1.65
B	0.23		0.41
C	0.19		0.25
D	4.8		5.0
E	3.8		4.0
e		0.8	
H	5.8		6.2
h	0.25		0.5
L	0.4		1.27
k	0°		8°
X	1.9		2.5
Y	3.6		4.2
ddd			0.1

### 5.3 PowerSSO-24 package information

Figure 44. PowerSSO-24 package dimensions

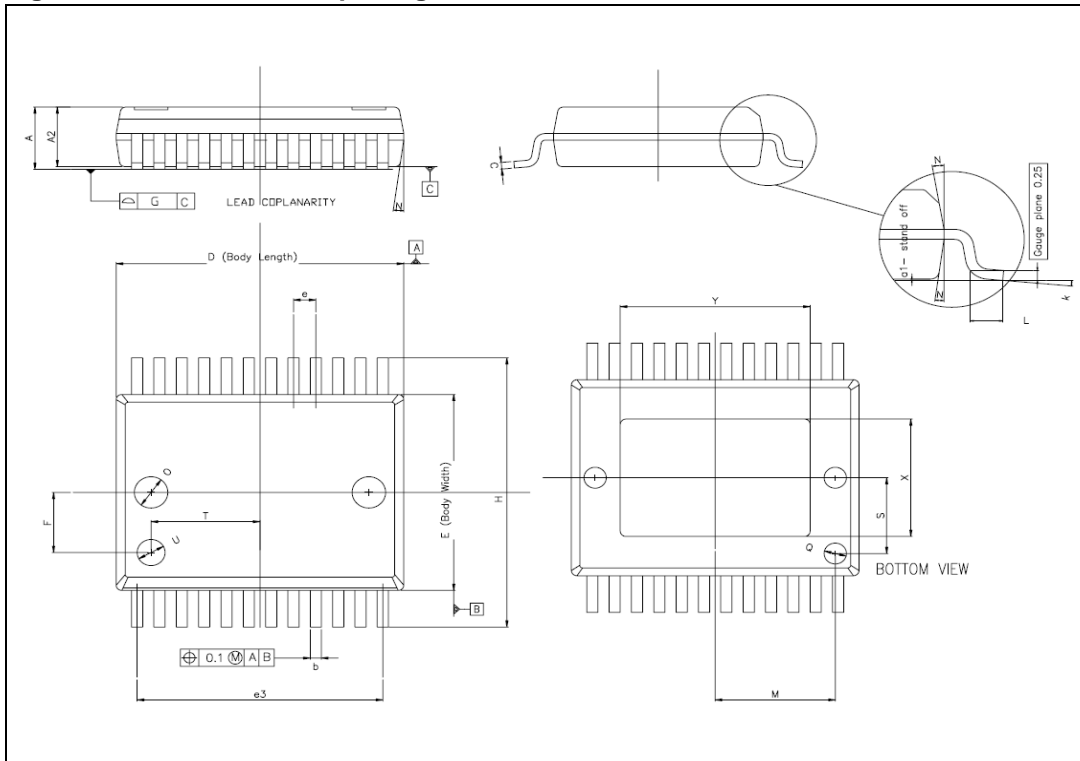


Table 18. PowerSSO-24 mechanical data<sup>(1) (2)</sup>

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D <sup>(3)</sup>	10.10		10.50
E <sup>(3)</sup>	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
N			10°
X	4.1		4.7
Y	6.5		7.1

1. No intrusion allowed inwards the leads.
2. Flash or bleeds on exposed die pad shall not exceed 0.5 mm per side
3. "D and E" do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.15 mm per side

### 5.4 PowerSSO-12 packing information

Figure 45. PowerSSO-12 tube shipment (no suffix)

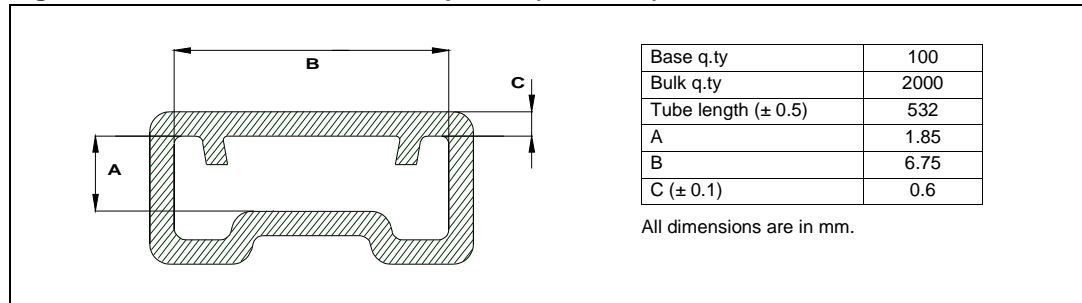
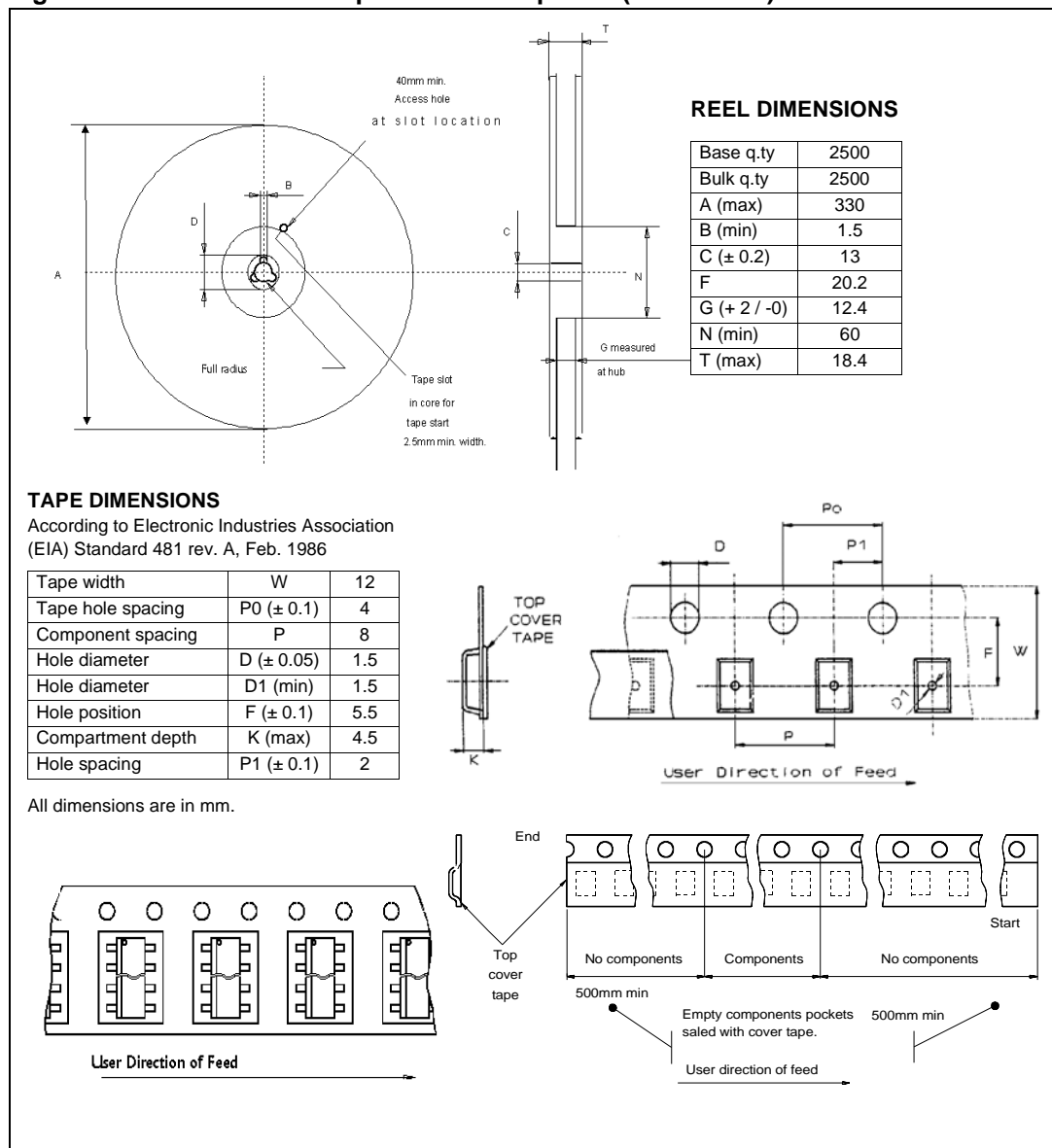


Figure 46. PowerSSO-12 tape and reel shipment (suffix "TR")



### 5.5 PowerSSO-24 packing information

Figure 47. PowerSSO-24 tube shipment (no suffix)

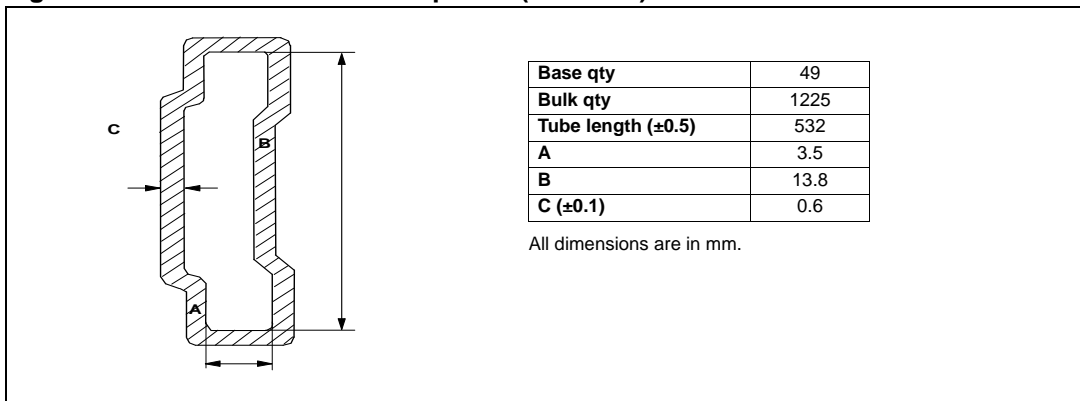
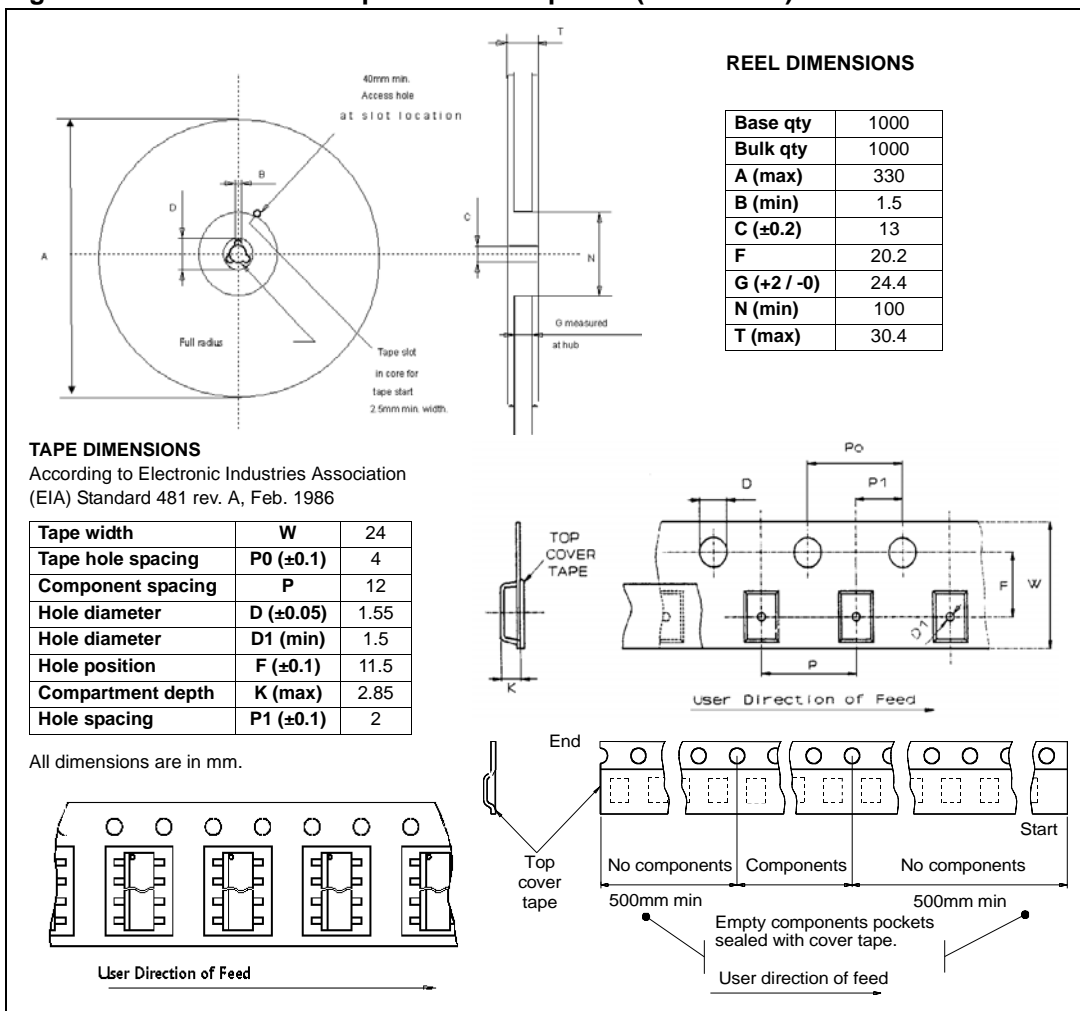


Figure 48. PowerSSO-24 tape and reel shipment (suffix “TR”)





## 6 Order codes

Table 19. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VND5E050ACJ-E	VND5E050ACJTR-E
PowerSSO-24	VND5E050ACK-E	VND5E050ACKTR-E

## 7 Revision history

**Table 20. Document revision history**

Date	Revision	Changes
18-Nov-2011	1	Initial release.
18-Sep-2013	2	Updated disclaimer.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)