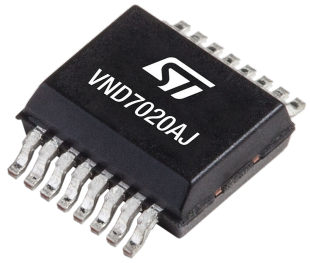
VND7020AJ

Datasheet

Double channel high-side driver with MultiSense analog feedback for automotive applications



Product status link
VND7020AJ

Features

Max transient supply voltage	VCC	40 V
Operating voltage range	VCC	4 to 28 V
Typ. on-state resistance (per Ch)	RON	22 mΩ
Current limitation (typ)	ILIMH	63 A
Standby current (max)	ISTBY	0.5 µA

- AEC-Q100 qualified
- General
  - Double channel smart high side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for automotive turn indicators (up to 2x P27W or SAE1156 and R5W paralleled or LED rear combinations)

Description

The device is a double channel high-side driver manufactured using ST proprietary VIPower® M07 technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A FaultRST pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

1 Block diagram and pin description

Figure 1. Block diagram

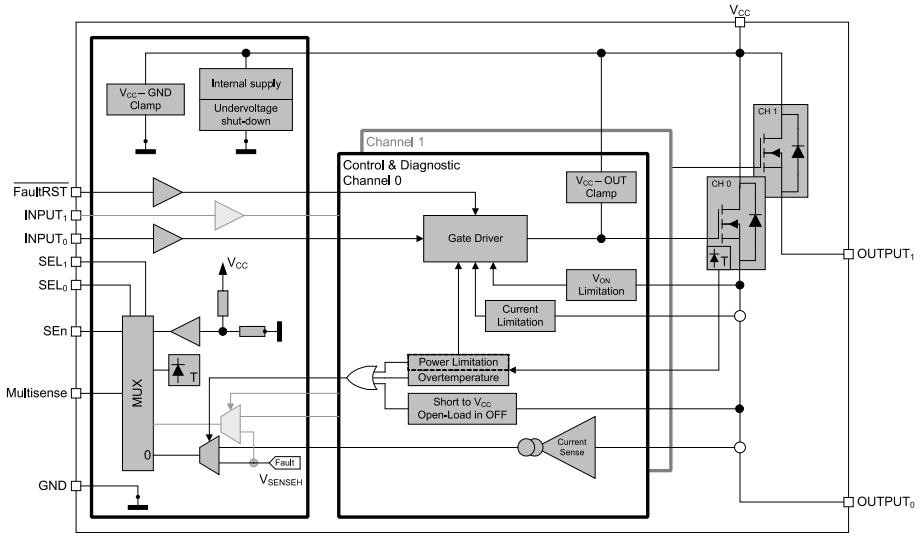


Table 1. Pin functions

Name	Function
VCC	Battery connection.
$OUTPUT_{0,1}$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
$INPUT_{0,1}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
SEL0,1	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer.
FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart. mode

Figure 2. **Block diagram and pin desription**

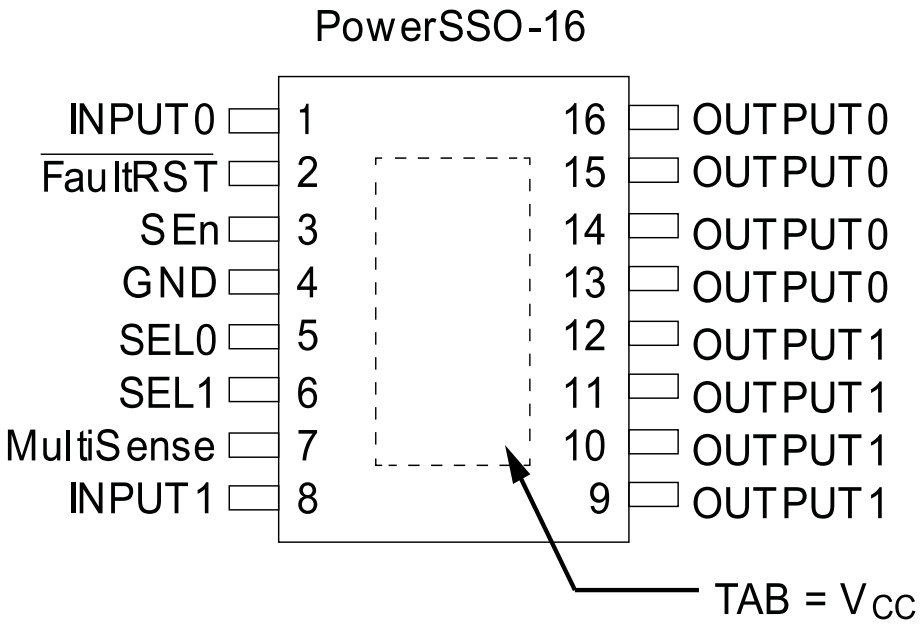


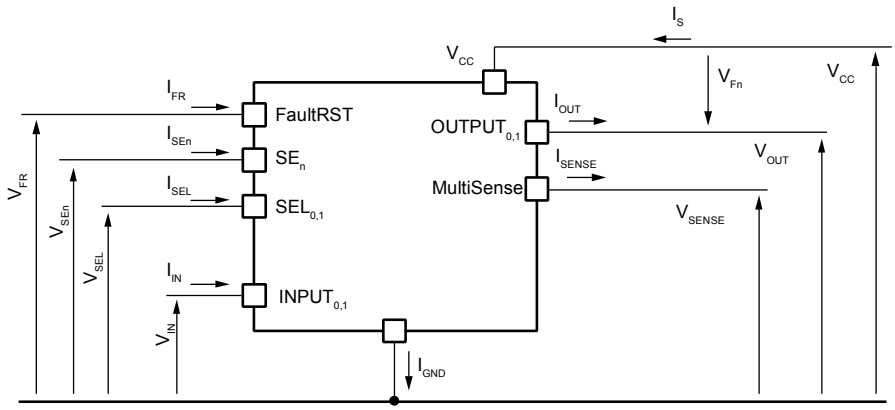
Table 2. **Suggested connections for unused and not connected pins**

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, FaultRST
Floating	Not allowed	X (1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. *X: do not care.*

2 Electrical specification

Figure 3. Current and voltage conventions



Note: V_{FnV}=$O_{UTn-VCC}$ during reverse battery condition.

Table 3. Suggested connections for unused and not connected pins

Connction/pin	MultiSense	N.C.	Output	Input	SEn, SELx, FaultRST
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. *X: do not care.*

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 4 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40V; R_L = 4 Ω)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1}$ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	17	
I_{IN}	$INPUT_{0,1}$ DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		

Symbol	Parameter	Value	Unit
I_{SEL}	$SEL_{0,1}$ DC input current	-1 to 10	mA
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	-20	
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150 °C)	64	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) • $INPUT_{0,1}$ • MultiSense • SEn, $SEL_{0,1}$, FaultRST • $OUTPUT_{0,1}$ □ VCC	4000 2000 4000 4000 4000	V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) (1)(2)	4.9	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(3)	55.5	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(2)	21.5	

1. *One channel ON.*
2. *Device mounted on four-layers 2s2p PCB*
3. *Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace*

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	V
$V_{USDReset}$	Undervoltage shutdown reset				5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
R_{ON}	On-state resistance (1)	I_{OUT} = 3 A; T_j = 25°C		22		mΩ
		I_{OUT} = 3 A; T_j = 150°C			44	
		I_{OUT} = 3 A; V_{CC} = 4 V; T_j = 25°C			30	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	Clamp voltage	I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	V
		I_S = 20 mA; T_j = -40°C	38			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V (2)	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C(3)			0.5	
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V VIN = VOUT = VFR = VSEL0,1 = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN0} = 5 V; V_{IN1} = 5 V; I_{OUT0} = 0 A; I_{OUT1} = 0 A		5	8	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN0} = 5 V; V_{IN1} = 5 V; I_{OUT0} = 3 A; I_{OUT1} = 3 A			12	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V(1)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage(1)	I_{OUT} = -3 A; T_j = 150°C			0.7	V

1. *For each channel*
2. *PowerMOS leakage included.*
3. *Parameter specified by design; not subject to production test.*

Table 7. Switching

V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 4.3 Ω	10	60	120	µs
$t_{d(off)}$(1)	Turn-off delay time at T_j = 25 °C		10	40	100	
(dVOUT/dt)on(1)	Turn-on voltage slope at T_j = 25 °C	R_L = 4.3 Ω	0.1	0.36	0.7	V/µs
(dVOUT/dt)off(1)	Turn-off voltage slope at T_j = 25 °C		0.1	0.36	0.7	
W_{ON}	Switching energy losses at turn-on (twon)	R_L = 4.3 Ω	—	0.38	0.49 (2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 4.3 Ω	—	0.39	0.54(2)	mJ
t_{SKEW}(1)	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 4.3 Ω	-75	-25	25	µs

1. *See Figure 6: "Switching time and Pulse skew"*

2. *Parameter guaranteed by design and characterization; not subject to production test.*

Table 8. Logic inputs

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$INPUT_{0,1}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
FaultRST characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 9. Protections

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	45	63	90	A
		4 V < V_{CC} < 18 V(1)				
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		23		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (TTSD - TR)(1)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40°C; V_{CC} = 13 V		60		K
t_{LATCH_RST}	Fault reset time for output unlatch(1)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; □ E.g. Ch_0: V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40°C	VCC 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25°C to 150°C	VCC 41	VCC 46	VCC 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.5 A		20		mV

1. *Parameter guaranteed by design and characterization; not subject to production test.*

Table 10. MultiSense

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
Current sense characteristics						
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	1020			
dK_{cal}/K_{cal}(1)(2)	Current sense ratio drift at calibration point	I_{OUT} = 0.01 A to 0.05 A; I_{cal} = 30 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.1 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	1800	3450	5100	
dK_{LED}/K_{LED}(1)(2)	Current sense ratio drift	I_{OUT} = 0.1 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	2120	3020	3915	

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
dK_0/K_0 (1)(2)	Current sense ratio drift	I_{OUT} = 0.5 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20		20	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	2060	2875	3690	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 1 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	2340	2755	3170	
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 3 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-6		6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 9 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	2550	2740	2950	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 9 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%
$dK/K_{(tot)}$ (1)(3)	Current sense ratio drift for single point calibration	Calibration point: I_{cal} = 2.4 A; T_j = 25°C; V_{CC} = 13 V I_{OUT} = 0.5 A I_{OUT} = 1.5 A I_{OUT} = 2.0 A I_{OUT} = 2.4 A I_{OUT} = 3.0 A I_{OUT} = 4.0 A	 -30 -13 -7 -6 -7 -8		 30 13 7 6 7 8	 % % % % % %
V_{OUT_MSD} (1)	Output Voltage for MultiSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ; □ E.g. Ch_0: V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; IOUT0 = 3 A		5		V
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V	0		0.5	µA
		MultiSense disabled: -1 V < VSENSE < 5 V (1)	-0.5		0.5	
		MultiSense enabled: V_{SEn} = 5 V; All channels ON; I_{OUTX} = 0 A; Ch_X diagnostic selected; • E.g. Ch_0: V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; I_{OUT1} = 3 A	0		2	
		MultiSense enabled: V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected:	0		2	

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{SENSE0}	MultiSense leakage current	• E.g. Ch_0: V_{IN0} = 0 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; IOUT1 = 3 A				µA
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 kΩ; V_{SEn} = 5 V; V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 9 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	11.5			A
OFF-state diagnostic						
V_{OL}	OFF-state openload voltage detection threshold	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = 40°C to 125°C	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 9)	V_{SEn} = 5 V; Ch_X ON to OFF transition; Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN0} = 0 V; V_{IN1} = 0 V; V_{FR} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		$V_{SENSE\_TC\ (T)} = VS_{ENSE\_TC\ (T0)} + dV_{SENSE\_TC}$ / dT * (T - T0)				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function (4)		$V_{SENSE\_VCC} = V_{CC}$ / 4				
Fault diagnostic feedback (see Table 11)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ; • E.g: Ch_0 in open load V_{IN0} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see *Figure 7*")						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; RL = 4.3 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; RL = 4.3 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; RL = 4.3 Ω		100	250	µs
$\Delta_{tDSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 4.3 Ω			100	µs
$t_{DSENSE2L}$	Current sense turnoff delay time from falling edge of	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; RL = 4.3 Ω		50	250	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
	INPUT					
MultiSense timings (chip temperature sense mode - see Figure 8)						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see Figure 8)						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (Multiplexer transition times)(5)						
t_{D_XtoY}	MultiSense transition delay from Ch_X to Ch_Y	V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 0 A; I_{OUT1} = 3 A; RSENSE = 1 kΩ			20	µs
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT0} = 1.5 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT0} = 1.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT1} = 1.5 A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT1} = 1.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V;			20	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
		R_{SENSE} = 1 kΩ				
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVSENSEH}$	MultiSense transition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	V_{IN0} = 5 V; V_{IN1} = 0 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 3 A; V_{OUT1} = 4 V; R_{SENSE} = 1 kΩ			20	µs

1. *Parameter guaranteed by design and characterization; not subject to production test.*
2. *All values refer to VCC = 13 V; Tj = 25°C, unless otherwise specified.*
3. *Total current drift over -40 °C to 150 °C, V_{CC}: 7 V to 18 V and output current variation, respect to a calibration point measured at T_j = 25 °C and V_{CC} = 13 V.*
4. *V_{CC} sensing and TC sensing are referred to GND potential.*
5. *Transition delay are measured up to +/- 10% of final conditions.*

Figure 4. IOUT/ISENSE versus IOUT

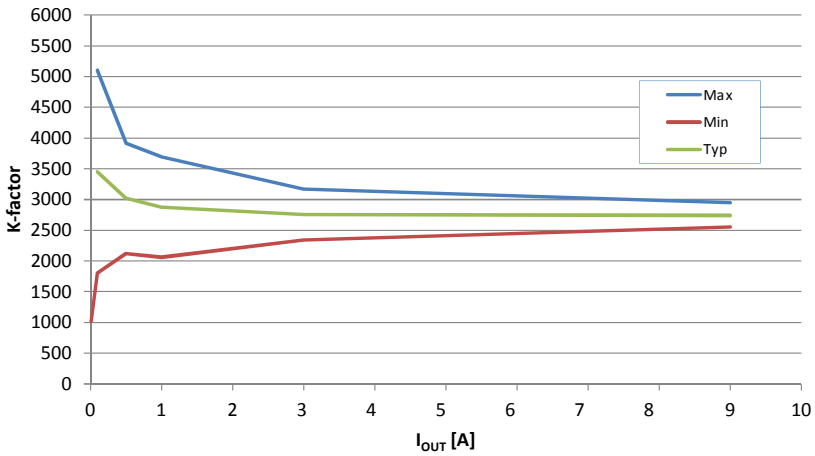


Figure 5. **Current sense accuracy versus IOUT**

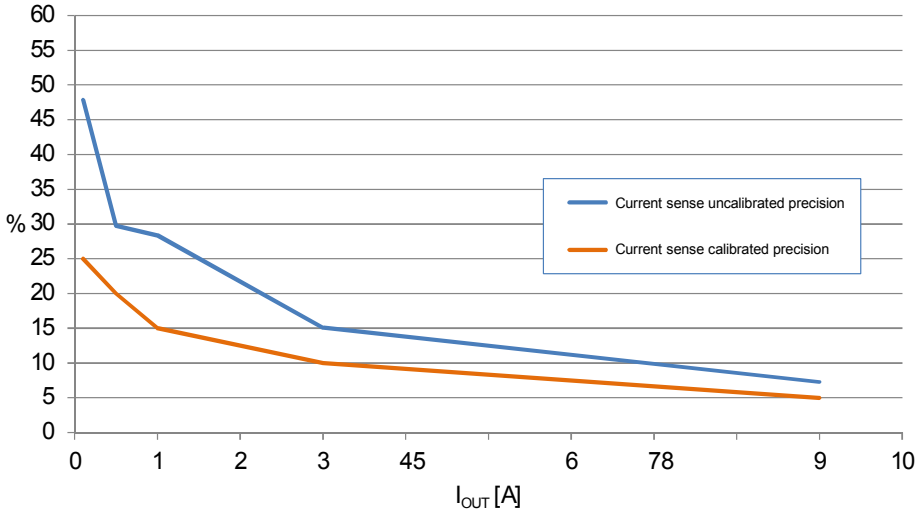


Figure 6. **Switching time and Pulse skew**

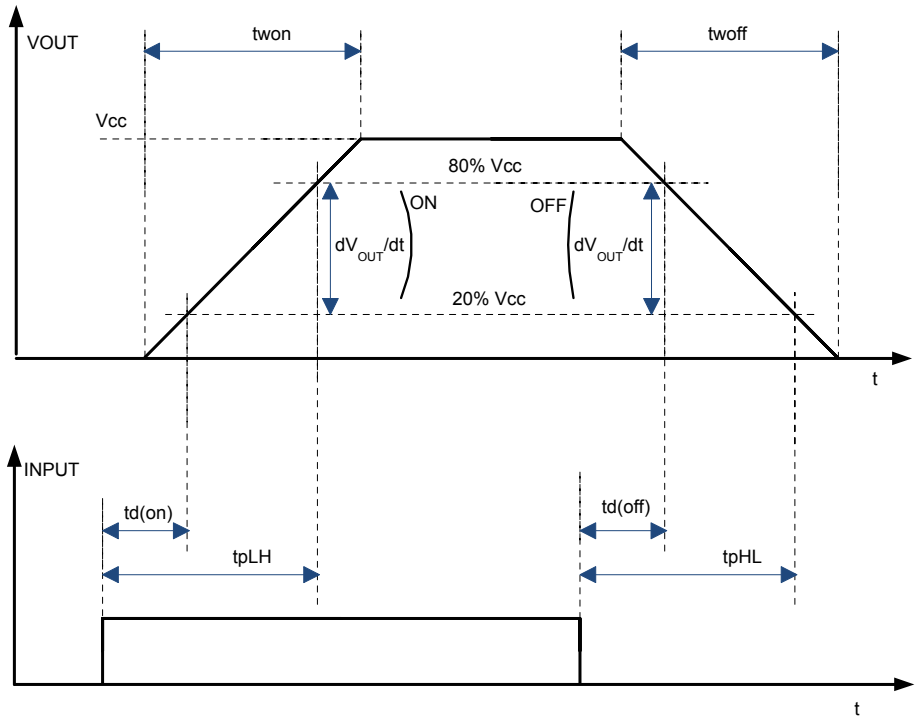


Figure 7. **MultiSense timings (current sense mode)**

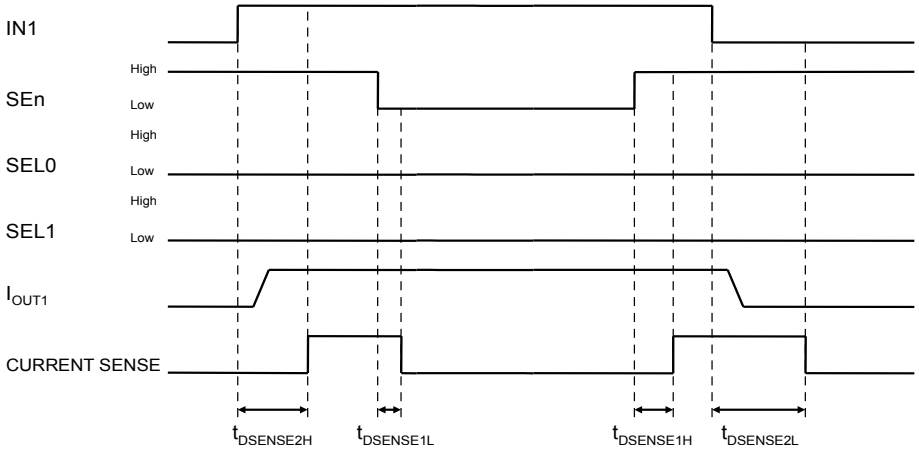


Figure 8. **Multisense timings (chip temperature and VCC sense mode)**

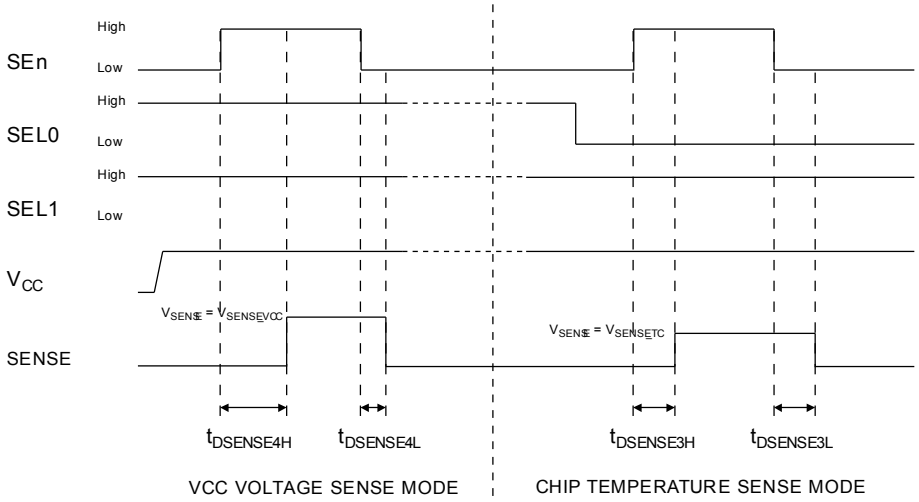


Figure 9. **TDSTKON**

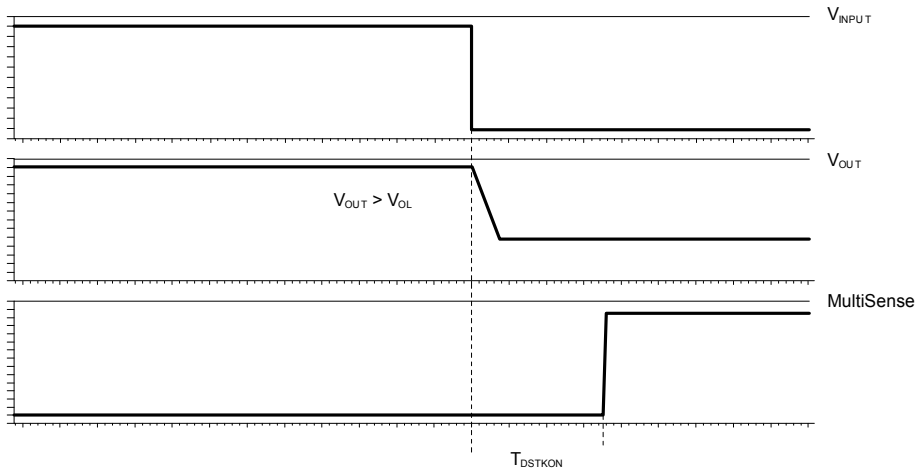


Table 11. Truth table

Mode	Conditions	IN X	F R	SE n	SEL X	OUT X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150 °C	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Outputs configured for auto-restart
		H	H			H	See (1)	Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Output cycles with temperature hysteresis
		H	H			L	See (1)	Output latches-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD}$ + VUSDhyst (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See (1)		H	See (1)	
	Open-load	L	X			H	See (1)	External pull-up
Negative output voltage	Inductive loads turnoff	L	X	See (1)		< 0 V	See (1)	

1. *Refer to Table 12*

Table 12. MultiSense multiplexer addressing

SEn	SEL_1	SEL_0	MUXchannel	MultiSense output			
				Normal mode	Overload	OFF-state diag. (1)	Negative output
L	X	X			Hi-Z		
H	L	L	Channel 0 diagnostic	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H	Channel 1 diagnostic	$I_{SENSE} = 1/K * I_{OUT1}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	L	T_{CHIP} Sense		$V_{SENSE} = V_{SENSE\_TC}$		
H	H	H	V_{CC} Sense		$V_{SENSE} = V_{SENSE\_VCC}$		

1. *In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.*

Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0.

Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

2.4 Waveforms

Figure 10. **Latch functionality - behavior in hard short circuit condition (TAMB << TTSD)**

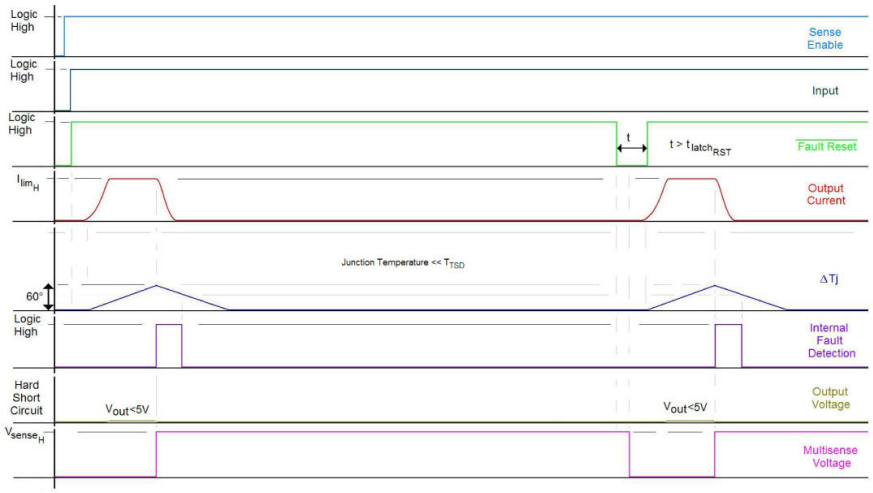


Figure 11. **Latch functionality - behavior in hard short circuit condition**

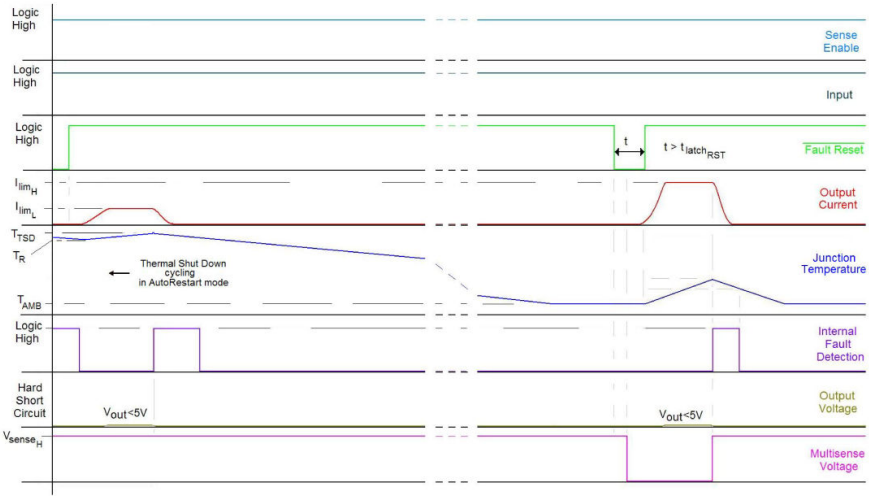


Figure 12. **Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)**

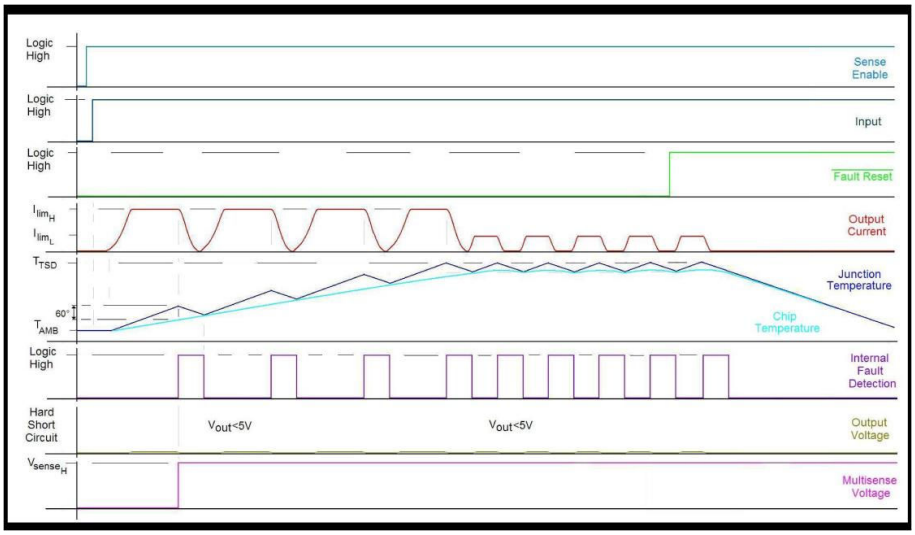


Figure 13. **Standby mode activation**

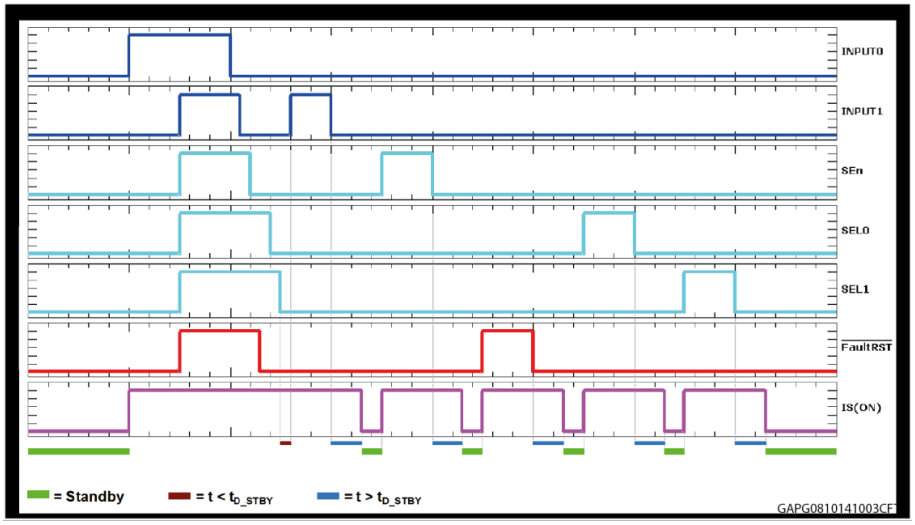
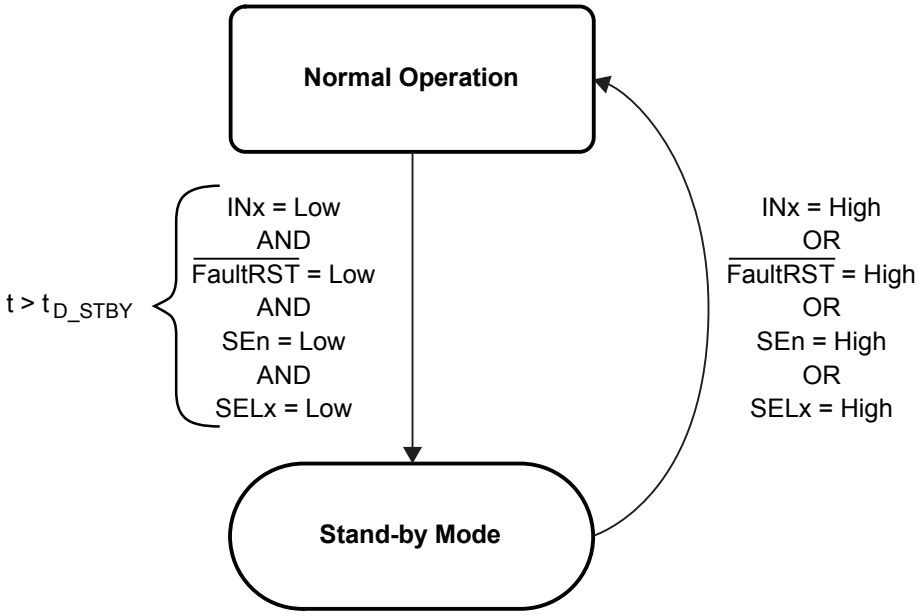


Figure 14. **Standby state diagram**



2.5 Electrical characteristics curves

Figure 15. **OFF-state output current**

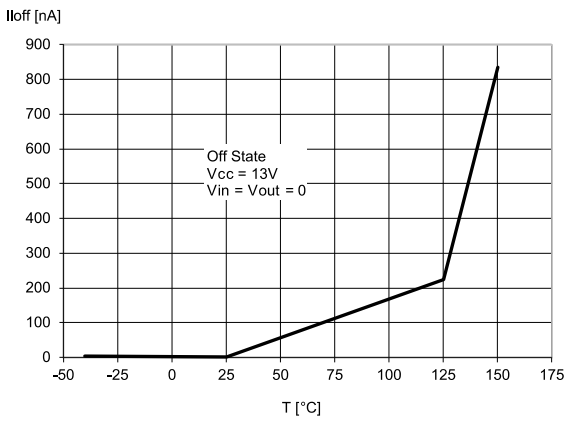


Figure 16. **Standby current**

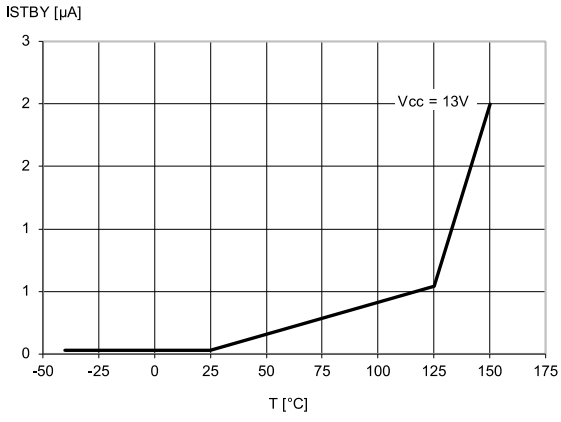


Figure 17. IGND(ON) vs. Iout

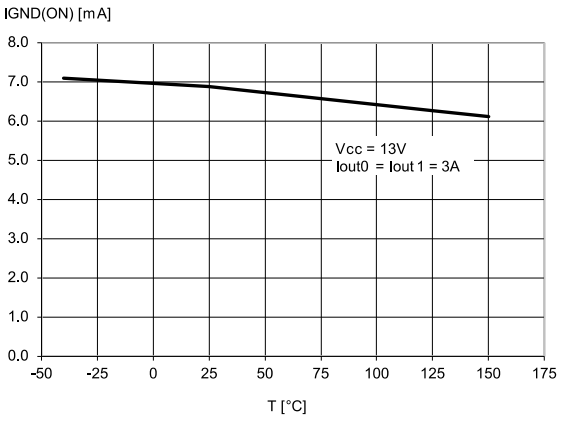


Figure 18. Logic Input high level voltage

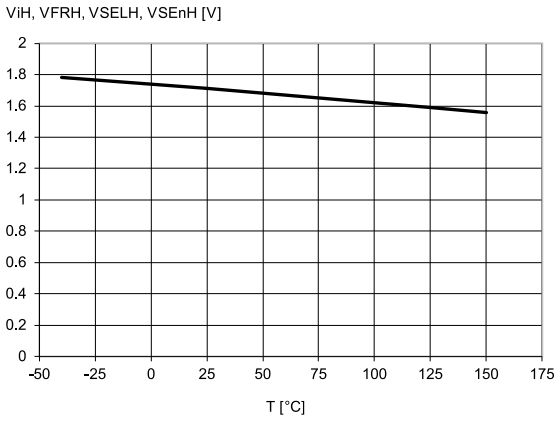


Figure 19. Logic Input low level voltage

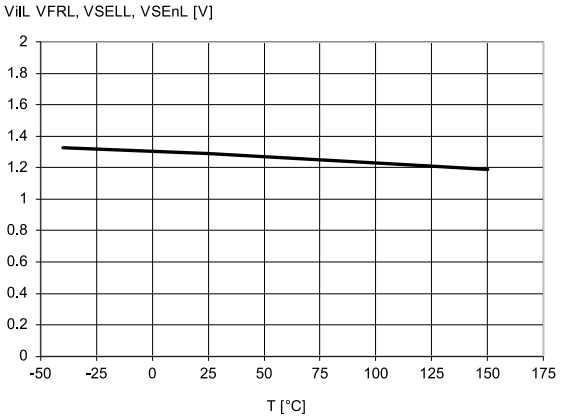


Figure 20. High level logic input current

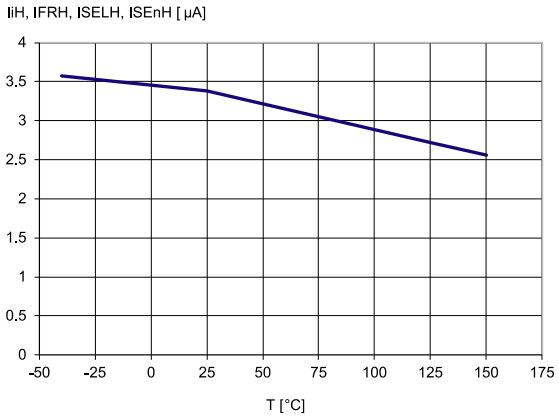


Figure 21. Low level logic input current

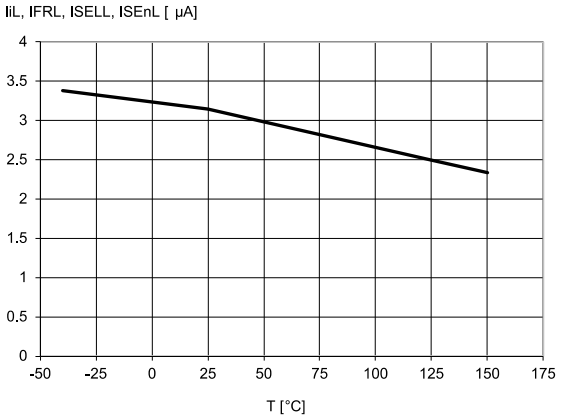


Figure 22. Logic Input hysteresis voltage

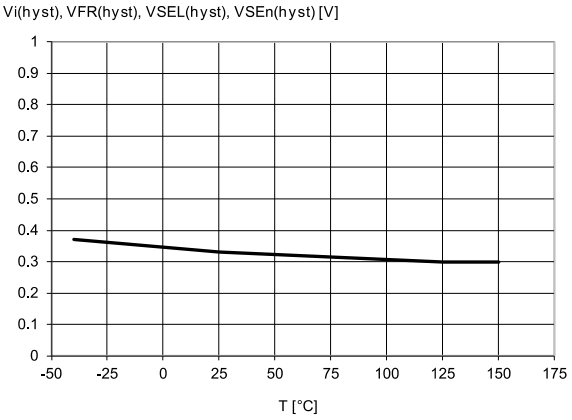


Figure 23. FaultRST Input clamp voltage

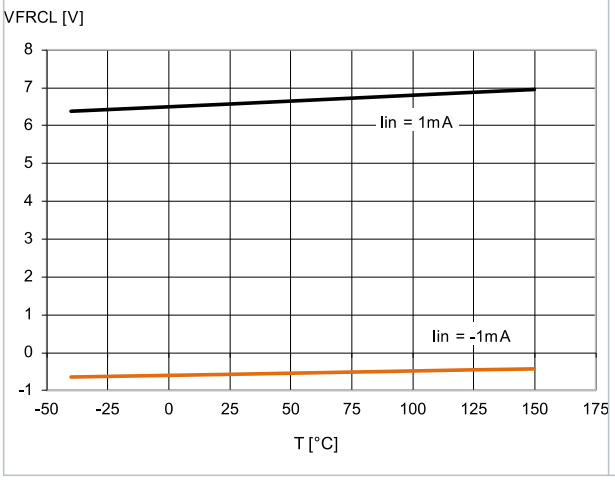


Figure 24. Undervoltage shutdown

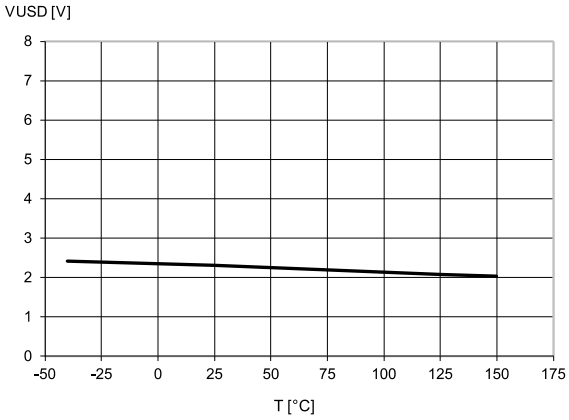


Figure 25. On-state resistance vs. Tcase

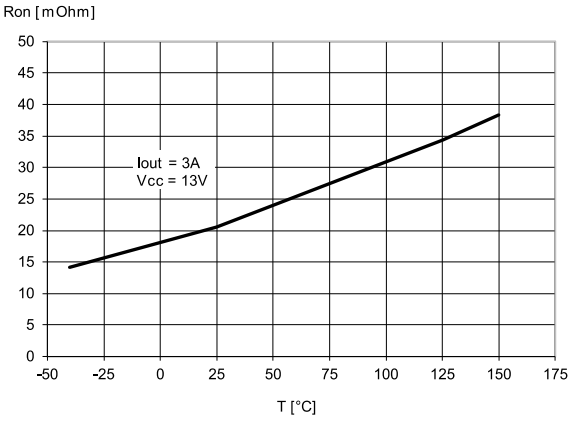


Figure 26. On-state resistance vs. VCC

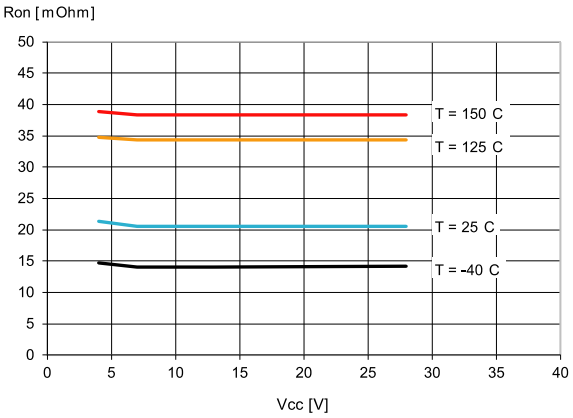


Figure 27. Turn-on voltage slope

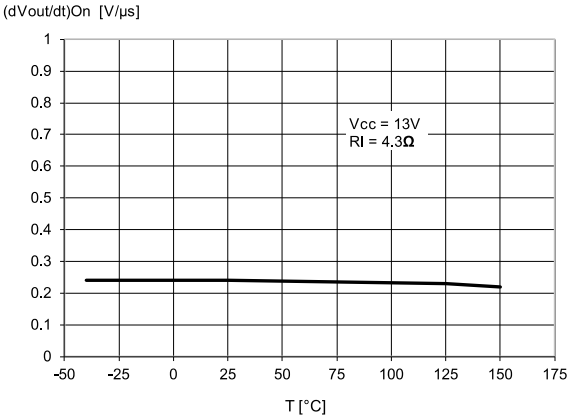


Figure 28. Turn-off voltage slope

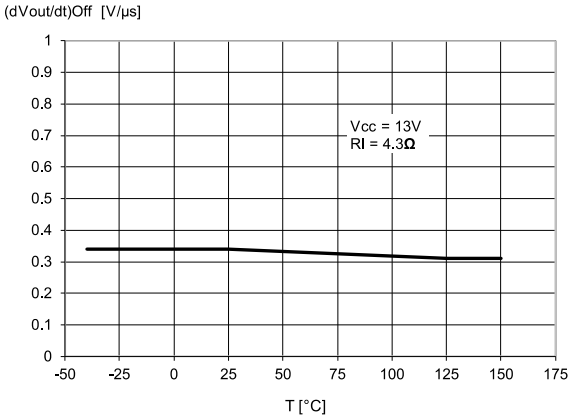


Figure 29. Won vs. Tcase

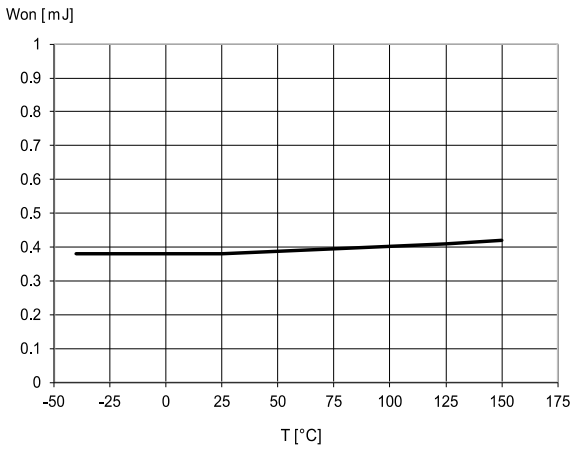


Figure 30. Woff vs. Tcase

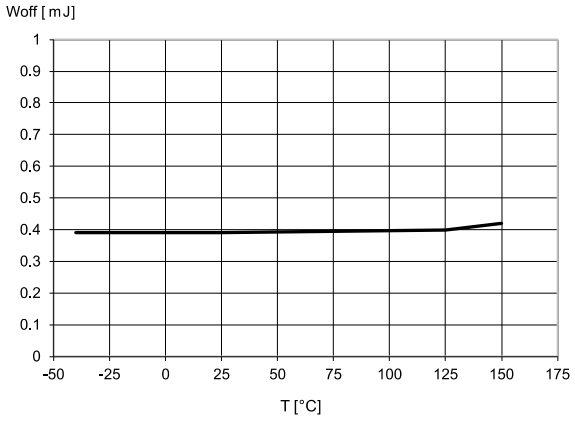


Figure 31. ILIMH vs. Tcase

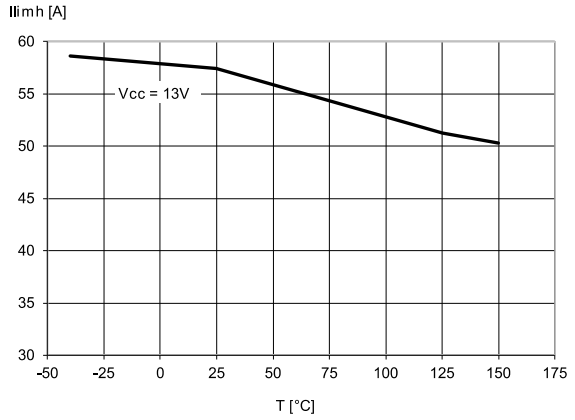


Figure 32. OFF-state open-load voltage detection threshold

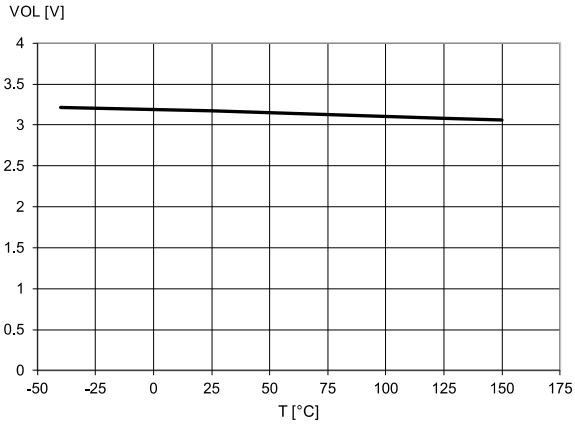


Figure 33. Vsense clamp vs. Tcase

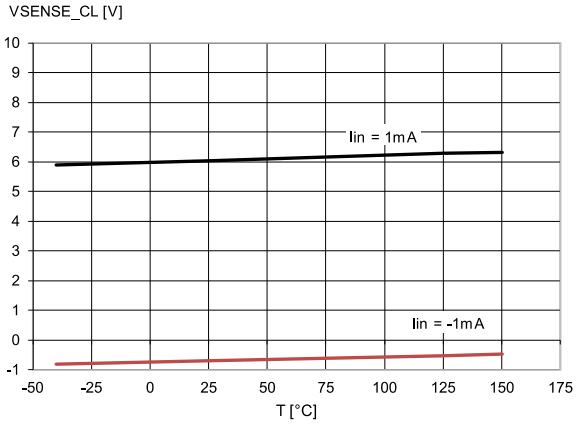
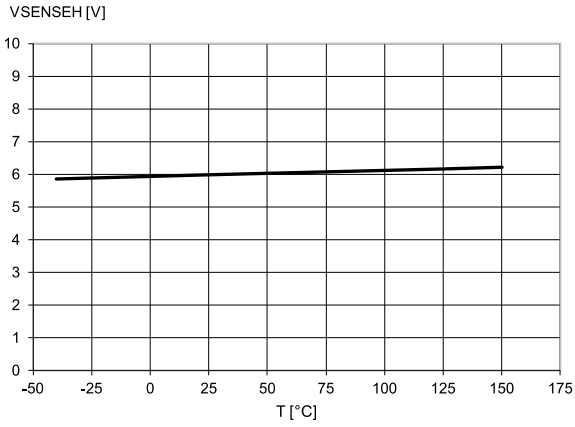


Figure 34. Vsenseh vs. Tcase



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

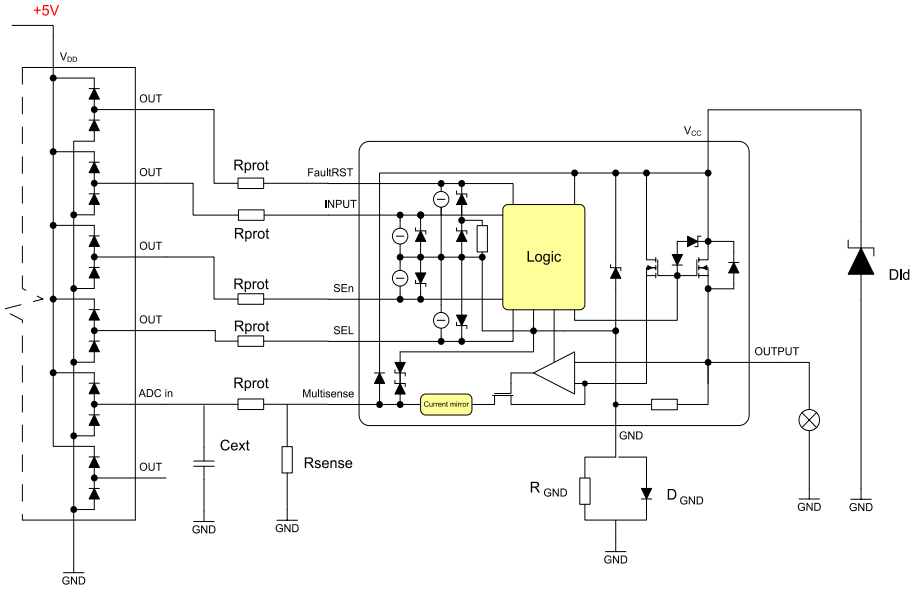
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

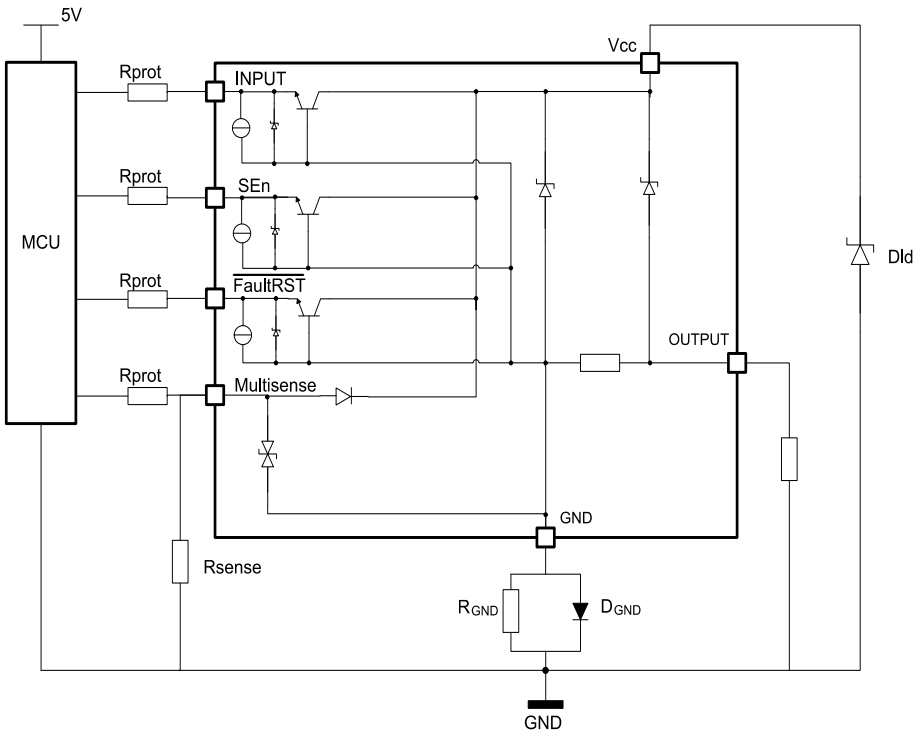
4 Application information

Figure 35. **Application diagram**



4.1 GND protection network against reverse battery

Figure 36. **Simplified internal structure**



4.1.1 Diode (DGND) in the ground line

A resistor (typ. R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in Table 13.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 13. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	US (1)		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a(2)	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4(3)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B(2)		40 V	5 pulse	1 min		400 ms, 2 Ω

1. *US is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.*
2. *With 40 V external suppressor referred to ground (-40°C < T_j < 150 °C).*
3. *Test pulse from ISO 7637-2:2004(E).*

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$VCCpeak/Ilatchup \leq Rprot \leq (VOH\mu C - VIH - VGND) / IIHmax \quad (1)$$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup}$ ≥ 20 mA; $V_{OH\mu C}$ ≥ 4.5 V

7.5 kΩ ≤ R_{prot} ≤ 140 kΩ.

Recommended values: R_{prot} = 15 kΩ

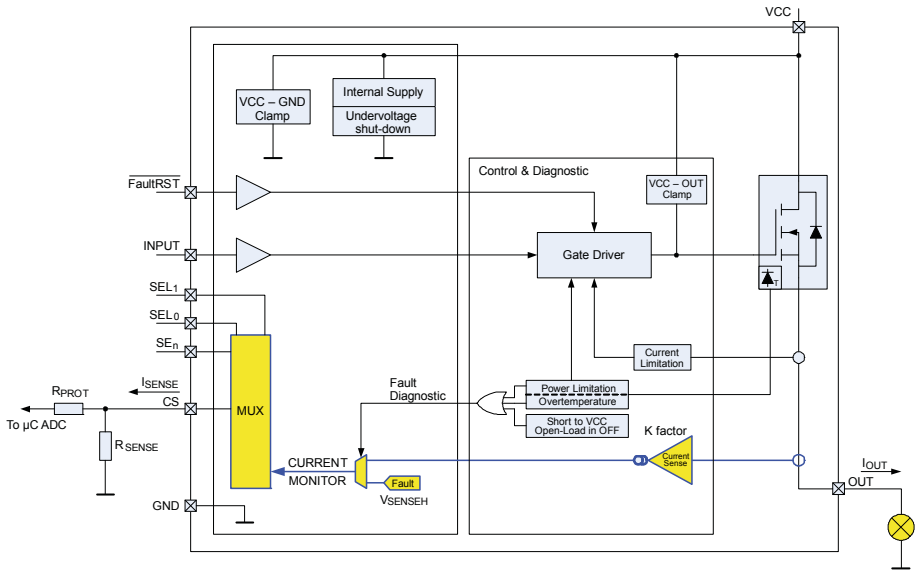
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage propotional to V_{CC}
- T_{CASE}: voltage propotional to chip temperature

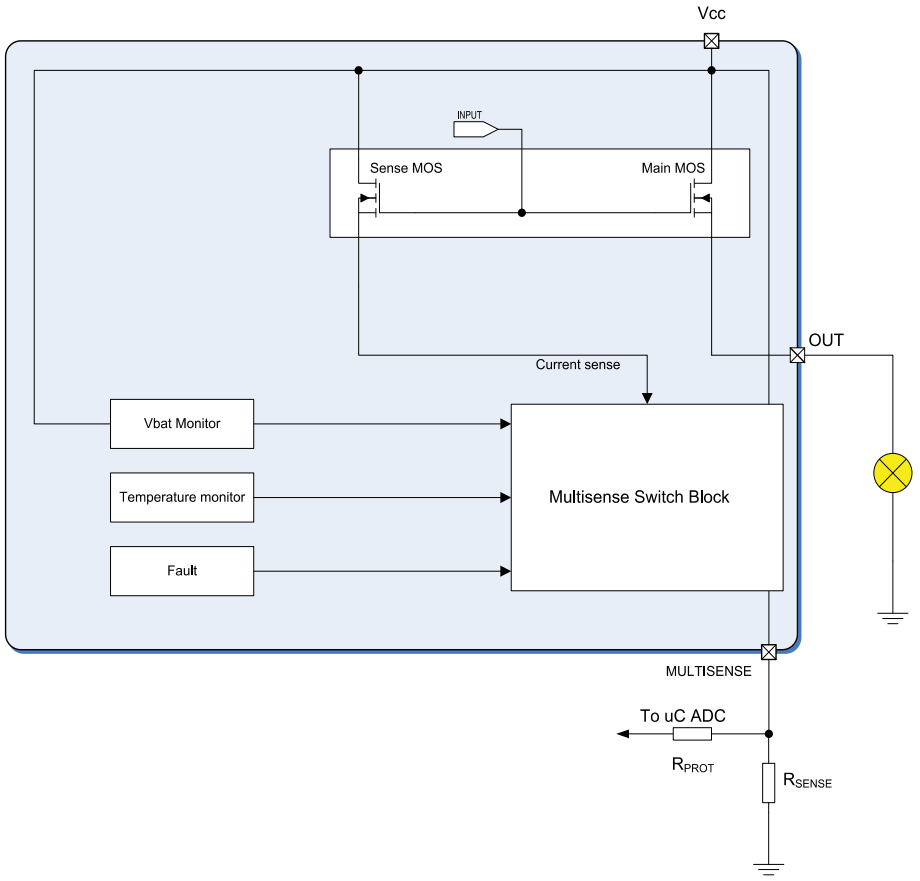
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in Table 12. MultiSense multiplexer addressing.

Figure 37. MultiSense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 38. **MultiSense block diagram**



Current monitor

When current mode is selected in the MultiSense, this output is capable to provide:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENS}E \cdot I_{OUT}/K$

Where:

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from MultiSense pin in current output mode
- I_{OUT} is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the MultiSense pin which is switched to a “current limited” voltage source, V_{SENSEH}.

In any case, the current sourced by the MultiSense in this condition is limited to I_{SENSEH}.

The typical behavior in case of overload or hard short circuit is shown in Section 2.4: Waveforms.

Figure 39. Analogue HSD – open-load detection in off-state

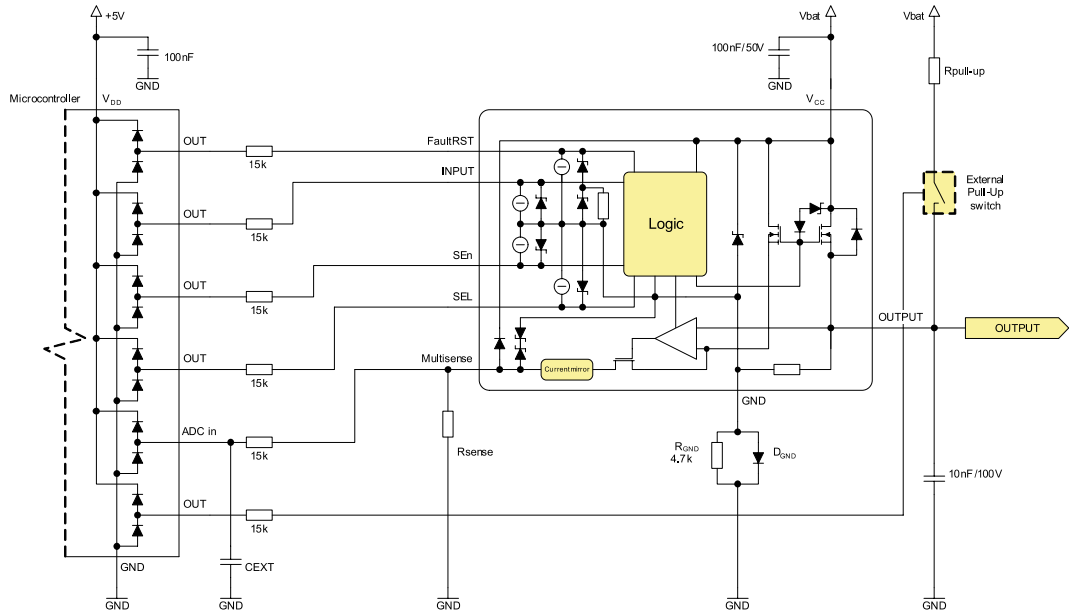


Figure 40. Open-load / short to VCC condition

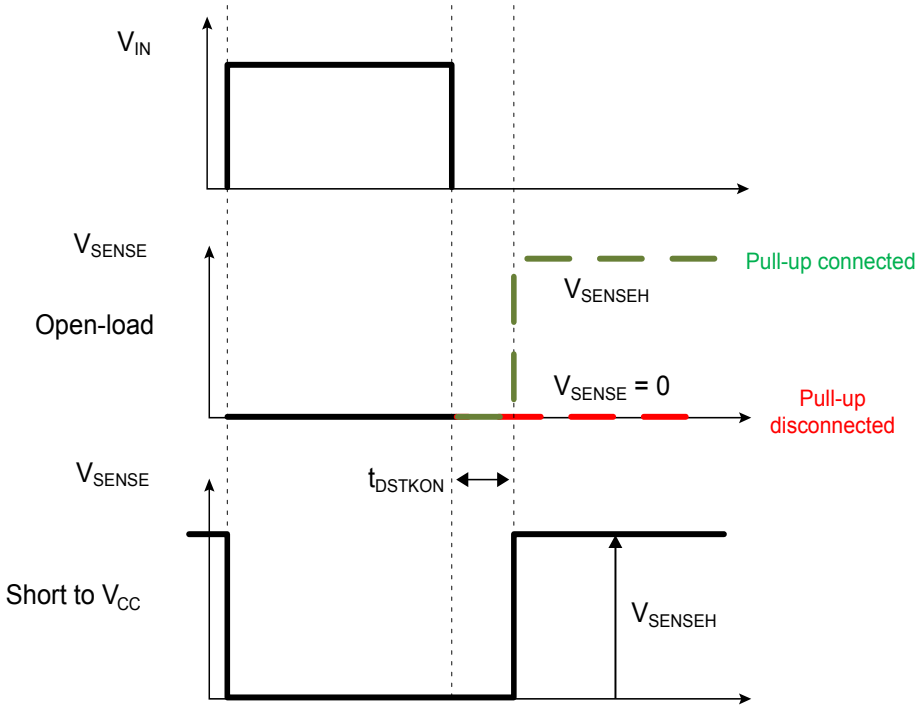


Table 14. MultiSense pin levels in off-state

Condition	Output	MultiSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L

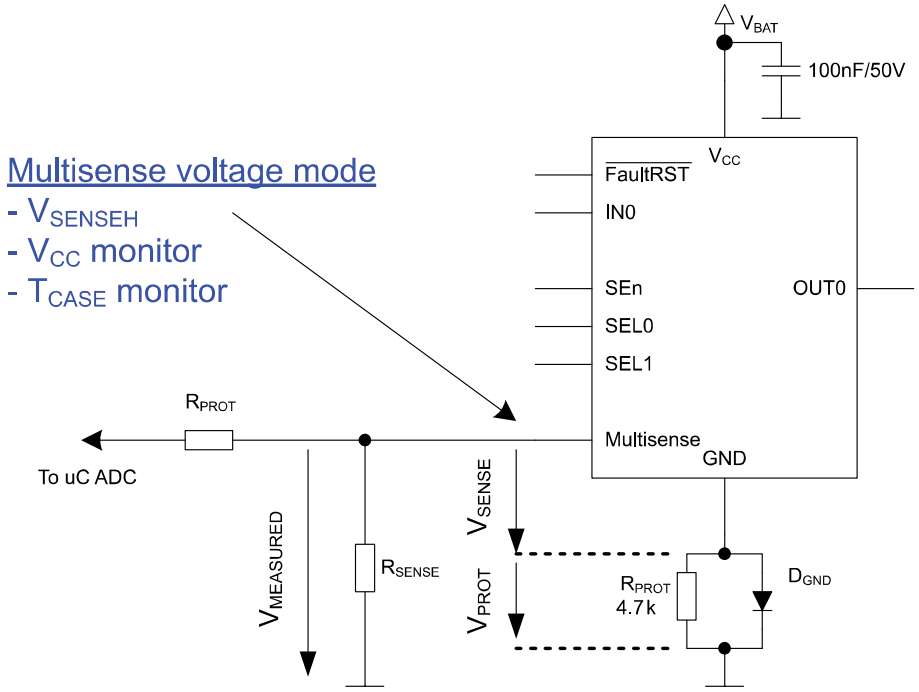
Condition	Output	MultiSense	SEn
Open-load	$V_{OUT} > V_{OL}$	V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 TCASE and VCC monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because a voltage shift is generated between the device GND and the microcontroller input GND reference.

Figure 41 shows the link between $V_{MEASURED}$ and the real V_{SENSE} signal.

Figure 41. GND voltage shift



V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 8$.

Case temperature monitor

Case temperature monitor is capable of providing information about the actual device temperature. Since a diode is used for temperature sensing, the following equation describes the link between temperature and output V_{SENSE} level:

$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T0) + dV_{SENSE\_TC} / dT * (T - T0)$ where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40 °C to 150 °C)).

4.4.3 Short to VCC and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)\min@4V}} \quad (2)$$

5 Maximum demagnetization energy (VCC = 16 V)

Figure 42. **Maximum turn off current versus inductance**

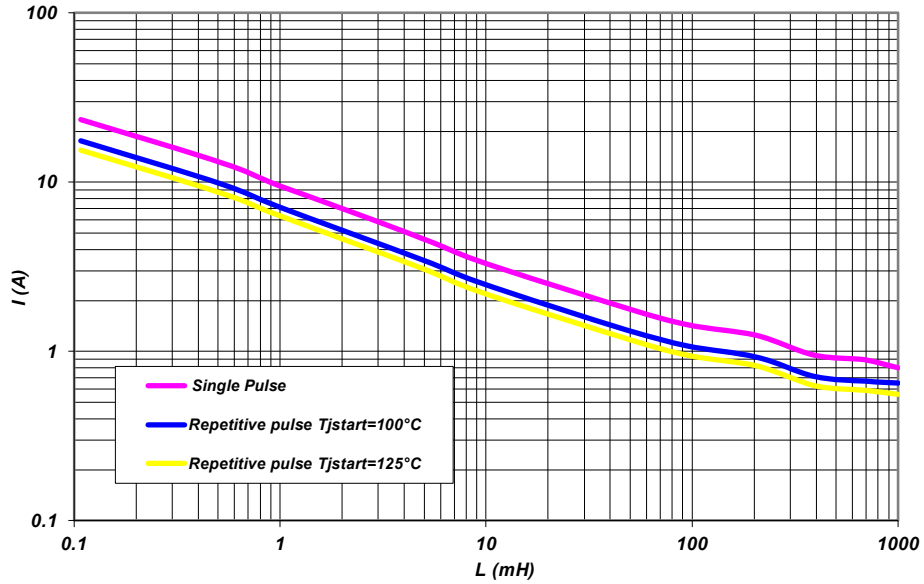
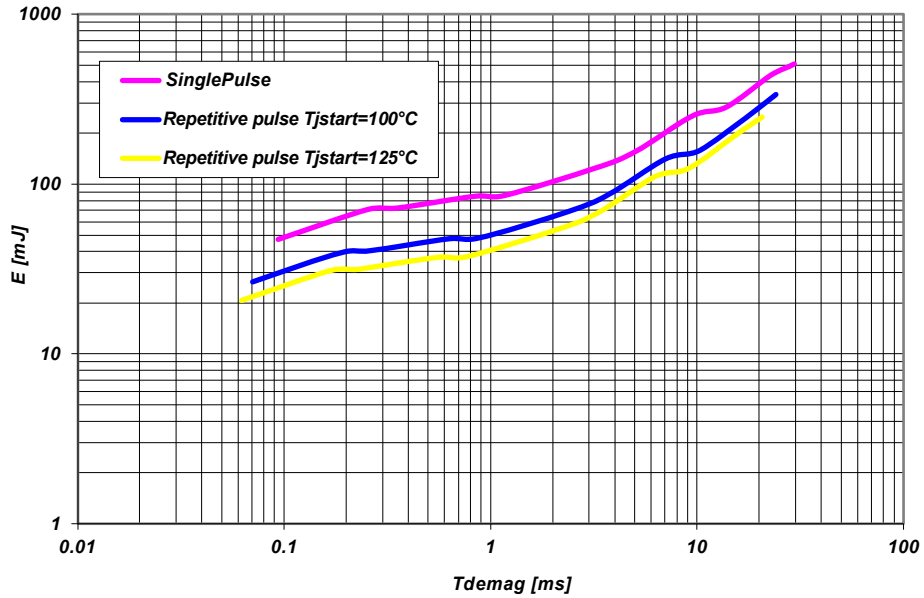


Figure 43. **Maximum Maximum turn off Energy versus Tdemag**



Note: Values are generated with RL = 0 Ω. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

6 Package and PCB thermal data

6.1 PowerSSO-16 thermal data

Figure 44. **PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)**

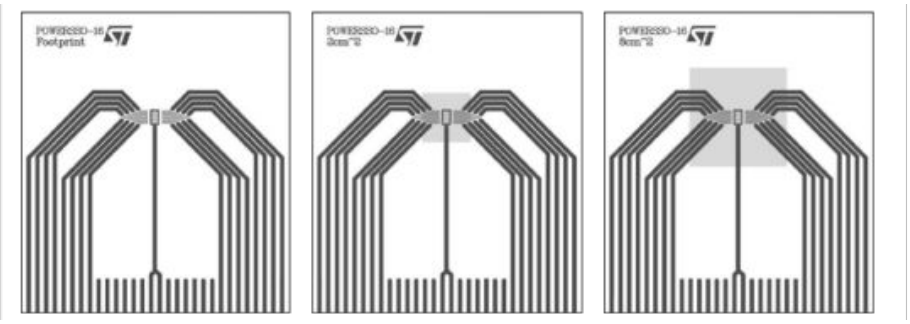


Figure 45. **PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)**

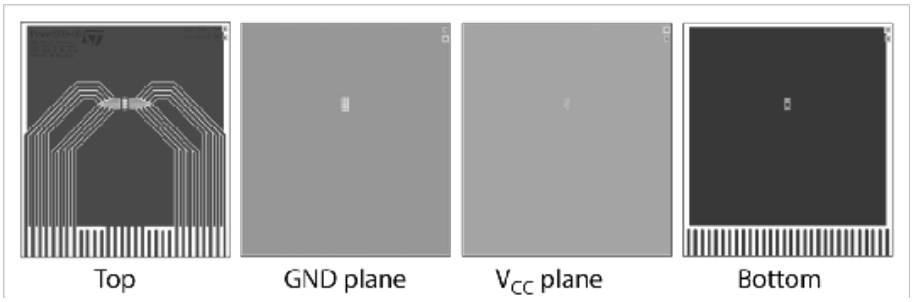


Table 15. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 46. **Rthj-amb vs PCB copper area in open box free air condition (one channel on)**

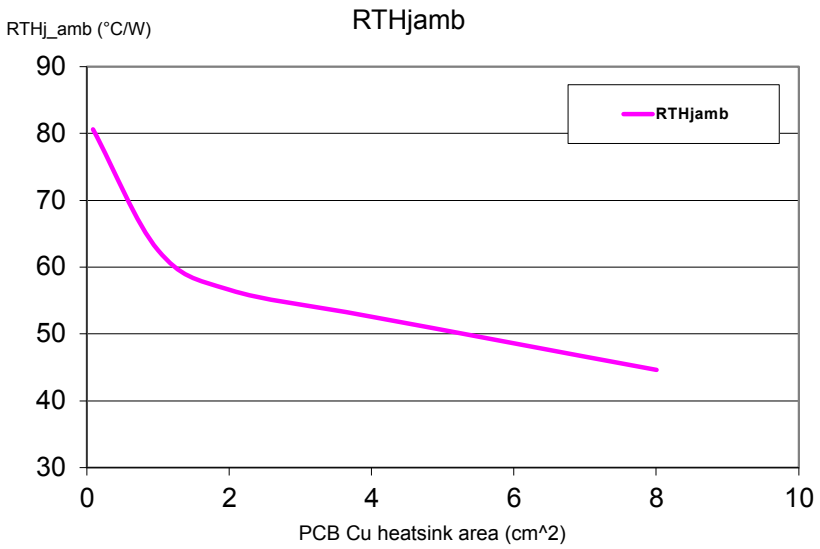
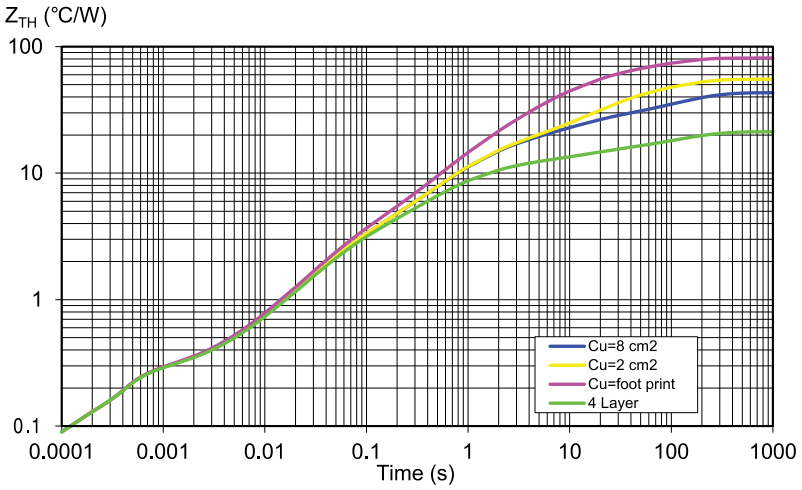


Figure 47. **PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)**

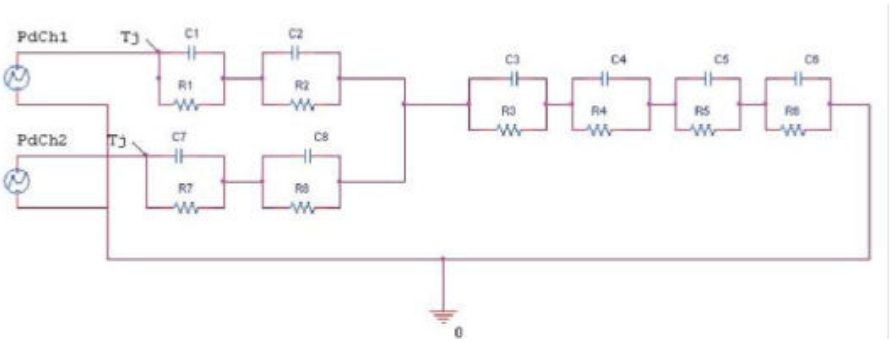


Equation: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta) \quad (3)$$

where δ = tP/T

Figure 48. **Thermal fitting model of a double-channel HSD in PowerSSO-16**



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. **Thermal parameters**

Area/island (cm^2)	Footprint	2	8	4L
R1 = R7 (°C/W)	0.25			
R2 = R8 (°C/W)	2			
R3 (°C/W)	7	7	7	5
R4 (°C/W)	16	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1 = C7 (W.s/°C)	0.001			
C2 = C8 (W.s/°C)	0.025			
C3 (W.s/°C)	0.1			
C4 (W.s/°C)	0.2	0.3	0.3	0.4
C5 (W.s/°C)	0.4	1	1	4
C6 (W.s/°C)	3	5	7	18

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-16 package information

Figure 49. PowerSSO-16 package dimensions (A)

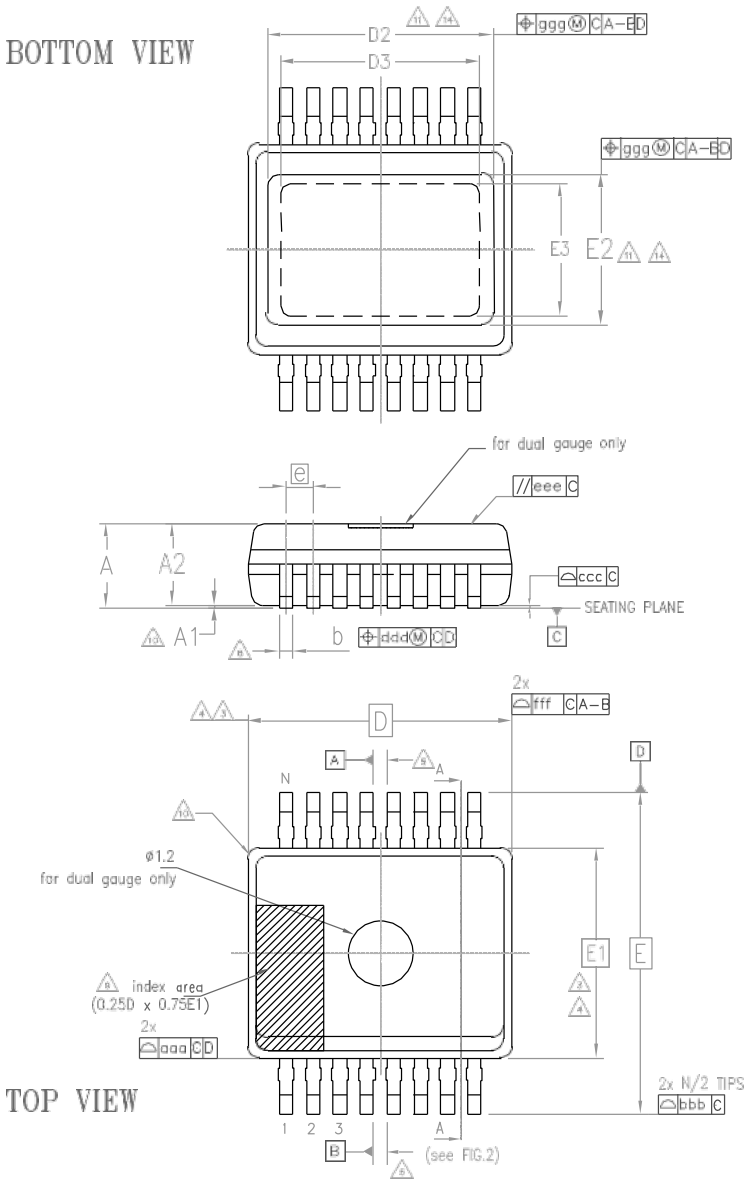


Figure 50. **PowerSSO-16 package dimensions (B)**

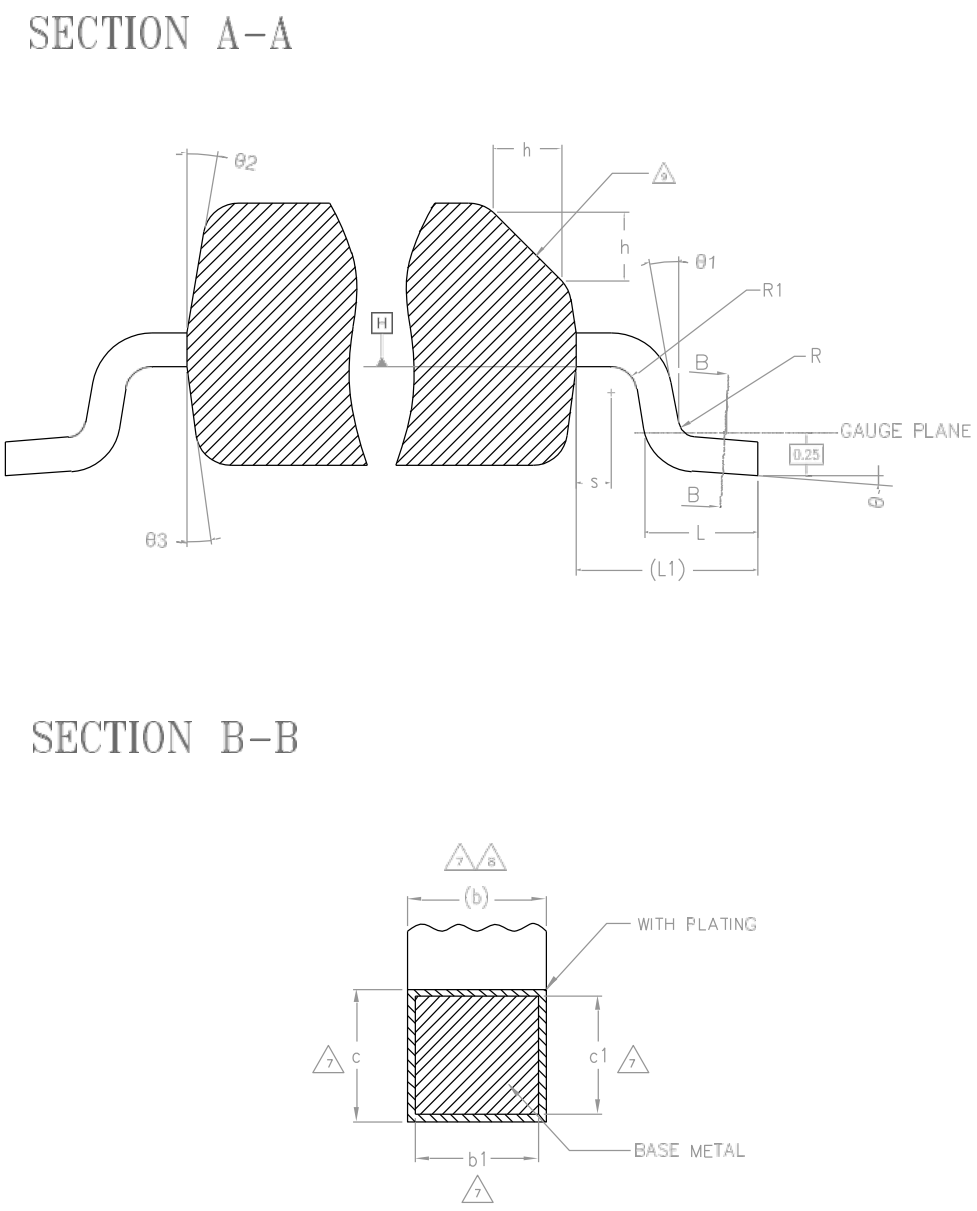


Table 17. PowerSSO-16 mechanical data

Symbol	Min.	Nom.	Max.	Note
Θ	0°	-	8°	
Θ1	0°	-	-	
Θ2	5°	-	15°	
Θ3	5°	-	15°	
A	-	-	1.70	
A1	0.00	-	0.10	10
A2	1.10	-	1.60	
b	0.20	-	0.30	7,8
b1	0.20	0.25	0.28	7,8
c	0.19	-	0.25	7
c1	0.19	0.20	0.23	7
D	4.90 BSC			3,4
D2	3.60	-	4.20	
D3	2.90	-	-	
e	0.50 BSC			
E	6.00 BSC			
E1	3.90 BSC			3,4
E2	1.90	-	2.50	
E3	1.20	-	-	
h	0.25	-	0.50	9
L	0.40	0.60	0.85	
L1	1.00 REF			
N	16	6		
R	0.07	-	-	
R1	0.07	-	-	
S	0.20	-	-	
Symbol	Tolerance of forrm and position			
	Databook			
aaa	0.10			
bbb	0.10			
ccc	0.08			
ddd	0.08			
eee	0.10			
ffff	0.10			
ggg	0.15			
NOTE	1,2			
REF				

7.2 PowerSSO-16 packing information

Figure 51. **PowerSSO-16 reel 13"**

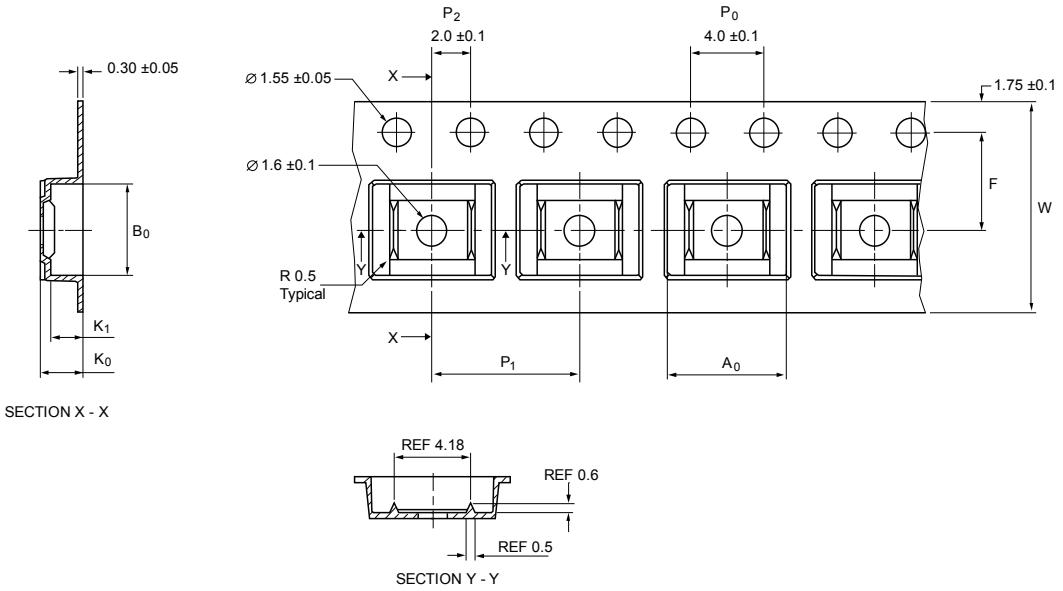


Table 18. **Reel dimensions**

Description	Value(1)
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. *All dimensions are in mm.*

Figure 52. **PowerSSO-16 carrier tape**

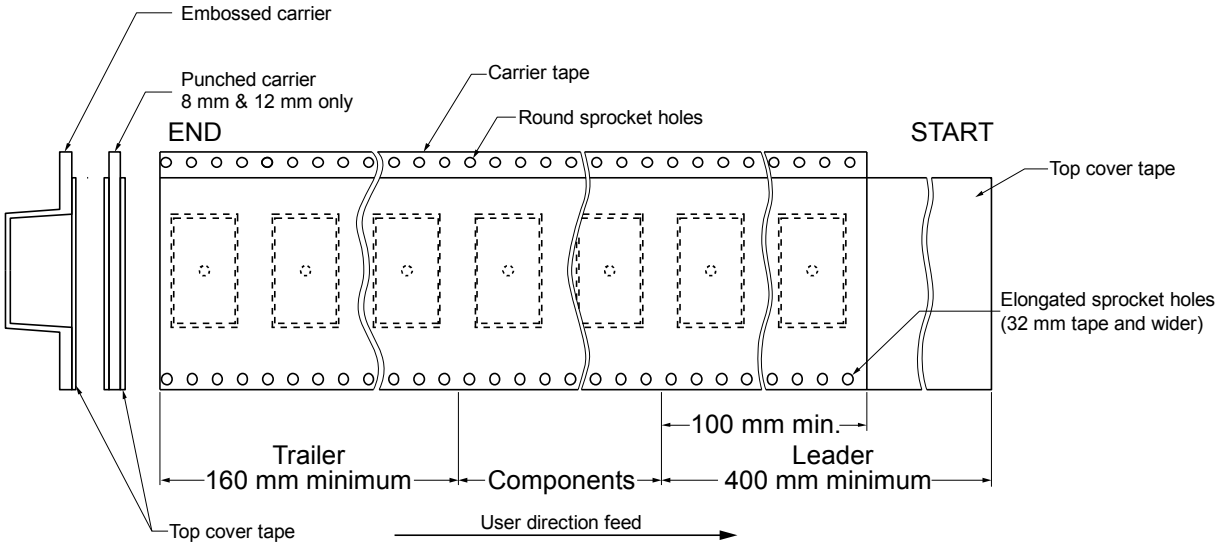
Table 19. **PowerSSO-16 carrier tape dimensions**

Description	Value(1)
A_0	6.50 ± 0.1
B_0	5.25 ± 0.1
K_0	2.10 ± 0.1
K_1	1.80 ± 0.1
F	5.50 ± 0.1

Description	Value(1)
P_1	8.00 ± 0.1
W	12.00 ± 0.3

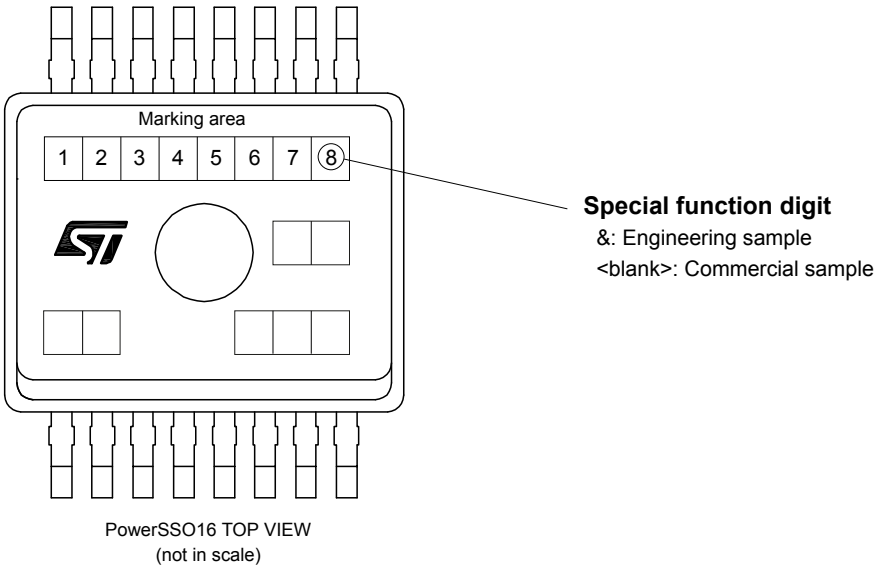
1. *All dimensions are in mm.*

Figure 53. PowerSSO-16 schematic drawing of leader and trailer tap



7.3 PowerSSO-16 marking information

Figure 54. PowerSSO-16 marking information



Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8 Order codes

Table 20. **Order codes**

Package	Order codes	
	Tube	Tape and reel
PowerSSO-16	—	VND7020AJTR

Revision history

Table 21. **Document revision history**

Date	Revision	Changes
04-Feb-2015	1	Initial release.
25-Oct-2017	2	Added *Section 7.2: "PowerSSO-16 packing information"* and *Section 7.3: "PowerSSO-16 marking information"*; Feature "AEC-Q100 qualified" and automotive icon added on cover page.
17-Oct-2025	3	Updated Section 7.1 and Section 7.2

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.