DT0138
Design tip

High voltage startup booster

A design tip is a description of an application oriented, technical implementation that leads to a specific benefit. For more information or support, visit www.st.com

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Main components	
STNRG011	Digital combo multi-mode PFC and time-shift LLC resonant controller

Purpose and benefits

This Design Tip describes an external circuit enabled to reduce the start-up time of an application based on the STNRG011 (or other devices including a compatible High Voltage startup). The STNRG011 digital combo is a PFC + LLC digital controller that allows the design of a high efficiency SMPS with the minimum component count.

1. As described in Section 2.3 of AN5118, the total start-up time (from AC main applied to the LLC soft-start ends) is composed of 4 main phases:
2. Turning on the device. As soon as the mains is applied, the STNRG011, thanks to the internal High Voltage Start up circuit, starts sinking current from the VAC pin, charging the VCC capacitor up to 17 V. When the VCC voltage reaches the 17 V (VccOn threshold) the device turns on.
3. Synchronization. After the VCC reaches the 17 V, the device requires at least 1 complete mains cycle to perform the MCC synchronization. After that, the device turns on at the estimated peak of the mains voltage and at the falling edge of the internal MCC line comparator (i.e. at about 135° of the sinusoidal voltage), in order to estimate the resonance period of the PFC boost section for the TM and valleys skipping operation.
4. PFC soft-start. The PFC soft-start begins at the next mains estimated zero crossing, with a fixed power set by the “PFC pss” parameter. The PFC soft-start ends when the PFC reaches the value set by the NVM with the parameter “PFC Vout SS end (delta)”.
5. LLC soft-start. The LLC soft-start begins only at the next mains estimated zero crossing, until the output voltage reaches the regulation. The LLC soft-start ends when the LLC feedback reaches the steady-state condition.

This document describes a circuit in order to reduce the phase number 1 of the startup of the STNRG011.

Description

The main goal is to help the device to charge the VCC with an external circuit. The standard circuit for VCC management is as follows (please see the AN5118):

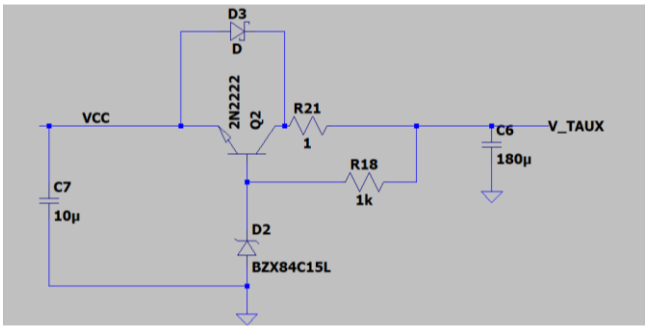

Figure 1 – VCC management standard circuit

There are 4 main elements in this circuit:

- VCC cap (small cap about 10 uF)
- V_TAUX (big cap about 180 uF)
- Linear composed by Q2, D2 and R18
- D3

Booster Implementation

The start-up booster is based only on 1 BJT and 3 resistor SMD 1206; The circuit can be seen in the following Figure:

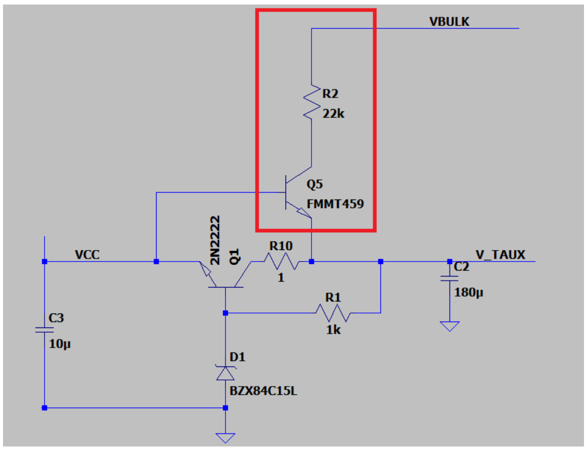

Figure 2 – Start-up booster into the red box

As can be seen in the red box, the circuit is based on BJT and resistor (just 1 in simulation, in the real application more than one is needed, especially for maximum voltage on SMD 1206 resistor). Moreover, D3 is removed.

At the beginning, the STNRG011 supplies current from the VCC pin; this current is divided into base current (in order to activate the BJT) and C3 charge current. The current to charge the big cap C2 is supplied from the BULK when the Q5 is activated plus the base current from the device. The design of the circuit is simple, but the user has to take some limitations into account:

- There is a maximum value of C3 that can be used. In particular: Considering a minimum beta of 50 and 20 mA as current from bulk, the required current on base could be approximated as:

$$I_{base} = \frac{I_{chargeC2}}{\beta_{min}} = 0.4mA$$

  So the current to charge C3 can be considered as:

$$I_{c3} = I_{VCC\_device} - I_{base} = 6mA - 0.4mA = 5.6mA$$

  And so the maximum C3 can be calculated as:

$$C_{3max} = \frac{C_2 \times I_{chargeC2}}{I_{C3}} \approx 50.4\mu F$$

- The Emitter-base breakdown voltage limits the maximum value of Auxiliary voltage.

Simulation

In order to analyze the circuit, a simulation is implemented with the following circuit (LTSPICE simulation):

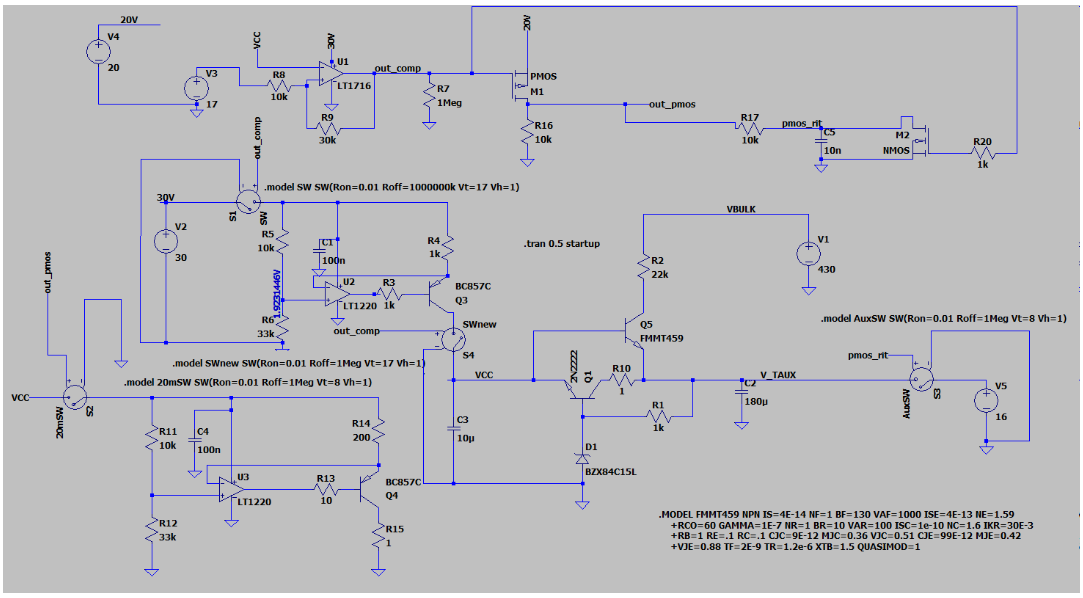

Figure 3 – Simulation schematic

The simulation, in addition to the components shown in Figure 2, includes also a state machine able to implement the startup of the device, i.e. when the VCC is above 17 V the HVSU is turned off, the FW of STNRG011 starts to elaborate so there is current consumption from the VCC pin (from S2 to Q4 circuit); moreover, the S3 is used as fixed voltage from auxiliary winding.

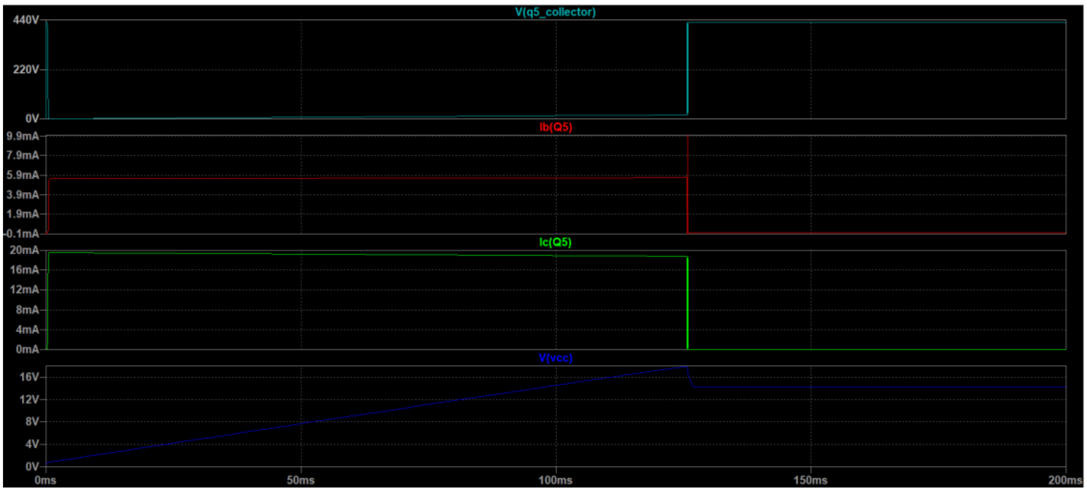

Figure 4 – Simulation result C3 10uF

The start-up time is about 125 ms considering 180 uF and 10 uF for C2 and C3 respectively. In this simulation the current from HVSU is about 7 mA (a little bit more with respect to the real case). The C3 is below the minimum for work in the desired area. In case it is increased up to 80 uF:

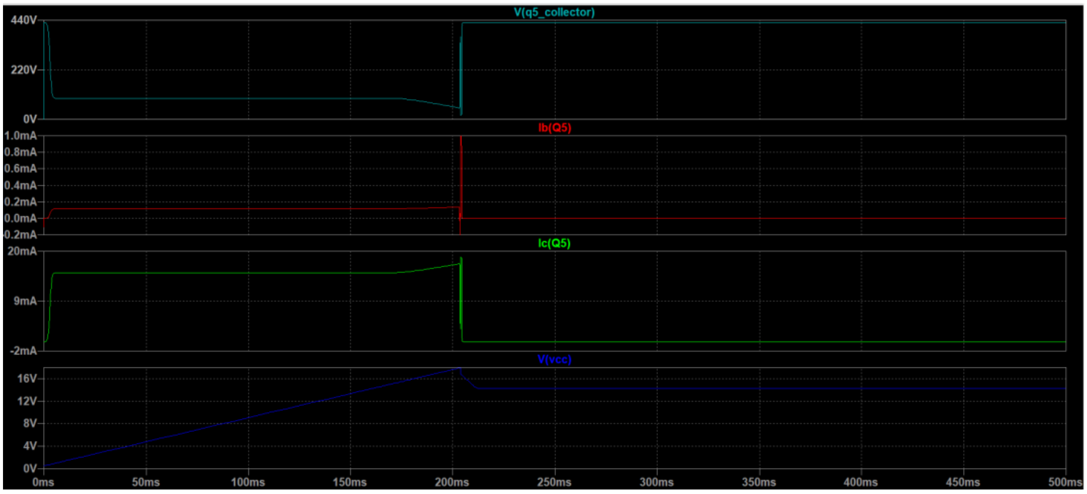

Figure 5 – Simulation result C3 80uF

In the latter case the current from HVSU is used to charge the C3 and not to set the BJT in the saturation area. In this case the start-up time is increased and the power is dissipated on BJT also for the high voltage across it.

Test on board

The circuit is implemented on board with the 150 W STNRG011 adapter. The VCC circuit is as follows:

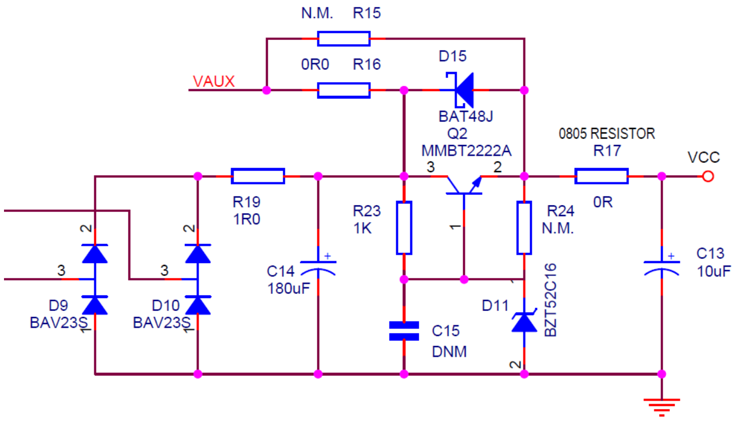

Figure 6 – 150W adapter VCC circuit

The following figure shows the actual start up time for 90 Vac full load:

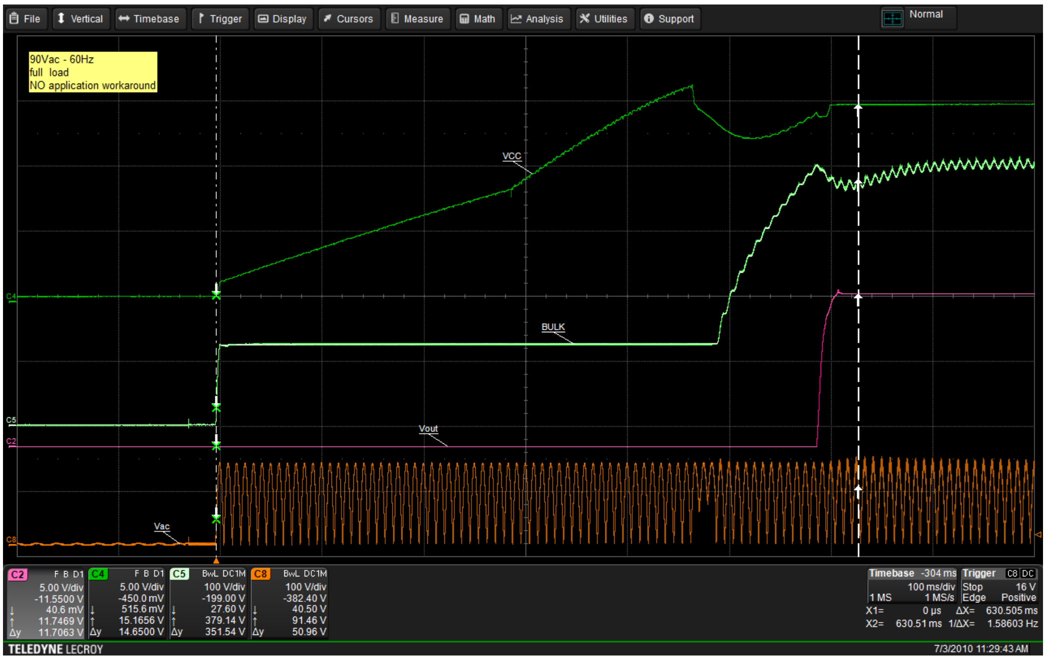

Figure 7 - 90Vac 60Hz full load startup with NO start-up booster

The following figure shows the startup with start-up booster for 90 Vac full load:

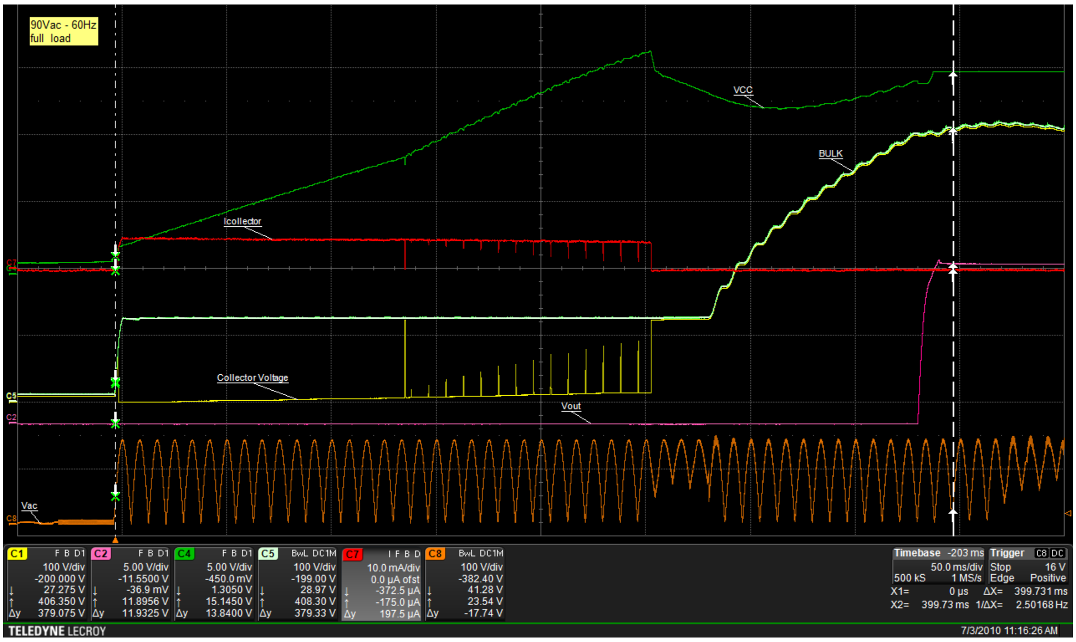

Figure 8 – 90Vac 60Hz full load startup with start-up booster

As can be seen, the total start-up time is about 400 ms; the peak on the collector voltage is related to the turn-on of VCORE so the base is turned off. The current from Bulk is about 5 mA, which can be increased a little bit, but it is important to take into account the power dissipation on resistors working at maximum bulk voltage.

In case the BJT is connected on bulk, the start-up booster is independent from the type of input, AC or DC (please consider the STNRG011 is not able to manage the DC input voltage).

Table 1 – Start-up time (VCC from 0V to 17V), booster present

Input AC [V]	VCC from 0V to 17V [ms]
90	271
115	249
230	169

Table 2 – Start-up time (VCC from 0V to 17V), booster not present[1]

Input AC [V]	VCC from 0V to 17V [ms]
90	500
115	500
230	512

[1] The board used a 1N4148 instead of BAT48J for D15 in adapter 150W board.

As can be seen, the start-up time in the case 230 Vac with booster not present is 512 ms, instead of 169 ms when booster is present.

Components characteristic

- Resistors

The resistors are able to manage up to maximum Bulk voltage and withstand the energy dissipated during the charge pulse.

An example can be 3 1206 high pulse withstanding resistors.

- NPN BJT

The main characteristics of this component are:

- Collector emitter breakdown voltage (V_{CEB})
- Emitter base breakdown voltage (V_{EBB}) is more than:
  Maximum voltage from Auxiliary winding – VCC after linear regulator

For example, the STM BJT STR1550, SOT23 has:

- V_{CEB} = 500 V (min.)
- V_{EBB} = 12 V (min.)

The cost of this component is very low.

If the drop on the regulator is higher than V_{EBB}, an extra diode can be added in series with the base.

Support material

Documentation
Datasheet STNRG011, Digital combo multi-mode PFC and time-shift LLC resonant controller
Application note, AN5118, 12 V – 150 W power supply based on STNRG011 digital combo and SRK2001 adaptive synchronous rectifier controller

Revision history

Date	Version	Changes
10-Aug-2020	1	Initial release