DT0144
Design tip

THD improvement at light-load in applications using STCMB1

***A design tip** is a description of an application oriented, technical implementation that leads to a specific benefit. For more information or support, visit www.st.com*

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Main components	
STCMB1	TM PFC with X-cap discharge and LLC resonant combo controller

Purpose and benefits

This design tip provides a simple modification with respect to the standard reference schematic based on the STCMB1 device, aimed to minimize the input current Total Harmonic Distortion (THD) down to 25% of full load.

The main purpose is to maximize the load range with low input current THD, making the AC/DC converters based on the STCMB1 capable of covering the latest LED lighting market requirements.

Description

The main change is an optimization of the control method of the PFC section (constant on-time control) adding a simple circuit composed by one Resistor and one Diode (RD circuit), which allows to reduce the burst-mode threshold intervention while keeping the best performance in terms of THD.

The suggested circuit can be also easily applied to the existing STCMB1 development kits (the formula is provided to design the suggested RD circuit).

Figure 1 shows the suggested RD circuit: an R_G resistor is connected between the current sense pin of the PFC section (ISEN_PFC pin) and the auxiliary winding of the PFC choke through a D_G diode. As a consequence, a current proportional to the instantaneous input voltage V_{IN} during the power switch on-time is sunk from the current sense ISEN_PFC pin, modulating the THD optimizer threshold (see STCMB1 datasheet, Section 7.6, where the THD optimizer threshold -preset I_{Lth} value- is constant).

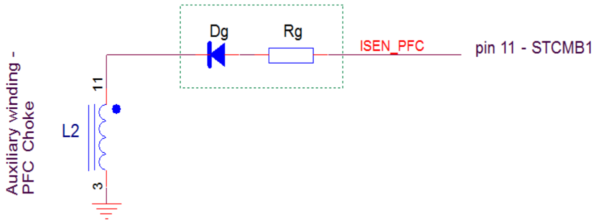

Figure 1. Suggested circuit diagram inside the green dotted line box.

As demonstrated in the following mathematical steps, this modulation improves the constant on-time control of the PFC converter, reducing the burst-mode threshold intervention but keeping the best performance in terms of THD.

Referring to the STCMB1 datasheet, equation 3 in Section 7.6 provides the analytic expression of the input current for a standard constant on-time control (COT), which is equal to the average value of the inductor current in a switching cycle:

$$I_{IN}(\theta) = \langle I_L \rangle = \frac{1}{2}\left(I_{Lvy} + I_{Lpk}\right) = \frac{V_{in\_pk} \sin\theta}{2L} T_{ON} + \sqrt{\frac{C_{drain}}{L}} V_{in\_pk} \sin\theta - \sqrt{\frac{C_{drain}}{L}} V_{out} \ . \qquad (1)$$

where L is the PFC choke and $Y_L = \sqrt{C_{drain} / L}$ is the admittance of the parasitic resonant tank.

The STCMB1 embeds a proprietary ECOT control, which activates the timer that sets the power switch on-time (T_{ON_C}) once the inductor current reaches a preset I_{Lth}, comparing the ISEN_PFC pin voltage with an internal $V_{ISEN\_PFC\_Z}$ fixed threshold.

Designing the I_{Lth} inductor preset value equal to the terms $\sqrt{\frac{C_{drain}}{L}} V_{out}$, the input current results:

$$I_{IN}(\theta) = \langle I_L \rangle = \frac{1}{2}\left(I_{Lvy} + I_{Lpk}\right) = \frac{1}{2}\left(\frac{1}{L} T_{ON\_C} + \sqrt{\frac{C_{drain}}{L}}\right) V_{in\_pk} \sin\theta \ . \qquad (2)$$

Assuming a narrow control loop bandwidth, like in any high-PF converter, the T_{ON_C} is constant along a line half-cycle. Therefore, the previous equation shows that the control on-time method (ECOT) achieves sinusoidal input current.

By averaging the product of $I_{IN}(\theta)$ given by (2), by the instantaneous line voltage $V_{IN}(\theta) = V_{in\_pk} \sin\theta$ over a line half-cycle, it is possible to find the DC input power P_{IN} to the converter:

$$P_{IN} = \frac{V_{in\_pk}^2}{4}\left(\frac{T_{ON\_C}}{L} + Y_L\right) . \qquad (3)$$

Now considering the efficiency η of the PFC converter, the output power P_{OUT} results:

$$P_{OUT} = \eta P_{IN} = \eta \frac{V_{in,pk}^2}{4}\left(\frac{T_{ON\_C}}{L} + Y_L\right) . \qquad (4)$$

The previous equation shows that the PFC converter gives a minimum output power, even in the ideal case where the on-time control loop T_{ON_C}=0:

$$P_{OUT\_MIN\_IDEAL} = \eta \frac{V_{in,pk}^2}{4} Y_L \ . \qquad (5)$$

Considering a minimum on-time T_{ON_MIN} (sum of the STCMB1 delay to output $td_{(H-L)}$ and the power switch off-time td_{OFF}), the minimum output power results:

$$P_{OUT\_MIN} = \eta \frac{V_{in,pk}^2}{4}\left(\frac{T_{ON\_MIN}}{L} + Y_L\right) \ . \qquad (6)$$

If the power requested by the PFC load is lower than (6) the PFC converter enters into burst-mode, to keep the output voltage regulation, much increasing the THD.

Considering the suggested RD circuit, the current sunk from the ISEN_PFC pin is:

$$I_G(\theta) = \frac{V_{IN}(\theta)}{m} \frac{1}{R_G} , \qquad (7)$$

where m is the primary-to-auxiliary turns ratio ($m = N_P / N_{AUX}$) of the PFC choke.

As a consequence, the I_{ROS} current flowing in the R_{OS} resistor results:

$$I_{ROS}(\theta) = I_{OS} - I_G(\theta) = I_{OS} - \frac{V_{IN}(\theta)}{m}\frac{1}{R_G}, \tag{8}$$

where I_{OS} is the constant current sourced from the ISEN_PFC pin (I_{OS}=50 µA typ., see STCMB1 datasheet). The resulting ISEN_PFC pin voltage is:

$$V_{ISEN\_PFC}(\theta) = -R_S I_L(\theta) + R_{OS} I_{ROS}, \tag{9}$$

where R_S is the PFC current sense resistor.

Replacing (8) in (9) and considering that the device activates the timer that sets the power switch on-time (T_{ON_C}) once the ISEN_PFC pin voltage reaches the $V_{ISEN\_PFC\_Z}$ internal fixed threshold ($V_{ISEN\_PFC\_Z}$ =-25 mV typ., see datasheet), the I_{Lth} preset inductor value results:

$$I_{Lth}(\theta) = \left(\frac{|V_{ISEN\_PFC\_Z}| + R_{OS} I_{OS}}{R_S}\right) - \left(\frac{V_{IN}(\theta) R_{OS}}{m}\frac{1}{R_G R_S}\right). \tag{10}$$

It is worth noting that the I_{Lth} inductor preset value is not constant and is composed by two terms: the first term is constant, and the second term depends on the input voltage.

Selecting the I_{Lth} preset value equal to $\sqrt{\frac{C_{drain}}{L}} V_{out} - \sqrt{\frac{C_{drain}}{L}} V_{in\_pk} \sin\theta$, after some simple calculations the (1) results:

$$I_{IN}(\theta) = \langle I_L \rangle = \frac{1}{2}\left(\frac{1}{L} T_{ON\_C}\right) V_{in,pk} \sin\theta \tag{11}$$

which is still sinusoidal as in (1).

Considering (11), as done in (3), the output power P_{OUT} results:

$$P_{OUT} = \eta \frac{V_{IN,pk}^2}{4}\left(\frac{T_{ON\_C}}{L}\right). \tag{12}$$

The previous equations show that with the suggested RD circuit that the input current is sinusoidal, but the minimum output power can be zero in the ideal case (T_{ON_C}=0). This permits to maximize the load range with low input current THD (no burst-mode intervention).

Considering (10) and the desired inductor preset value $\sqrt{\frac{C_{drain}}{L}} V_{out} - \sqrt{\frac{C_{drain}}{L}} V_{in\_pk} \sin\theta$, after some simple mathematical steps, results:

$$R_{OS} = \frac{R_S\, V_{out}\sqrt{C_{drain}/L} \; - |V_{ISEN\_PFC\_Z}|}{I_{OS}} \tag{13}$$

which is the same formula reported in the STCMB1 datasheet (the suggested RD circuit does not influence the design of the R_{OS}) and:

$$R_G = \frac{R_{OS}}{m\, R_S}\frac{1}{\sqrt{C_{drain}/L}} \tag{14}$$

It is worth noting that the suggested R_G resistor depends on the equivalent capacitance afferent to the switching node, which is mainly composed by the sum of the parasitic capacitance associated to the MOSFET and the added capacitor between drain to ground, so some fine-tuning on the real application could be needed.

Test results

The effectiveness of the proposed RD circuitry has been validated on a 150 W dimmable LED driver, where the main characteristics of the whole AC/DC converter and the PFC power section are reported in table 1. Applying the formula (14), the suggested R_G resistor results:

$$R_G = \frac{R_{OS}}{m\,R_S}\frac{1}{\sqrt{C_{drain}/L}} = \frac{470}{10\cdot 0.082}\frac{1}{\sqrt{720\cdot 10^{-12}/310\cdot 10^{-6}}} = 376k\Omega$$

AC/DC LED driver - parameter	**Symbol**	**Value**	**Unit**
Line voltage range	V_{IN}	90 - 265	Vac
Line frequency range	f_{line}	47 - 63	Hz
Regulated output current	I_{LED}	0.05 to 1	A
Rated output voltage	V_{LED}	150	V
PFC section - parameter			
Regulated output voltage	V_{OUT_PFC}	400	V
Inductance	L	310	µH
Inductor turns-ratio	$m = N_P / N_{AUX}$	10	-
Current sense resistor	R_S	0.082	Ω
Current sense offset resistor	R_{OS}	470	Ω
Equivalent drain capacitor (parasitic + external)	C_{DRAIN}	250+470	pF

Table 1. Main characteristic of the 150 W LED driver converter.

Figure 2 shows the THD comparison between the original board (dark) and the modified board (green) **adding the optimized RD circuit (R_G = 300 kΩ, D_G = 1N4148)**, versus output power.

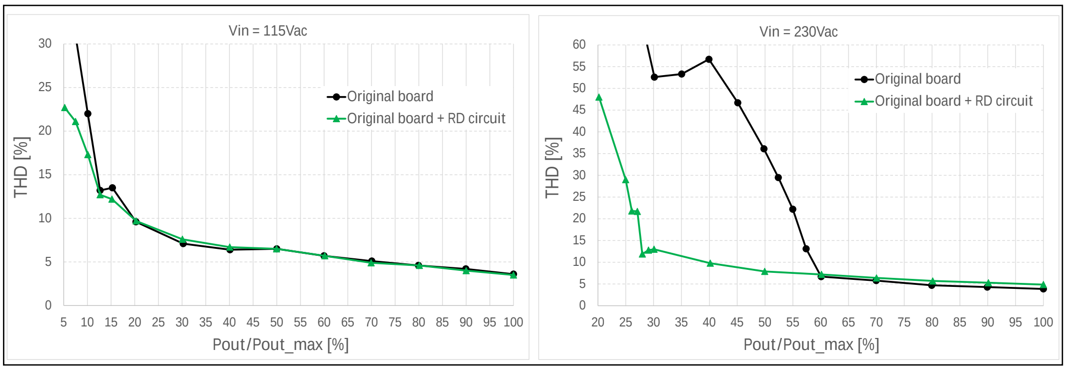

Figure 2. THD comparison adding the optimized RD circuit.

It is evident the huge improvement of the THD at high line. Basically, the burst-mode intervention is reduced from around 60% to around 25% of the load.

The following images show the Power Factor (PF) comparison results.

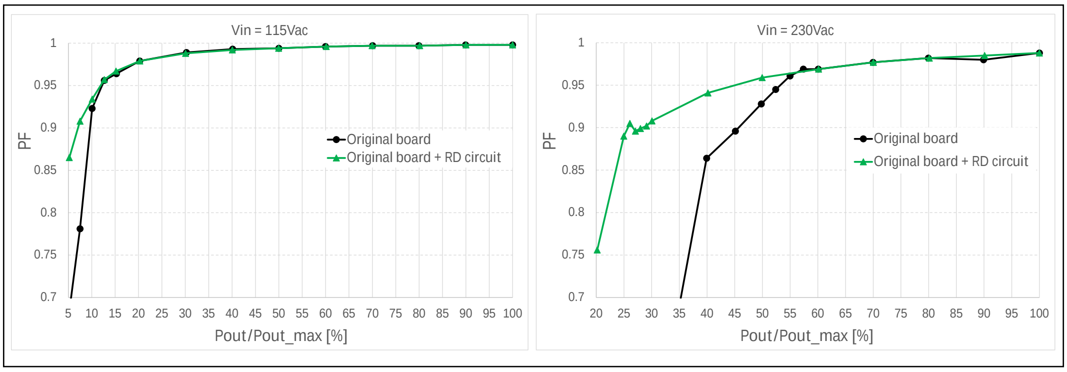

Figure 3. PF comparison adding the optimized RD circuit.

Note: PFC choke value impacts and suggestion

Equations (6) and (12) show that the minimum output power of the PFC converter depends also on the PFC choke value L: the higher the inductor value, the lower the minimum output power.

Considering (12) and indicating the desired burst-mode threshold intervention as a percentage of the maximum output power, results:

$$BM[\%] = \frac{P_{OUT\_MIN}}{P_{OUT\_MAX}}100 = \eta \frac{V_{IN,pk}^{2}}{4}\left(\frac{T_{ON\_MIN}}{L}\right)\frac{1}{P_{OUT\_MAX}}100 \quad (15)$$

For example, considering a minimum on-time of 420 ns ($td_{(H\text{-}L)}$=220 ns, td_{OFF}=200 ns), figure 4 shows the burst-mode threshold versus the PFC choke value.

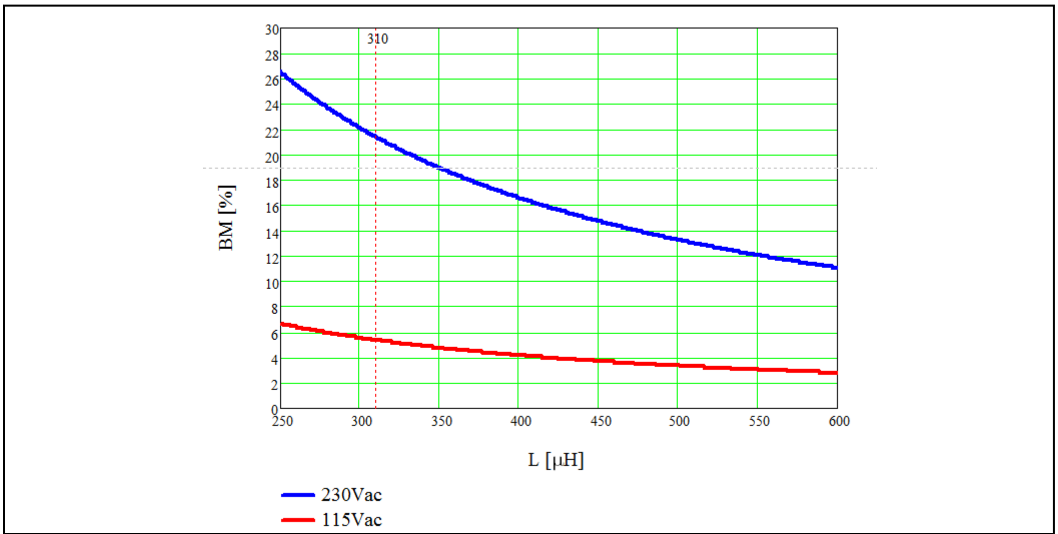

Figure 4. Burst-mode threshold (BM) versus PFC choke value (L).

Finally, solving (15) for the PFC choke value, it is possible to find an estimate of the required inductor value to obtain the desired burst-mode threshold:

$$L_{BM} = \left(\eta \frac{V_{IN,pk}^{2}\ T_{ON\_MIN}}{4}\right) \frac{1}{P_{OUT\_MAX} BM[\%]} 100 \qquad (16)$$

Support material

Documentation
Datasheet, STCMB1 - TM PFC with X-cap discharge and LLC resonant combo controller

Revision history

Date	Version	Changes
01-Dec-2021	1	Initial release.