PM8803/03C design tip: T2P issue with certain PSE

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Main components	
PM8803	PM8803 datasheet
PM8803C	PM8803C datasheet

Purpose and benefits

This Design tip describes how to improve PM8803/03C behavior that in some applicative cases was found marginal.

Description of the issue

An interoperability shortcoming may be discovered when connecting a Class 4 PD designed with PM8803/03C with certain PSE; just to mention one of the most popular switches for enterprise applications: Cisco Catalyst 3750E is one of those. This short application note tries to explain how the issue can be observed and describes an applicative solution to solve it.

PM8803/03C has a pin (T2P) which is dedicated to indicate the successful connection with a "Type 2 PSE" i.e. when 2-event classification is detected. For old generation devices the T2P pin has a logic level high after turn-on while it is low when connected to a PSE doing 2-event classification.

The mentioned Catalyst switch performs multiple cycles of detection/classification before powering the port. Classification is done with one event, relying on LLDP to further negotiate the power to be allocated.

The following figures show that despite classification being done with one event the T2P signal remains low after power-on, indicating an erroneous detection of a Type 2 PSE. The value of the T2P signal is also observed to be dependent on the port of the above mentioned switch: connection with some ports of the switch provide always good discovery (T2P high) while others have a variable rate of erroneous detection with successive connection / disconnection attempts.

The phenomena

The phenomena comes at the turn-on, no matter what happens before (during the n cycles of detection + classification repeated every 500 ms). While the Vport of the switch is not loaded, it rises monotonically.

However, it appears that if a PD applies 40 mA of classification current at the classification threshold (approximately between 11 V to 13 V), the switch goes into current limitation and consequently the voltage has the observed negative slope.

Figure 1. T2P not asserted. Note the VDD rise that is monotonic. This picture is obtained removing the classification resistance

Figure 2. Same PD with Class 4: The T2P is asserted. Note the VDD rise that is not monotonic, but has for two times a negative slope, clear indication that the switch port is in current limitation.
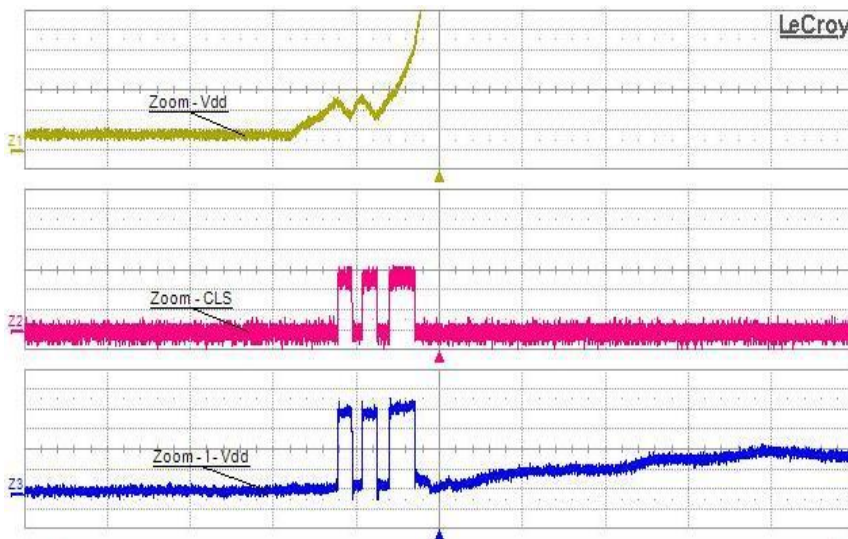

Figure 3. T2P asserted. Note the VDD rise that is not monotonic;

Note also that the two-time negative slopes are coincident with the 40 mA classification pulses

The switch at turn-on must change its current limit values to adapt them to the different ranges of the output voltage during turn-on, as requested by the IEEE802.3at standard; The IEEE802.3at-2009 standard states:

The IEEE802.3at 2009 standard say:

The PSE shall limit the maximum current sourced at the PI during POWER_UP. The maximum inrush current sourced by the PSE shall not exceed the PSE inrush template in Figure 33–13.

a) During POWER_UP, for PI voltages between 0 V and 10 V, the minimum I_{Inrush} requirement is 5 mA.
b) During POWER_UP, for PI voltages between 10 V and 30 V, the minimum I_{Inrush} requirement is 60 mA.
c) During POWER_UP, for PI voltages above 30 V, the minimum I_{Inrush} requirement is as specified in Table 33–11.

Please note that nothing is said about the timing to set the different limit in current.

To rephrase the previous description, it seems like the switch at the turn-on dynamically goes out of spec, because when it reaches the classification voltage range it is not able at the same time to sustain a 40 mA classification pulse.

- One way to overcome this "marginality" is to wait until the switch is ready to support the 40 mA classification pulse

- From the measure done on a single 24-port switch this delay is between 100 and 150 us, but it has been observed that each port behaves differently from the other ones

- PM8803C has an internal delay on the settling time of the classification current of about 10us, not enough for this specific application

- A simple circuit allows to increase the settling time at about 300 us, a safe delay for all the ports
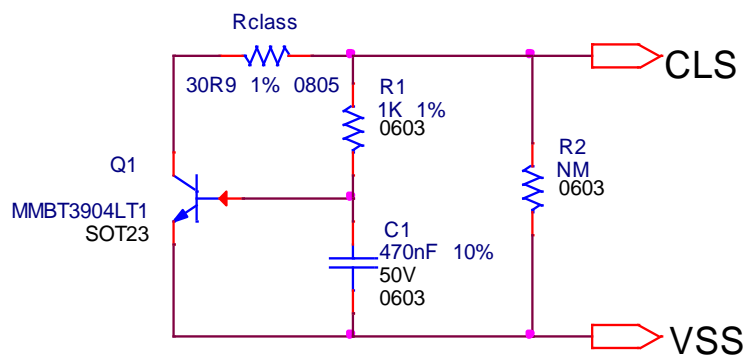
The described circuit applies only for Class 4 PDs with the highest classification current.
For Classes 0 to 3, covered by the old standard IEEE802.3af, with lower classification current and where the T2P signal is not foreseen, in those applications it could be not used.

The classification resistance must be reduced to consider the contribution of the transistor and has been found that a good value, also over a temperature range of -40 to 85 C, is 30.9 ohm, 1%.

The following table shows the delay as function of the capacitance C1.

Capacitor	Time Constant	Delay Calculated	Delay Measured
220nF	220us	133us	135us
330nF	330us	200us	210us
470nF	470us	285us	300us

The following image shows the delay of about 300 uS at Tamb with C1=470 nF.
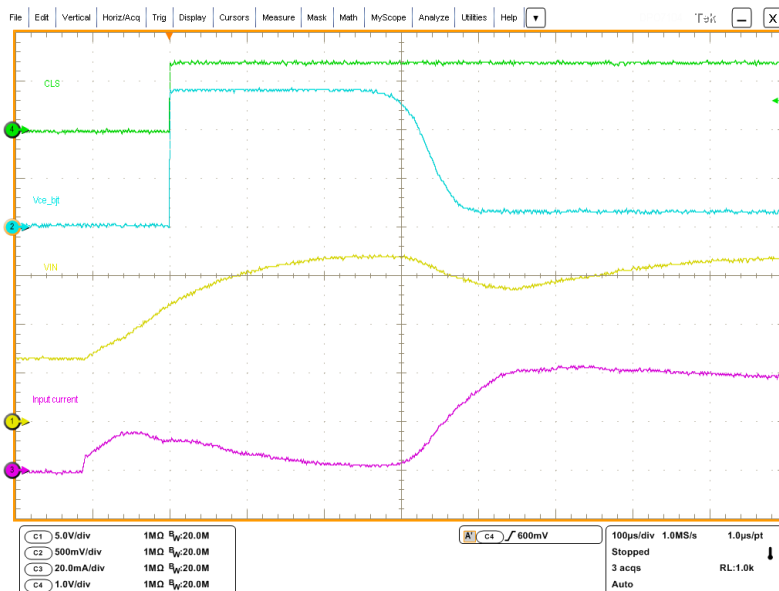
Ch1 (yellow trace)   Input voltage VIN
Ch2 (blue trace)   BJT Vce
Ch3 (pink trace)   Input current
Ch4 (green trace)   CLS voltage

Conclusions

A simple circuit allows to set a delay on the classification current of PM8803/03C that permits a proper set-up of the current limitation of some switch ports as function of its output voltage.

As an example, with reference to the circuit schematic, a good combination of values to assure a delay of at least 300 uS is:

R1=1Kohm, 1%
C1=470nF, 10%, 10V, X5R   or better
Rc=30.9 ohm, 1%, 0805   for about 40 mA class current.

Thermal effects on the junction base-emitter of BJT have been estimated and measured with good agreement between estimated data and measured values.

Revision history

Date	Version	Changes
03-Dec-2021	Rev 1	Initial release.

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