

PM8803/03C design tip: how to solve a marginality of AT standard

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Main components	
PM8803	PM8803 datasheet
PM8803C	PM8803C datasheet

Purpose and benefits

This Design tip describes how to fix a PM8803/03C behavior that could be marginal in respect to the AT standard, and that sometimes leads to problems with the right interpretation of the PoE standards.

Description of the issue

A marginality issue has been discovered when connecting a PD designed with PM8803/03C with certain electronic systems.

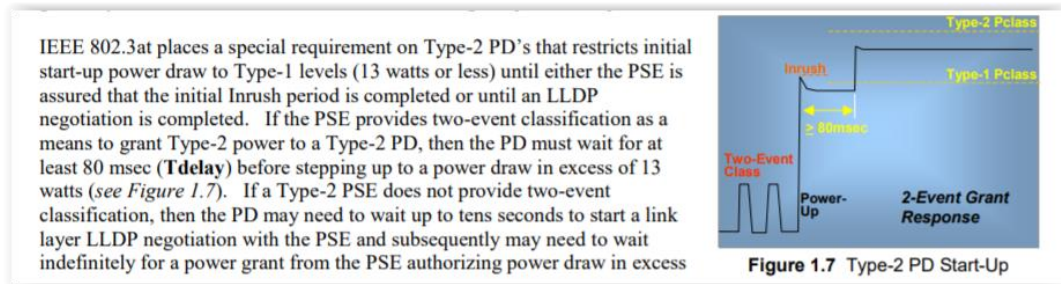
This short application note tries to explain how the issue can be observed and describes an applicative solution to solve it while making the whole system compliant with the AT standard.



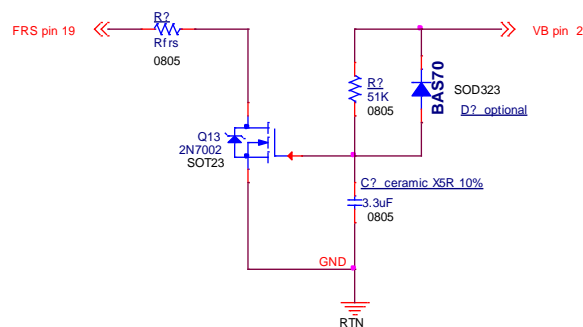
Figure 1. A PM8803 typical Tdelay: it is around 25 ms

The AT standard foreseen for a Type 2 PD, a two-step behavior of the powered electronic system; it is the PD as a whole system that must comply with the standard: to respect the **Tdelay** parameter it is enough having the electronics powered via PoE with an initial start-up operating condition requiring less than 13 W and waiting a time period of at least 80 msec before going into full load conditions (25.5 W). If this is the case the PM8803 /03C can be used as is, without any additional circuit.

Here a description of this parameter done by SIFOS in its PDA300 manual:



In some cases, the electronic powered via PoE cannot respect the two-step startup previously described, and therefore in that case the issue is observed. It is suggested to add the following circuit:



This circuit is based on the fact that the PM8803/03C do not work if there is no resistor connected from FRS to RTN pin; the start of operations can be delayed by means of a suitable selection of the R-C values that are used to drive the N-channel MOSFET.

VB is selected in place of VC because it is more accurate (+/-5%);
 VB is derived from VC and is soon made available (see image);
 The 2N7002 has a wide drift on the threshold of Vgs and this impacts on the estimation of the delay introduced.

Here are some example calculations:

- Typ. threshold 2N7002 = 2.0 V or 40% of 5 V
- Charging of a capacitor at 40% achieved at about 0.5 time constant
- We put 80 ms = 0.5 RC → assumed R = 51 k → C = (80 ms) / 0.5 x 51 k = 3.13 uF
- A standard value of 3.3 uF can be used

Use 1% resistor and 10% ceramic capacitor with a rated voltage at least 10 V.
 Discharge diode optional;

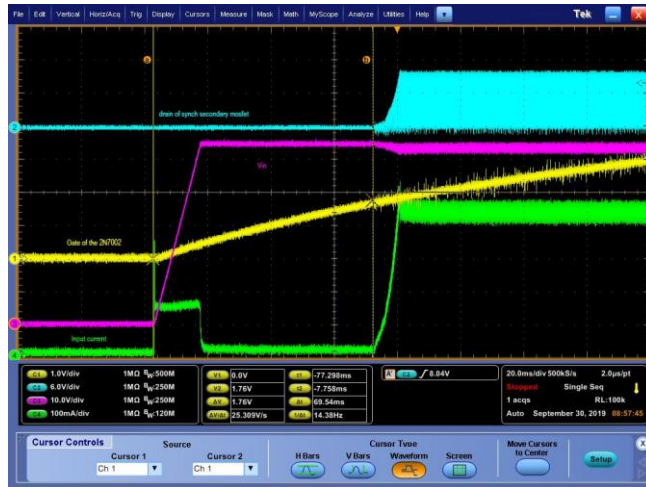


Figure 2. The behavior of PM8803/03C with the circuit shown before;

Now the Tdelay is about 70 msec and not the estimated 80 msec, because of a lower threshold of 2N7002: about 1.75 V in place of a typical 2.1 V as per the datasheet. Doing again the calculations with the measured values:

- Actual threshold 2N7002 = 1.75 V or about 35% of 5 V
- Charging of a capacitor at 35% achieved at about 0.4 time constant
- We put Delay = 0.4 RC → assumed R = 51 k → Delay = 0.40 x 51 k x 3.3 uF = 67 ms, consistent with the measured of about 70 ms.

Conclusions

This short report describes a simple circuit to be added to PM8803/03C that allows to extend the delay from the inrush phase to the DC/DC converter startup in order to meet the PoE.AT standard regarding the parameter **Tdelay**, it must be at least 80 ms.

Nevertheless, it is useful to remember here that it is the PD as a whole system that must comply with the AT standard: to respect the Tdelay parameter it is enough having the electronics powered via PoE with an initial startup requiring less than 13 W and waiting a time period of at least 80 msec before going into full load conditions (25.5 W). If that condition is satisfied the PM8803/03C can be used as is without the circuit described in this document.

Revision history

Date	Version	Changes
03-Dec-2021	Rev 1	Initial release.

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