DT0150
Design tip

Light-load THD improvement, in applications based on L6564 controller family

A design tip *is a description of an application oriented, technical implementation that leads to a specific benefit. For more information or support, visit www.st.com*

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Main components	
L6564	Transition-Mode PFC controller
L6564H	High voltage startup Transition-Mode PFC controller

Purpose and benefits

This design tip provides a simple modification with respect to the standard reference schematic based on L6564/L6564H, aimed to minimize the input current Total Harmonic Distortion (THD) also at light-load (e.g. down to 15-20% of full-load).

The main purpose is to maximize the load range with low input current THD, making the Power Factor Corrector (PFC) boost converters, based on the L6564 controller family, capable of covering the latest LED lighting markets requirements.

Description

The main change is an optimization of the control method of the PFC, adding a simple external circuit composed of a resistor (R_G), plus eventually the addition of an RC filter on the current sense pin, which allows to reduce the burst-mode threshold intervention but maintain the best performance in terms of THD.

The suggested circuit can be easily applied to all existing L6564/L6564H development kits, using the mathematical formula (12) to design the R_G resistor based on the specific application.

Figure 1 shows the typical PFC boost application schematic based on the L6564/L6564H device, with the suggested circuit highlighted in green: a resistor R_G is connected between the input voltage (across the C_{IN} capacitor after the bridge diode) and the current sense pin (CS) of the IC controller. As a consequence, a current proportional to the instantaneous input voltage $V_{IN}(\theta) = V_{in,pk}\, sin\, \theta$ is added to the current sense CS pin and through the external current sense filter resistor (R_{CS}) is converted into a voltage. This voltage is thus added to the inductor current information sensed through the external current sense resistor Rs in series to the power switch M.

As shown in the following mathematical steps, this modulation improves the control of the PFC converter reducing the burst-mode intervention threshold but keeping the best performance in terms of THD.

Referring to the L6564/L6564H datasheet and the following figure 1, where the main block of the peak-current mode control loop is highlighted, it is possible to express the internal current reference voltage $V_{CS\_REF}(\theta)$ as:

$$V_{CS\_REF}(\theta) = \frac{\sin\theta}{K_P\, V_{in,pk}}\, K_M\, V_C + V_{OFS}(\theta)\ , \tag{1}$$

where $K_P=R_2/R_1+R_2$ is the gain of the MULT partitioning resistors, K_M is the internal multiplier gain, V_C is the control-loop voltage (that is basically constant along a line half-cycle due to a narrow bandwidth, like in any high-Power Factor) and $V_{OFS}(\theta)$ is the voltage generated by the internal THD optimizer circuit.

Referring to the L6564/L6564H datasheet, section 6.4 and Table 4, the THD optimizer circuit generates a small offset near line zero-crossing to reduce the well-known dead-angle that increases the THD. In particular, the offset is not constant but, as shown in figure 1, has a sort of sinusoidal envelope to avoid distortion on the rest of the line period. Considering the typical value reported in the datasheet (Table 4, Vcs_{ofst} parameter), it is possible to express the internal voltage $V_{OFS}(\theta)$ with the following formula:

$$V_{OFS}(\theta) = K_{OFS}\left(V_{REF\_OFS} - K_P\, V_{in,pk}\, \sin\theta\right), \tag{2}$$

where K_{OFS} is 6.66 [mV] and V_{REF_OFS} is 6 [V].

Replacing (2) in (1), the programmed current reference voltage results:

$$V_{CS\_REF}(\theta) = \frac{\sin\theta}{K_P\, V_{in,pk}}\, K_M\, V_C + K_{OFS}\,(V_{REF\_OFS} - K_P\, V_{in,pk}\, \sin\theta). \tag{3}$$

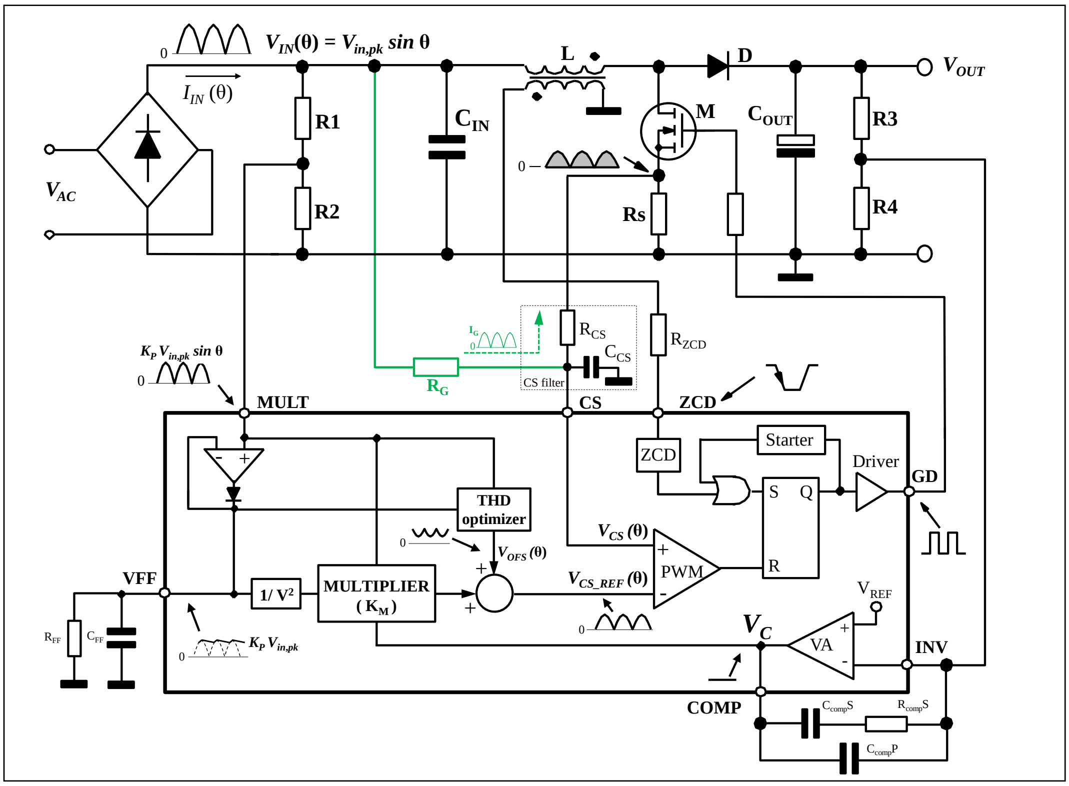

Figure 1. Typical L6564/L6564H PFC schematic with the suggested circuit highlighted.

The power switch M is turned off as soon as the CS pin voltage reaches the internal current reference $V_{CS\_REF}(\theta)$, thus, considering the standard control scheme (R_G resistor not mounted), the resulting inductor peak current is:

$$I_{L,pk}(\theta) = \frac{V_{CS\_REF}(\theta)}{R_S}, \qquad (4)$$

where R_S is the current sense resistor.

Considering that the converter operates in Transition-Mode (aka Quasi-Resonant mode), the input current $I_{IN}(\theta)$ (that is equal to the average value of the inductor current in a switching cycle) results:

$$I_{IN}(\theta) = \langle I_L \rangle = \frac{I_{L,pk}(\theta)}{2} = \frac{V_{CS\_REF}(\theta)}{2\,R_S}. \qquad (5)$$

Replacing (3) in (5), results:

$$I_{IN}(\theta) = \frac{K_M}{2\,R_S}\frac{\sin\theta}{K_P\,V_{in,pk}}V_C + \frac{V_{REF\_OFS}\,K_{OFS}}{2\,R_S} - \frac{K_{OFS}\,K_P}{2\,R_S}V_{in,pk}\sin\theta\,. \qquad (6)$$

By averaging the product of $I_{IN}(\theta)$ given by (6), with the instantaneous line voltage $V_{IN}(\theta) = V_{in\_pk}\sin\theta$ over a line half-cycle, it is possible to find the DC input power P_{IN} to the converter:

$$P_{IN} = \frac{K_M}{4\,K_P\,R_S}V_C + \frac{V_{REF\_OFS}\,K_{OFS}}{\pi\,R_S}V_{in,pk} - \frac{K_P\,K_{OFS}}{4\,R_S}V_{in,pk}^{\;2}. \qquad (7)$$

Now considering the efficiency η of the PFC converter, the output power P_{OUT} results:

$$P_{OUT} = \eta P_{IN} = \frac{\eta\,K_M}{4\,K_P\,R_S}V_C + \eta\frac{V_{in,pk}}{2\,R_S}K_{OFS}\left(\frac{2\,V_{REF\_OFS}}{\pi} - \frac{K_P}{2}V_{in,pk}\right). \qquad (8)$$

The previous equation shows that the PFC converter gives a minimum output power, even in the ideal case where the control loop voltage $V_C=0$:

$$P_{OUT\_MIN\_IDEAL} = \eta \frac{V_{in,pk}}{2\,R_S} K_{OFS} \left(\frac{2\,V_{REF\_OFS}}{\pi} - \frac{K_P\,V_{in,pk}}{2}\right). \tag{9}$$

If the power requested by the PFC load is lower than (9) the PFC converter enters burst-mode to keep the output voltage regulation, increasing a lot the THD.

Based on the previous considerations, to minimize the minimum output power deliverable by the converter, the idea is to minimize the offset voltage on the top of the sinusoid while keeping it near line zero-crossing to still guarantee the THD optimizer circuitry efficacy, as shown with the dotted-line in figure 2. This can be done externally to the IC controller, adding a positive offset voltage to the current sense information proportional to the line input voltage.

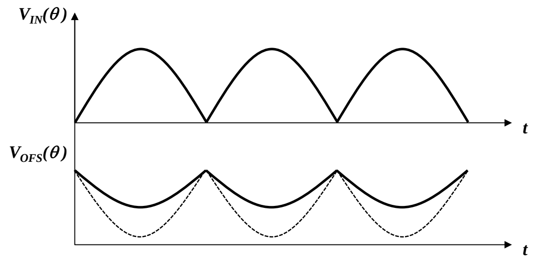

Figure 2. Offset voltage optimization proposal.

Referring to figure 1, and considering that $V_{IN} >> V_{CS}$, the current $I_G(\theta) = \frac{V_{IN}(\theta)}{R_G}$ is added to the CS pin and converted into a voltage through the R_{CS} filter resistor:

$$V_{CS\_OFS}(\theta) = R_{CS} \frac{V_{in,pk}\,\sin\theta}{R_G}. \tag{10}$$

Basically, the added $V_{CS\_OFS}(\theta)$ positive offset on the CS pin can be programmed to compensate the internal offset voltage on the peak of the sinusoid ($\theta=\pi/2$):

$$R_{CS} \frac{V_{in,pk}}{R_G} = K_{OFS} \left(V_{REF\_OFS} - K_P\,V_{in,pk}\right). \tag{11}$$

Solving (11) for the R_G resistor, results:

$$R_G = R_{CS} \frac{V_{in,pk}}{(V_{REF\_OFS} - K_P\,V_{in,pk})} \frac{1}{K_{OFS}}. \tag{12}$$

It is worth noting that the suggested R_G resistor depends on the input voltage, so the optimal compensation should be applied considering the higher nominal input voltage (e.g. 230 Vac in a standard wide range 90 Vac-265 Vac application), where the internal offset effect is more evident. Some small fine-tuning of the R_G resistor may be needed based on the real application.

Test results

The effectiveness of the proposal circuitry has been validated on the EVL6699-HVSL, a 150 W dimmable LED driver where the main characteristics of the whole AC/DC converter and the PFC power section based on L6564H are reported in table 1.

Considering the optimal compensation at 230 Vac input, applying the formula (12) the suggested R_G resistor results:

$$R_G = R_{CS} \cdot \frac{V_{in,pk}}{V_{REF\_OFS} - K_p V_{in,pk}} \cdot \frac{1}{K_1} = 470 \cdot \frac{230 \cdot \sqrt{2}}{6 - 7.06m \cdot 230 \cdot \sqrt{2}} \cdot \frac{1}{6.66m} = 6.2\ M\Omega$$

EVL6699-HVSL converter parameter	**Symbol**	**Value**	**Unit**
Line voltage range	V_{IN}	90 - 265	Vac
Line frequency range	f_{line}	47 - 63	Hz
Regulated output current	I_{LED}	0.05 to 1	A
Rated output voltage	V_{LED}	150	V
EVL6699-HVSL PFC section parameter			
Regulated output voltage	V_{OUT_PFC}	400	V
Inductance	L	310	µH
Current sense resistor	R_S	0.172	Ω
Input voltage partitioning resistors gain	K_P	7.06	mΩ/Ω
Current sense filter resistor	R_{CS}	470	Ω
IC controller	L6564H		

Table 1. Main characteristics of the 150W LED driver converter.

Figure 3 shows the THD comparison between the original board (dark) and the modified board (green) adding the suggested R_G resistor (6 MΩ), versus output power.

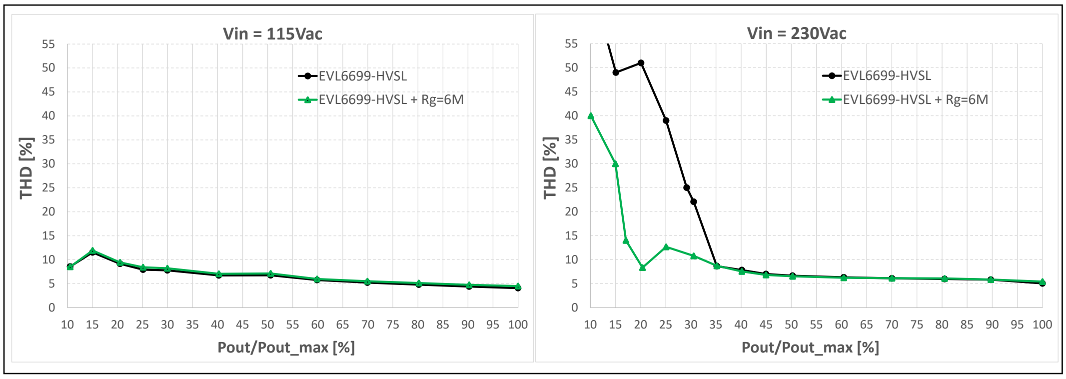

Figure 3. THD comparison adding the suggested R_G resistor.

The huge improvement of the THD at high line is evident. The burst-mode intervention is reduced from around 35% to around 15% of the load, keeping the same performance in terms of THD at medium-high load.

The following images show the Power Factor (PF) comparison results.

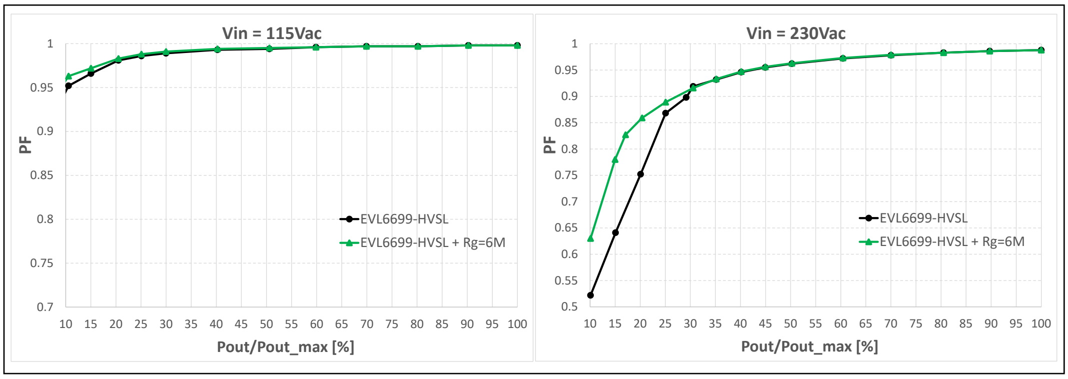

Figure 4. PF comparison adding the suggested R_G resistor.

Support material

Documentation
Datasheet, L6564 - Transition-Mode PFC controller
Datasheet, L6564H - High Voltage startup Transition-Mode PFC controller
Evaluation board, EVL6699-HVSL (150 V - 150 W LED driver with the L6564H and the L6699 Transition Mode PFC Pre-regulator, Half-Bridge LCC Resonant Converter)

Revision history

Date	Version	Changes
15-Feb-2022	1	Initial release